

Chapter #

## **PHASE LOCKED LOOP TEST METHODOLOGIES**

*Current Characterisation and Production Test Practices*

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### **1. INTRODUCTION: PLL OPERATION AND TEST MOTIVATIONS.**

Phase locked loops are incorporated into almost every large-scale mixed signal and digital system on chip (SOC). Various types of PLL architectures exist including fully analogue, fully digital, semi-digital, and software based. Currently the most commonly used PLL architecture for SOC environments and chipset applications is the Charge-Pump (CP) semi-digital type. This architecture is commonly used for clock synthesis applications, such as the supply of a high frequency on-chip clock, which is derived from a low frequency board level clock. In addition, CP-PLL architectures are now frequently used for demanding RF (Radio Frequency) synthesis, and data synchronization applications. On chip system blocks that rely on correct PLL operation may include third party IP cores, ADCs, DACs and user defined logic (UDL). Basically, any on-chip function that requires a stable clock will be reliant on correct PLL operation. As a direct consequence it is essential that the PLL function is reliably verified during both the design and debug phase and through production testing.

This chapter focuses on test approaches related to embedded CP-PLLs used for the purpose of clock generation for SOC. However, methods discussed will generally apply to CP-PLLs used for other applications.

## 1.1 Phase Locked Loop key elements operation and test issues.

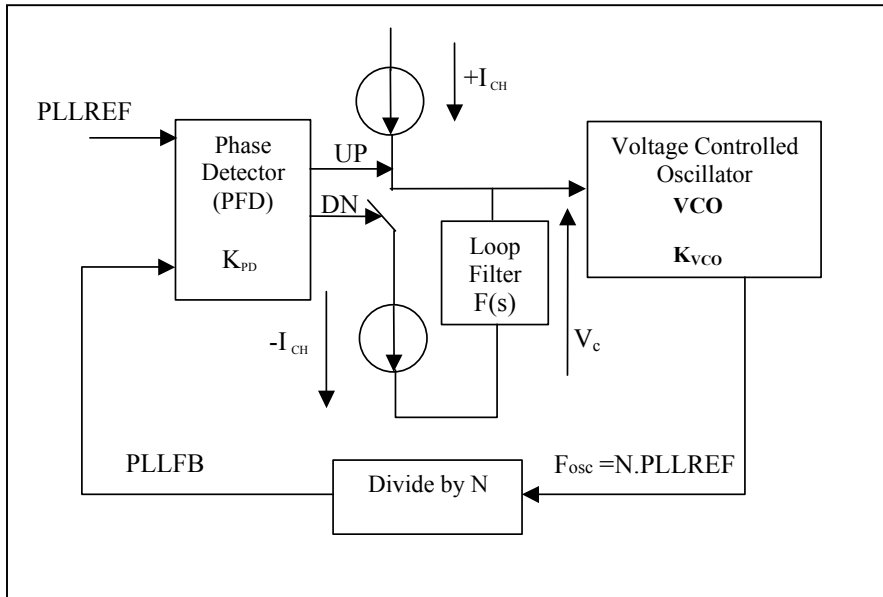


Figure 1 Block diagram of typical CP-PLL configuration

The charge-pump PLL architecture of figure 1 consists of a phase detector, a charge pump, a loop filter (LF), a voltage controlled oscillator (VCO) and a feed back divider ( $\div N$ ). The phase frequency detector (PFD) senses the relative timing differences between the edges of the reference clock and VCO clock (feedback clock) and applies charge-up or charge down pulses to the charge pump that are proportional to the timing difference. The pulses are most commonly used to switch current sources, which charge or discharge a capacitor in the loop filter. The voltage at the output of the loop filter is applied to the input of the VCO, which changes oscillation frequency as a function of its input voltage. Note that ideally when the feedback and reference clocks are equal, that is they are both phase and frequency aligned, the charge pump transistors will operate in such a way as to maintain the loop filter voltage at a constant value. In this condition, the PLL is “locked” which implies that the output signal phase and frequency is aligned to the input within a certain limit. Note that the division block up converts the VCO output frequency to an integer multiple of the frequency present on its reference input (PLLREF). It follows that when the PLL is in its locked state:

$$F_{out} = N \cdot PLLREF$$

Equation 1

In figure 1, the following conversion gains are used for the respective blocks.

- $K_{PD}$  = Phase detector gain =  $I_{ch}/2\pi$  (A r<sup>-1</sup>)
- $F(s)$  = Loop filter transfer function
- $K_{VCO}$  = VCO gain (r s<sup>-1</sup> v<sup>-1</sup>)

Using feedback theory the generalized transfer equation in the Laplace domain for the system depicted in figure 1 is.

$$H(s) = \frac{\theta_o(s)}{\theta_i(s)} = \frac{N \cdot K_{PD} \cdot K_{VCO} \cdot F(s)}{sN + K_{PD} \cdot K_{VCO} \cdot F(s)}$$

Equation 2

Note that by substituting suitable values for N and F(s) equation 1 will generally apply to any order PLL system. [1]. Specific transfer equations are provided as part of the loop filter description.

It must be noted that even for the case of a CP-PLL the implementation details for the blocks may vary widely, however in many applications designers attempt to design the PLL to exhibit the response of a second order system. This is due to the fact that second order systems can be characterized using well-established techniques. The response of a second order CP-PLL will be generally considered in this chapter. [2] [3] [4].

A brief description of each of the blocks now follows. Further, basic principles of CP-PLL operation are given in [1][3][5][6].

*Phase Frequency Detector:*

The phase detector most commonly used in CP-PLL implementations is the type 4 edge sensitive PFD. The PFD may be designed to operate on rising or falling edges, for the purpose of this discussion it will be assumed that the PFD is rising edge sensitive A schematic of this type of PFD is shown below.

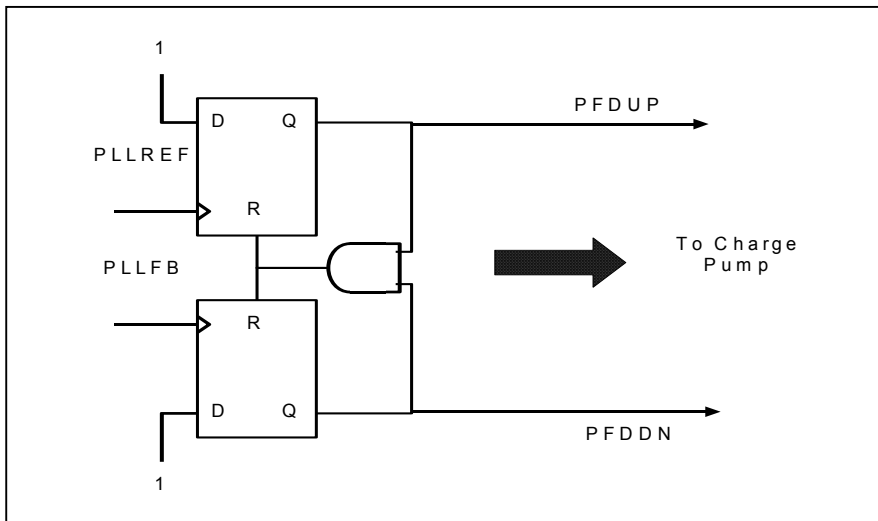


Figure 2 Typical implementation of type 4 PFD

In Figure 2, PFDUP and PFDDN represent the control signals for the up and down current sources respectively. When considering the operation of the PFD it is also useful to also consider the change in VCO output frequency. Considering phase alignment of the PFD input signals;  $\theta_{REF}$  will be used to designate the instantaneous phase of PLLREF and  $\theta_{FB}$  will be used to designate the instantaneous phase of the PLLFB signal. Using this convention and with reference to figure 2 and figure3 the PFD operation is now explained.

- (1)  $\theta_{FB}(t)$  leads  $\theta_i(t) \Rightarrow$  LF voltage falls and VCO frequency falls to try and reduce the difference between  $\theta_i(t)$  and  $\theta_{FB}(t)$ .
- (2)  $\theta_i(t)$  leads  $\theta_{FB}(t) \Rightarrow$  LF voltage rises and VCO frequency rises to try and reduce the difference between  $\theta_i(t)$  and  $\theta_{FB}(t)$
- (3)  $\theta_i(t)$  coincident with  $\theta_{FB}(t) \Rightarrow$  The PLL is locked and in its stable state.

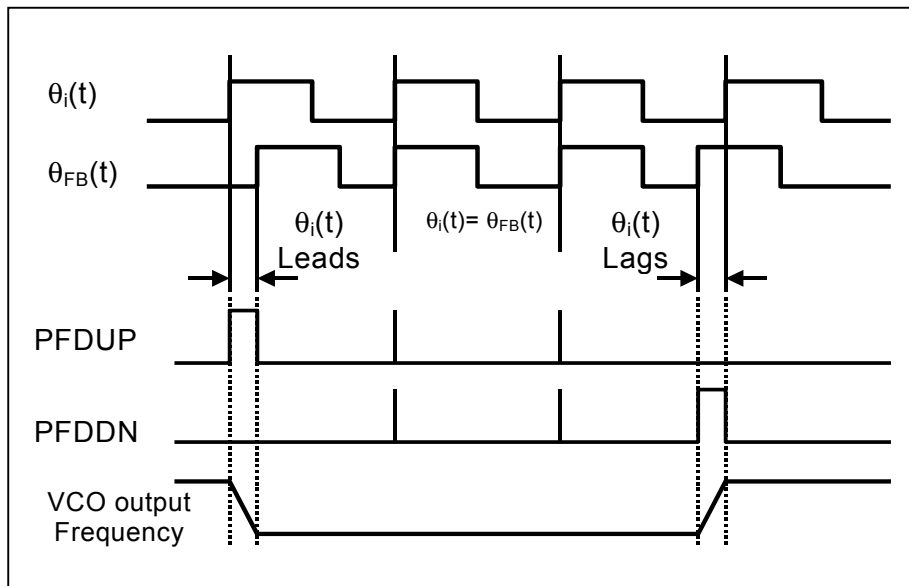


Figure 3 Operation of PFD and associated increase in VCO output frequency

#### Typical configurations for CP and $F(s)$ :

As above, the loop filter is designed to ensure that the whole system exhibits a second order response. A typical loop filter and charge pump configuration used for fully embedded CP-PLLs is illustrated in Figure 4.

The Laplace domain transfer function for this circuit is:

$$F(s) = R1 + \frac{1}{sC1}$$

Equation 3

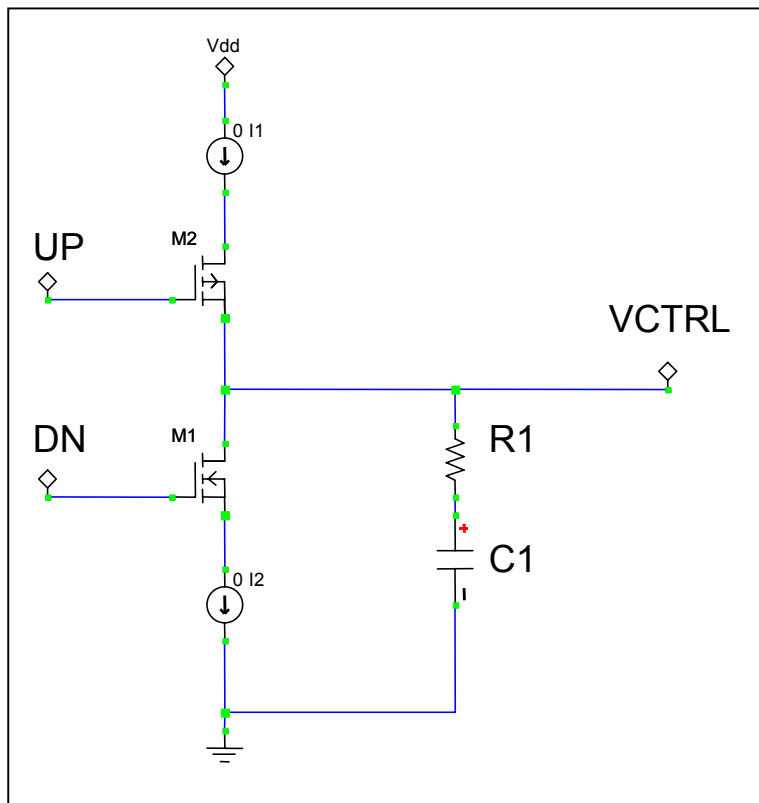


Figure 4 Typical Charge Pump and Loop filter configuration

Where we define following [3] :  $\tau_1=R1C1$

Now if the above loop filter transfer function is substituted into equation (2) for F(s). The following equation can be derived:

$$H(s) = \frac{\theta_o(s)}{\theta_i(s)} = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

Equation 4

Where:

$$\omega_n = \sqrt{\left(\frac{K_O I_P}{N 2\pi C_1}\right)}$$

Equation 5

$$\zeta = \frac{\tau_2}{2} \left[ \frac{K_O I_P}{N 2\pi C_1} \right]$$

Equation 6

It must be mentioned that for CP-PLLs in general and for embedded CP-PLLs specifically, that the loop filter node can be considered as the critical controlling node of the PLL. Any noise coupled into this node will generally manifest itself as a direct instantaneous alteration of the VCO output frequency, this action will be observed as PLL output jitter. Consequently PLL designers usually spend a great deal of design effort in screening this node. In addition, correct loop filter operation is essential if the PLL is to function properly over all desired operational ranges. Embedded loop filters usually include one or more large area MOSFET capacitors. These structures may be sensitive to spot defects, such as gate oxide shorts [7].

Matching of the Charge-Pump currents is also a critical part of PLL design. Leakage and mismatch in the Charge pump will lead to deterministic jitter on the PLL output.

### *Voltage Controlled Oscillator:*

For embedded CP-PLL configurations the VCO is usually constructed as a current starved ring oscillator structure. This is primarily due to the ease of implementation in CMOS technologies. The structure may be single ended or differential, with differential configurations being preferred, due to their superior noise rejection capabilities. A typical single ended current starved ring oscillator structure is illustrated in Figure 5.

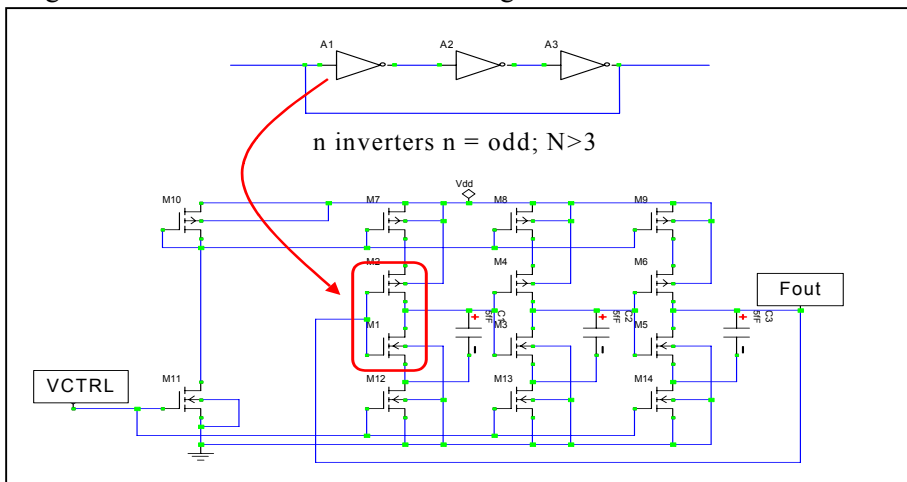


Figure 5 Single ended current starved ring oscillator structure.

In this circuit, VCTRL is the input control voltage taken from the loop filter node and Fout is the VCO output signal. Note that to prevent excessive loading of the VCO, its output is usually connected to buffer stages.

The transfer gain of the VCO is found from the ratio of output frequency deviation to a corresponding change in control voltage. That is:

$$K_{vco} = \frac{F2 - F1}{V2 - V1} (\text{MHzV}^{-1}) \text{ or } (rs^{-1}V^{-1})$$

Equation 7

Where F2 is the output frequency corresponding to V2 and F1 is the output frequency corresponding to V1. An example of experimental measurement of the VCO gain is given in section 2.1.1.4.

### *Digital structures:*

The digital blocks of the CP-PLL are generally constructed from standard digital structures. In some cases feedback dividers and PFDs may be constructed from standard cells. However, in many situations, to meet stringent timing requirements, the digital structures are constructed using full custom layout techniques. Digital structures of the PLL are generally less sensitive than the analogue structures and they are often modified to ease testing of the PLL.

## **1.2 Typical CP-PLL Test Specifications.**

Important functional characteristics that are often stated for CP-PLL performance are listed below:

- 1) Lock time / and ability to achieve lock from system startup.
- 2) Capture Range and Lock range.
- 3) Phase / Frequency step response time.
- 4) Overshoot.
- 5) Loop bandwidth ( $\omega_{3dB}$ ).
- 6) Output jitter.

All of the above parameters are interrelated to a certain extent. For example the loop bandwidth will have an effect on the PLL output jitter. However, loop bandwidth, lock time, overshoot and step response time are also directly related to the natural frequency and damping of the system. It must be mentioned that, certain non-idealities or faults may attribute to further jitter on the PLL output, or increased lock time. Examples of typical measurements for these parameters are provided in later sections.

Table 1 provides an initial analysis of testing issues for the PLL sub-blocks. Fault models that are suggested for use in fault coverage

calculations for each of the blocks. Further research and justification for the use of fault models in the key PLL sub-blocks are given in [7][8][9][10][11][12][13].

PLL Block	Structures		Direct access / modification	At speed testing required	Commonly Suggested Fault Models
	A	D			
(1) PFD		√	Yes	Yes	Single stuck at faults
(2) CP	√		No	Yes	MOS Transistor faults *
(3) LF	√		No	Yes	“”
(4) OSC	√	√	Yes	Yes	“”
(5) DIV		√	Yes	Yes	Single stuck at faults
* Mos transistor catastrophic faults: Gate to drain shorts; gate to source shorts; drain opens; source opens.					

Table 1 Common examples of test accessibility.

Note also that the fault models suggested in table 1 can also be used to assess the fault coverage of BIST (Built In Self Test) techniques. It should be noted however that many fault types are related to the structure realization of the PLL hence these guidelines should be used with care. Faults that may be implementation dependant include:

- Problems with interconnect due to pinholes or resistive vias.
- Coupling faults.

Obviously a high performance PLL will be routed in such a way so as to attempt to minimize the probability of these faults occurring.

### 1.2.1 Jitter Overview.

Jitter has been mentioned several times with respect to the PLL sub block descriptions. Non-Idealities, faults, or bad design practices, such as poor matching of structures, poor layout and insufficient de-coupling between critical functions can lead to excessive jitter in the PLL output. Jitter may be divided into two main classes as follows:



- Random Jitter (Gaussian Jitter): Is caused by non-deterministic events, such as coupling of electrical noise into the charge pump structures, the VCO control input, or the PLLs digital structures.
- Deterministic or correlated jitter: Can be viewed as changes in the PLL outputs instantaneous phase or frequency that can be directly correlated to changes in PLL operation or changes in the host system operation. Typical examples may be phase spurs due to charge pump mismatch, or a notable change in output jitter when a system output driver is switched.

For clock synthesis based applications jitter can be regarded as the amount of time variation that is present on the periodic output signal.

The diagram below shows a typical spread or bell shaped curve that would be used to represent truly random or Gaussian type jitter, superimposed upon this plot is a non Gaussian shape that may occur from deterministic jitter sources.

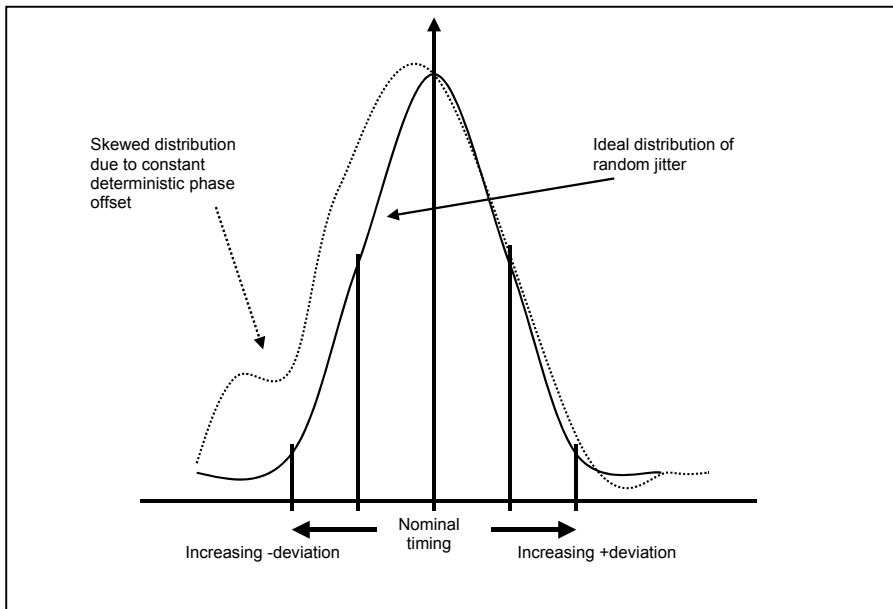


Figure 6 Ideal and non-ideal jitter probability density curves

As a general approximation, the maximum random signal jitter will increase to a peak-to-peak value of 6 standard deviations from the ideal case. However it, must be noted that due to non-deterministic effects, that the actual measured case may vary significantly from this. This statistical technique of viewing jitter is often used in conjunction with jitter histogram measurements. Obviously the confidence levels of the measurements will increase when an increasing number of measurements are taken. An example of this technique is given in later sections (see section 2.2.1).

A measurement often quoted that relates to non-deterministic jitter is that of RMS\_jitter. The expression for RMS\_jitter is given below.

$$RMS\_jitter = \sqrt{\frac{1}{N-1} \cdot \sum_{i=1}^N (T_i - \bar{T})^2}$$

Equation 8

Where  $\bar{T}$  is the mean of the measured time intervals and is defined as.

$$\bar{T} = \frac{1}{N} \cdot \sum_{i=1}^N T_i$$

Equation 9

In both of the above equations N represents the total number of samples taken and  $T_i$  represents the time dispersion of each individual sample.

For clock signals, jitter measurements are often classified in terms of short-term jitter and long term jitter. These terms are further described below:

Short term Jitter: This covers short-term variations in the clock signal output period. Commonly used terms include:

- **Period Jitter:** Is defined as the maximum or minimum deviation (whichever is the greatest) of the output period from the ideal period.
- **Cycle to Cycle Jitter:** Is defined as the period difference between consecutive clock cycles. That is Cycle-to-Cycle Jitter = [period (n) – period (n-1)]. It must be noted that Cycle-to-Cycle Jitter represents the upper bound for the period jitter.
- **Duty Cycle distortion Jitter:** Is the change in the duty cycle relative to the ideal duty cycle. The relationship often quoted for duty cycle is given below.

$$Duty\_cycle = \frac{High_{period}}{High_{period} + Low_{period}} \cdot 100 \quad (\%)$$

Equation 10

Where  $High_{period}$  is time duration the signal is high during one cycle of the waveform and  $Low_{period}$  is the time duration the signal is low over one period of the measured waveform. In an ideal situation the duty cycle will be 50%, the duty cycle distortion jitter will measure the deviation of the output waveform duty cycle from the ideal position. Typical requirements for duty cycle jitter is that it should be within 45 – 55 % [14] [15].

The above jitter parameters are often quoted as being measured in terms of degrees deviation with respect to an ideal waveform. Another metric often encountered is that of a UI (Unit Interval), where one UI is equivalent to 360°. A graphical representation of a unit interval is given below.

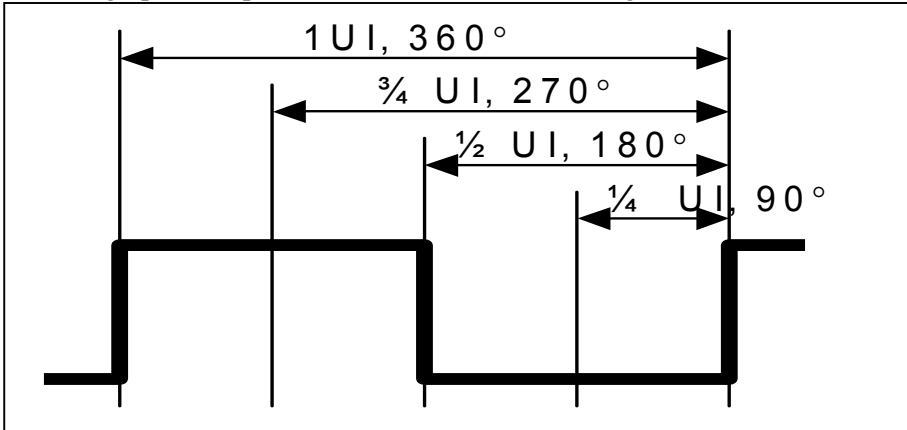


Figure 7 Graphical representation of a Unit Interval

**Long term Jitter:** Provides a measure of the long-term stability of the PLL output. That is, it represents the drift of the clock signal over time. It is usually specified over a certain time interval (usually a second) and expressed in ppm. For example, a long-term jitter specification of 1ppm would mean that a signal edge is allowed to drift by 1us from the ideal position in 1 second.

A graphical representation of all of the mentioned forms of jitter is provided below.

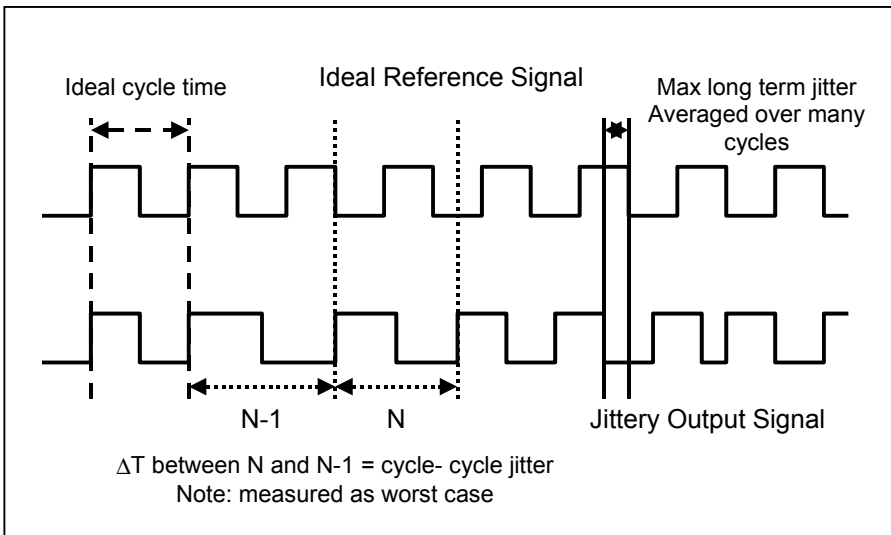


Figure 8 Pictorial summary of various types of jitter.

All of the above measurements, both long term and short term rely on either being able to discern the timing fluctuations of the signal when compared to an ideal reference or discern the timing difference between consecutive cycles. Absolute Jitter specifications will be dependant upon the specific application and will relate to the maximum output frequency of the PLL.

For example, in a 622Mbps SONET (Synchronous Optical Network) PLL [16] the maximum pk-pk generated jitter, is stated as 2.6 mUI. For this application. one unit interval is calculated as:

$$1UI = \frac{1}{622.08MHz} = 1.60ns$$

Equation 11

Therefore, 2.6mUI is equivalent to

$$2.6mUI = \frac{1UI}{1000} \cdot 2.6 = \frac{1.608ns}{1000} \cdot 2.6 = 4.1808ps$$

Equation 12

Further examples of jitter specifications and allowable tolerances are given in [17].

It can be seen from the above example that measurement of jitter requires highly accurate and jitter free reference signals that are a much higher frequency than that of the device being measured.

## **2. TRADITIONAL TEST TECHNIQUES.**

This section will explain traditional or commonly employed CP-PLL test techniques that are used for the evaluation of PLL operation. Many of the techniques will be applicable for an analogue or semi digital type of PLL or CP-PLL, however it must be recognized that although the basic principles may hold, the test stimuli may have to undergo slight modification for the fully analog case. The section is subdivided into two subsections, focusing on characterization and production test techniques respectively.

### **2.1 Characterization Focused Tests.**

In this subsection we will review typical techniques that are used to characterize a PLL system. Characterization in this context will refer to measurements made by the PLL designer upon an initial test die for the purpose of verifying correct circuit functionality, and to allow generation of the device or data sheet [18]. Characterization based tests usually cover a greater number of operational parameters than that carried out for production test. Also they can be carried out using specific special function test equipment and hardware, as appose to general-purpose production test equipment.

#### **2.1.1 Operational Parameter Based Measurements.**

The key parameter based measurements employed for CP-PLL verification generally consist of the following tests:

- 1) Lock Range and capture range.
- 2) Transient response:
  - Correct operation from power up of the system incorporating the PLL. This test is often ascertained using a frequency lock test (FLT).
  - Correct step response of the system, when the PLL is switched between two frequencies or phases.
- 3) Phase transfer function (or jitter transfer function monitoring):
  - To ascertain correct 3dB bandwidth of the PLL system.
  - To ascertain correct phase response of the PLL system.

The above tests can be considered to be full functionality tests as they are carried out upon the whole PLL system. It must also be mentioned that for

second order systems, both of the above techniques can be used to extract defining parameters such as  $\omega_n$  (natural frequency) and  $\zeta$  (damping).

Further tests are often carried out that are based upon structural decomposition of the PLL into its separate building blocks. These techniques are often used to enhance production test techniques [19][20]. Typical tests are;

- Charge pump current monitoring is used to ascertain the charge pump gain and hence the phase detector transfer characteristic. It is also used to monitor for excessive charge pump mismatch.
- 4) Direct control of the VCO is used to allow estimation of the VCO transfer characteristic.

The decomposition tests are also often coupled with some form of noise immunity test, that allow the designer ascertain the sensitivity of the VCO or charge pump structures to noise on the PLLs supply rails. As the CP currents and VCO control inputs are critical controlling nodes of the PLL, and determine the instantaneous output frequency of the PLL, any coupling of noise onto these nodes will cause jitter on the PLL output. Thus noise immunity tests are particularly important in the initial characterization phases. A more detailed discussion of the tests now follows.

#### 2.1.1.1 Lock range and capture range.

The normally encountered definitions for capture range and lock range are provided below.

- Capture range: Refers to the range of frequencies that the PLL can lock to when lock does not already exist.
- Lock range: The range of frequencies that the PLL can remain locked after lock has been achieved.

For certain applications these parameters are particularly important. For instance, lock range would need to be evaluated for frequency demodulation applications. When considering edge sensitive CP-PLLs the lock range is usually equal to the capture range.

For a CP-PLL synthesizer the lock range would be ascertained in the following manner for a single division ratio:

- 1) The CP-PLL would initially be allowed to lock to a reference frequency that is in the correct range for a particular divider setting.
- 2) The reference frequency would be slowly increased until the CP-PLL can no longer re-adjust its output to keep the PFDs inputs phase aligned.
- 3) When the CP-PLL fails to acquire constant lock the reference frequency is recorded.

This sequence is often aided by use of lock detect circuitry, that is used to provide a digital output signal when the PLL has lost lock.

#### **2.1.1.2 Transient type response monitoring.**

##### *Frequency Lock Test (FLT):*

An initial test that is carried out before more elaborate tests are employed is the frequency lock test (FLT). This test simply determines whether the PLL can achieve a stable locked condition for a given operational configuration. Stability criteria will be determined by the application and may consist of an allowable phase or frequency error at the time of measurement. Typically, this test is carried out in conjunction with a maximum specified time criteria, that is, if the PLL has failed to achieve lock after a specified time, then the PLL is faulty. The start of test initiation for the FLT is usually taken from system startup. It is common for this test to be carried out for various PLL settings, such as, maximum and minimum divider ratios, different loop filter settings etc. Due to its simplicity and the fact that it will uncover many hard faults and some soft faults in the PLL, this test is often used in many production test applications. A graphical description of the FLT is given below.

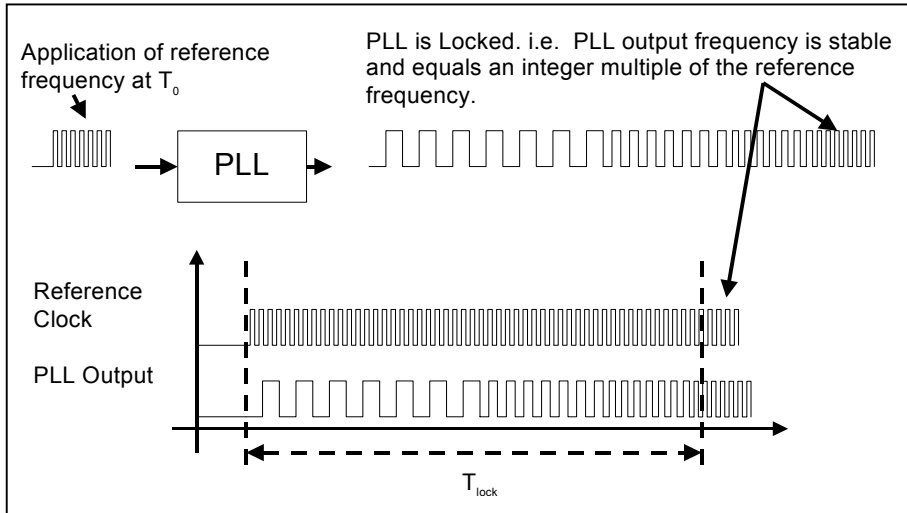


Figure 9 Graphical representation of a typical frequency lock test sequence

In the above diagram,  $T_0$  represents the start of the test and  $T_{lock}$  indicates the time taken to achieve lock.

In many applications the output frequency is simply measured after a predetermined time, this is often the case in ATE (Automated test equipment) based test schemes, where the tester master clock would be used to determine the time duration. Alternatively, in some situations the PLL itself is fitted with LD (lock detect) circuitry that produces a logic signal when the PLL has attained lock [20]. In this situation, a digital counter is started at  $T_0$  and stopped by the LD signal, thus enabling accurate lock time calculations to be made. Note that LD circuitry is not test specific, as it is often included in PLL circuits to inform other system components when a stable clock signal is available. However, sometimes a LD connection is fitted solely for DFT purposes. It must also be mentioned that in certain PLL applications it may be acceptable to access the loop filter node, if this is the case, the approximate settling time of the PLL can be monitored from this node. This technique is sometimes used for characterization of chipset PLLs, however, due to problems outlined in the previous sections it appears to be less commonly used for test of fully embedded PLLs.



*Step Response Test:*

The step response monitoring of PLL's is a commonly used bench characterization technique [2]; the basic hardware set-up is shown in Figure 10.

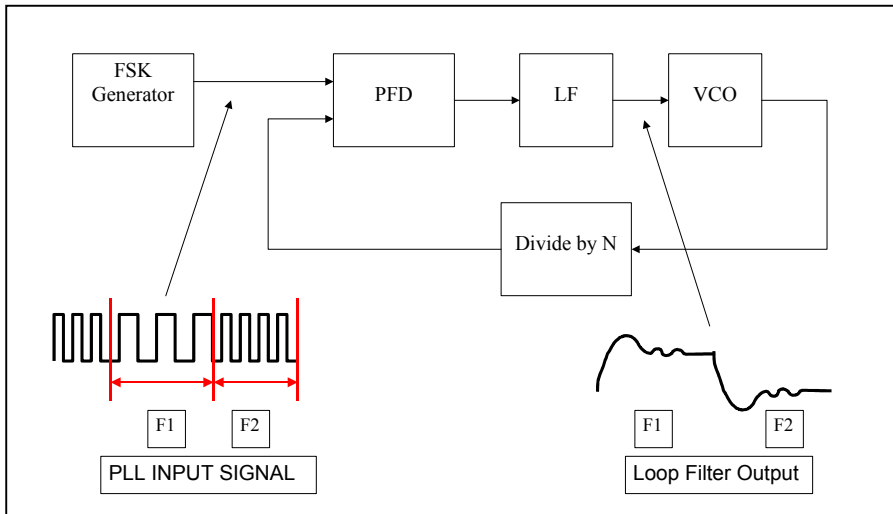


Figure 10 Basic equipment setup for PLL step response test

Further details relating to the above diagram are now given below:

- The input signal step is applied by using a signal generator set-up capable of producing an FSK signal. The signal is toggled periodically between F1 and F2. Note that a suitable toggling frequency will allow the system to reach the steady state condition after each step transition.
- If an external loop filter is used it is sometimes possible to measure the output response from the loop filter node. The signal measured at this node will be directly proportional to the variation in output frequency that would be observed at the PLL's output.

Also note that as the VCO output frequency is directly proportional to the loop filter voltage, the step response can also be measured at the VCO output. In fact, this is the technique that must be employed when loop filter access is prohibited. However, this technique can only be carried if test equipment with FT (frequency Trajectory) probing capabilities is available. This type of equipment allows a plot or oscilloscope trace of instantaneous frequency against time to be made, thus providing a correct indication of the transient step characteristics. Many high specification bench test equipment products incorporate FT functions, but it is often hard to incorporate the technique into a high volume production test plan.

An alternative method of introducing a frequency step to the system involves switching the feedback divider between  $N$  and  $N+1$ . This method will produce an output response from the PLL that is equivalent to the response that would be observed for application of an FSK input frequency step equal to the PLL's reference frequency. The technique can be easily verified with reference to equation 1.

The step response can be used to make estimates of the parameters outlined in section 1. To further illustrate the technique a graphical representation for a second order system step response is provided below.

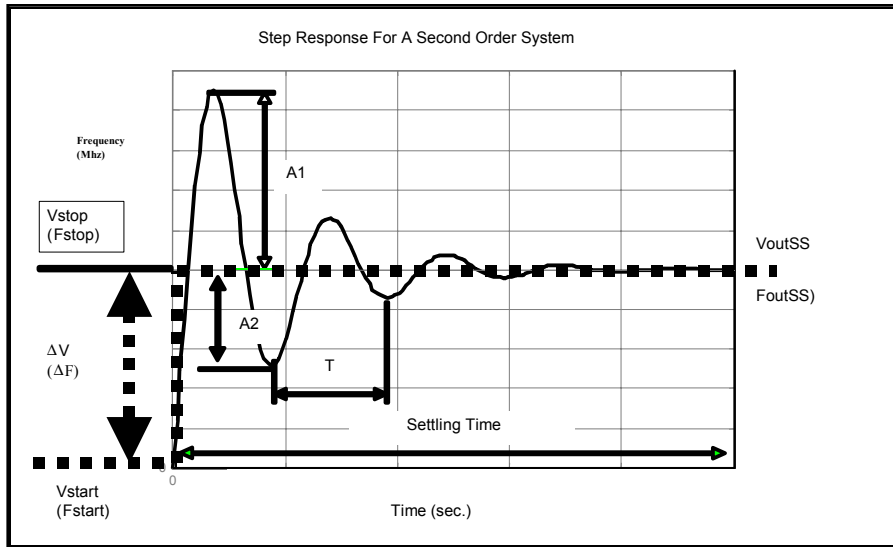


Figure 11 Graphical representation of a PLL step response.

In the above diagram the dashed line indicates the application of the input step parameter, and the solid line indicates the output response. Note that the parameters of interest are shown as  $V$  parameters and  $(F)$  parameters to indicate the similarity between a common second order system response and a second order PLL system response. An explanation of the parameters is now given.

- $V_{start}$  ( $F_{start}$ ): Is the voltage or frequency before the input step is applied.
- $V_{stop}$  ( $F_{stop}$ ): Is the final value of the input stimulus signal.
- $\Delta V$  ( $\Delta F$ ): Is the amount by which the input signal is changed.
- $V_{outSS}$  ( $F_{outSS}$ ): Represents the final steady state output value of the system.
- Settling time: The amount of time it takes after the application of the input step, for the system to reach its steady state value.

- A1: Peak overshoot of the signal.
- A2: Peak undershoot of signal.
- T: Time difference between the consecutive peaks of the transient response.

Direct measurement of these parameters can be used to extract  $\omega_n$  and  $\zeta$ . Estimation of the parameters is carried out using the following formulas that are taken from [2] and are also found in many control texts [4]. The formulas are valid only for under damped system i.e. one in which A1,A2 and hence T can be calculated. However if this is the case other parameters can be used to assess the system performance such as delay time or rise time. This is true for many applications, when what is really desired is the overall knowledge of the transient shape of the step response.

The damping factor  $\zeta$  can be found as follows:

$$\zeta = \frac{\ln\left(\frac{A1}{A2}\right)}{\left\langle \pi^2 + \left[ \ln\left(\frac{A1}{A2}\right)^2 \right] \right\rangle^{1/2}}$$

Equation 13

The natural frequency  $\omega_n$  can be found as follows:

$$\omega_n = \frac{2\pi}{T\sqrt{1-\zeta^2}}$$

Equation 14

Further PLL system theory and control system theory texts [2][3][4] also contain normalized frequency and phase step response plots, where the amplitude and time axis are normalized to the natural frequency of the system. Design engineers commonly employ these types of plots in the initial system design phase.

### 2.1.1.3 Transfer function monitoring.

In many applications a PLL system is designed to produce a second order response. It must be noted that although second order systems are considered

here, measurement of the transfer functions of higher order PLL loops can provide valuable information about system operation, and can be achieved using the methods explained here.

A bode plot of the transfer function of a general unity gain second order system is shown in Figure 12.

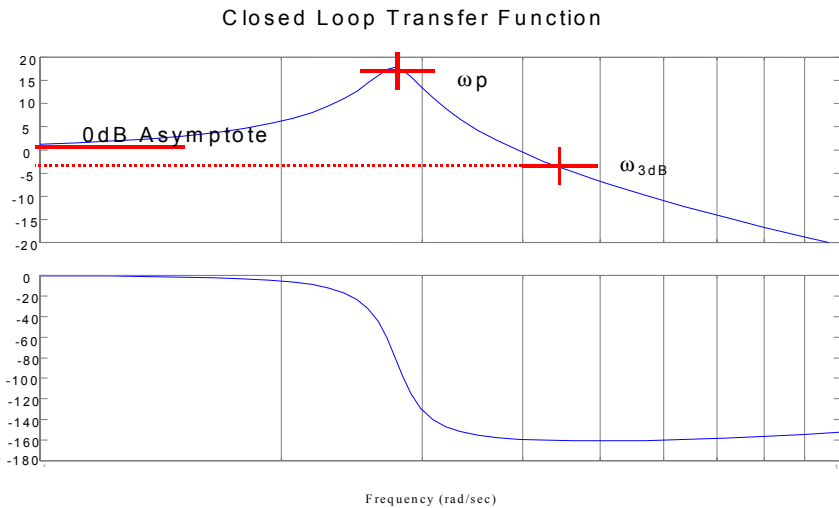


Figure 12 : Generalised bode plot for a second order

Typical parameters of interest for a second order system are highlighted in the above diagram; these are now explained in context with a PLL system:

**0dB Asymptote:** For a unity gain system, within the 3db frequency (see  $\omega_{3dB}$  below), the magnitude of the gain will tend to 1 (0dB) as the frequency of the excitation signal is reduced. The slope of this decrease will be determined by the damping of the system. In a similar manner the relative phase lag between the input and output of the system will tend to  $0^\circ$ . **Note** for a PLL the magnitude of the response within the loop bandwidth can be assumed to be unity [8]. As explained in later sections this is an important observation when considering PLL test.

**$\omega_p$ :** This is frequency where the magnitude of the system response is at its maximum. It is directly analogous to the natural frequency ( $\omega_n$ ) of the system. In addition, the relative magnitude of the peak (above the unity gain value) can be used to determine the damping factor ( $\zeta$ ) of the system. Relationships between  $\zeta$ , the dB Magnitude and the normalised radian frequency are available in many texts concerning Control or PLL theory [2][3][4].

**$\omega_{3dB}$ :** Following [1] this defines the one-sided loop bandwidth of the PLL. The PLL will generally be able to track frequency variations of the

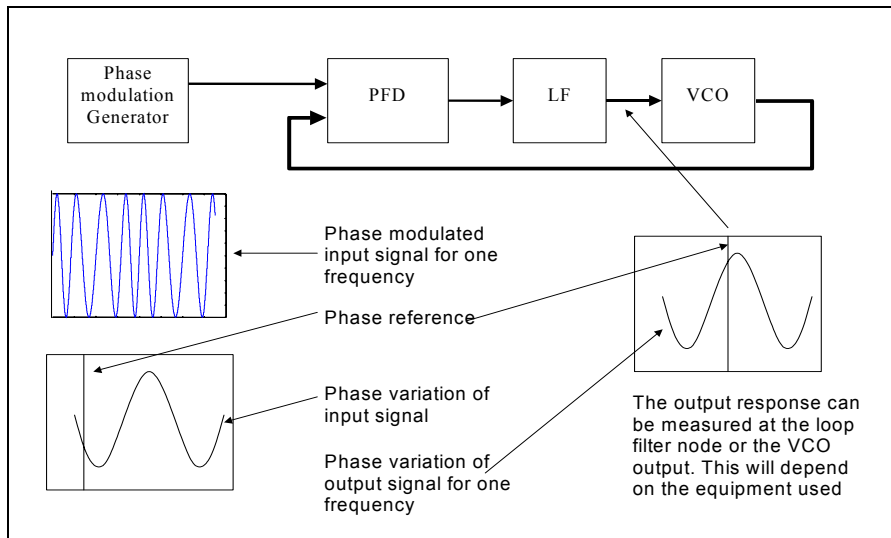


Figure 13 Illustrating application of a PLL transfer function measurement.

input signal that are within this bandwidth, and reject variations that are above this bandwidth.

For normally encountered second order systems i.e. ones with a voltage, current or force inputs and corresponding voltage, current or displacement outputs, the bode plot is constructed by application of sinusoidally varying input signal at different frequencies, the output of the system is then compared to the input signal to produce magnitude and phase response information. However the situation is slightly different for the PLL systems we are considering. In this situation the normal input and output signals are considered to be continuous square wave signals. The PLL's function is to phase align the input and output signals of the PLL system.

It can be seen from equation (2) and figure (1) that to experimentally measure the PLL transfer function we need to apply a sinusoidal variation of phase about the nominal phase of the input signal  $\theta_i(t)$ , i.e. we sinusoidally phase modulate the normal input signal. The frequency of the phase change is then increased and the output response is measured. The block diagram for an experimental bench type test set-up is shown in Figure 13.

For the above test, the output response can be measured at the loop filter node or the VCO output. The output of the loop filter node will be a sinusoidal varying voltage. The output of the VCO will be a frequency (or phase) modulated signal. Magnitude measurements taken at a sufficiently low point below  $\omega_p$  can be approximated to unity gain i.e. the PLL exhibits 100% feedback within the loop bandwidth. Additionally, the phase lag can be approximated to  $0^\circ$ . This means that all measurements taken from the

PLL output can be referenced to the first measurement. Figure 14 shows the method for phase measurement calculation between input and output.

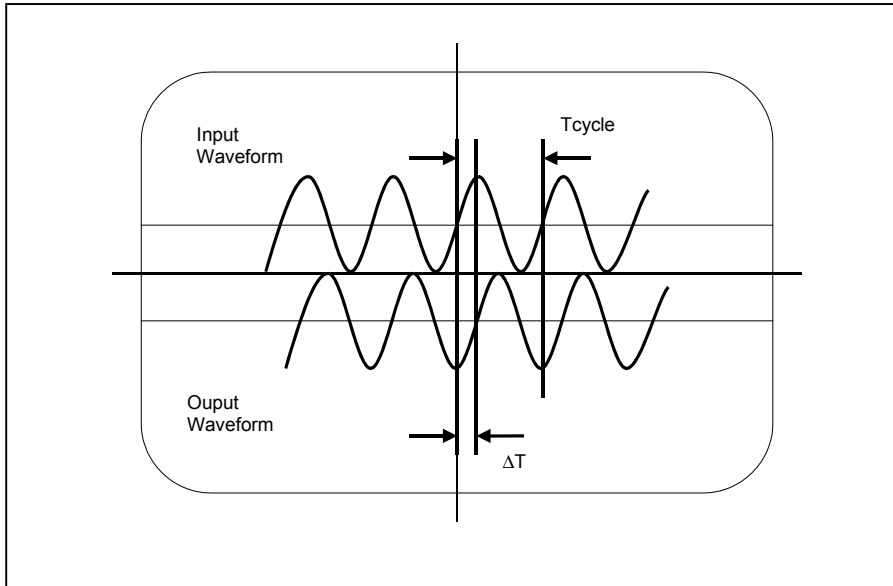


Figure 14 Measurement of phase difference between input and output.

Tcycle represents the time measured for one complete cycle of the input waveform.  $\Delta T$  represents the measured time difference between the input and output waveform.

Using Tcycle and  $\Delta T$ , the phase difference ( $\Delta\phi$ ) between the input and output signal can be estimated using the following relationship.

$$\phi(j\omega) = \Delta\phi = \frac{\Delta T}{T_{\text{cycle}}} \cdot 360 \quad (\text{Degrees})$$

Equation 15

For measurement of the magnitude response it must be recalled that well within the loop bandwidth the PLL response can be approximated as unity. It follows that an initial output signal resulting from an input signal, whose modulation frequency is sufficiently low, can be taken as a datum measurement. Thus, all subsequent measurements can be referenced an initial output measurement, and knowledge of the input signal is not required. For example, if an initial measurement was taken for a modulation of 100Hz, subsequent measurements could be carried out using the following relationship.

$$|H(j\omega)dB| = 20 \log_{10} \frac{Vm_{100Hz}}{Vm_N} \quad (\text{dB})$$

Equation 16

Where  $V_{m_{100\text{Hz}}}$  is the peak-to-peak voltage measured at an input modulation frequency of 100Hz and  $V_{m_N}$  is the Nth peak to peak voltage output for a corresponding modulation frequency.

The technique described above for phase transfer monitoring is almost identical to a similar test technique known as jitter transfer function monitoring [21][22]. However, in this case a known jittery source signal is used as the phase modulation signal, as appose to the sine wave modulation mentioned in this text.

#### **2.1.1.4 Structural decomposition.**

This subsection will outline common structural decomposition tests that are often used to ease PLL characterization. In the interests of brevity emphasis towards the analogue sub circuits of the PLL will be given. With reference to section 1 and the associated equations it can be seen that the PLL system is broken down into three main analogue type blocks, consisting of the charge pump, the loop filter and the voltage controlled oscillator. These are considered to be critical parts of the PLL, hence much design effort is spent on these blocks. The blocks are often designed independently so that the combination of the associated transfer characteristics will yield the final desired PLL transfer function. In consequence, it seems logical to attempt to verify the design parameters independently. Typical parameters of interest that are often checked include:

- Absolute Charge Pump Current.
- Charge Pump mismatch.
- VCO gain.
- VCO linearity.

If direct access to the loop filter control node is permitted, all of these tests can be enabled using relatively simple methods. Also, to allow these tests to be carried out, extensive design effort goes into construction of access structures that will place minimal loading on the loop filter node. However, injection of noise into the loop is still a possibility and the technique seems to be less commonly used. A brief explanation of common test methods is now provided.

### Charge Pump measurements:

A typical test setup for measuring the Charge pump current is shown in Figure 15.

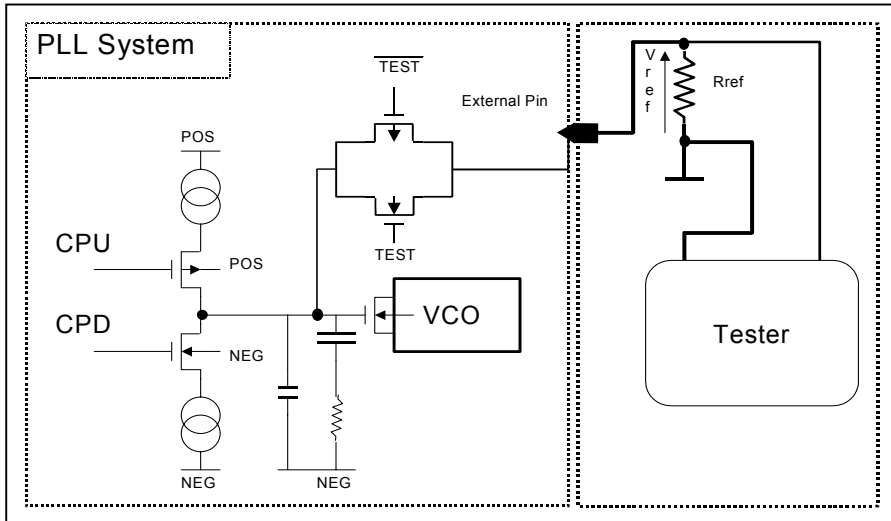


Figure 15 Direct access measurement of charge pump current.

Here, CPU is the up current control input, CPD is the down current control input, TEST is the test initiation signal that couples the loop filter node to the external pin via a transmission gate network, Rref is an external reference resistor, and Vref is the voltage generated across Rref due to the charge pump current. The tester senses Vref, and thus the charge pump current can be ascertained. A typical test sequence for the charge pump circuitry may contain the following steps.

- 1) Connect the loop filter node to the external reference network by enabling the TEST signal.
- 2) Activate the up current source by disabling CPD and enabling CPU.
- 3) Wait a sufficient time for the network to settle.
- 4) Measure the resultant UP charge pump current using the relationship.

$$I_{cpu} = \frac{V_{refup}}{R_{ref}}$$

Equation 17

- 5) Activate the down current source by disabling CPU and enabling CPD.
- 6) Wait a sufficient time for the network to settle.



7) Measure the resultant DOWN charge pump current using the relationship.

$$I_{cpd} = \frac{V_{refdn}}{R_{ref}}$$

Equation 18

An estimate of the charge pump current mismatch can be found by subtracting the results of equation 17 and equation 18. Also the CPU and CPD inputs can often indirectly controlled via the PFD inputs. Therefore, removing the necessity of direct access to these points and additionally providing some indication of correct PFD functionality.

Note that in the previous description, the test access point is connected to an inherently capacitive node consisting of the VCO input transistor, and the loop filter capacitors respectively. In consequence, if no faults are present in these components, there should be negligible current flow through their associated networks. It follows that this type of test will give some indication of the loop filter structure and interconnect faults.

*VCO measurments:*

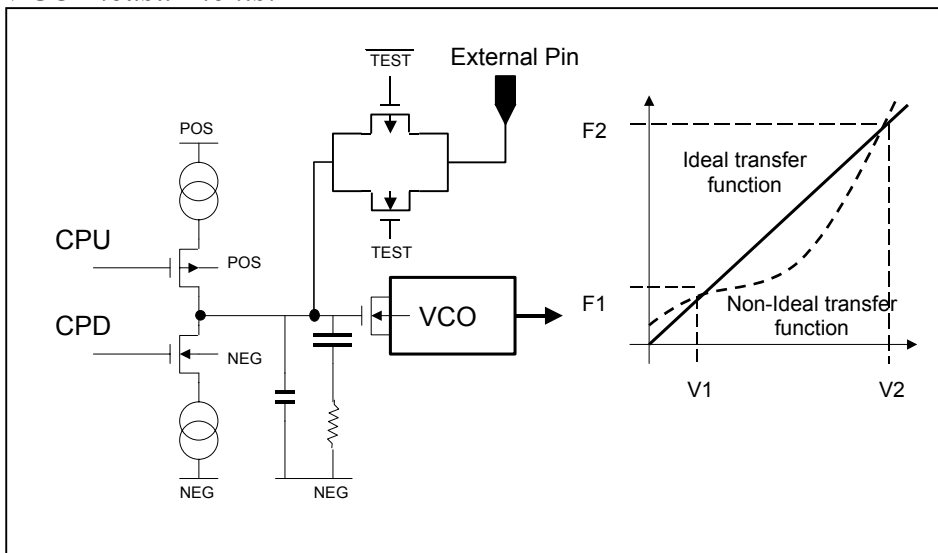


Figure 16 VCO test setup.

A typical test set up to facilitate the measurement of the VCO gain and linearity is shown in Figure 16 where CPU is the charge pump up current control input, CPD is the charge pump down current control input, and TEST is the test initiation control input. A typical test sequence would be carried out as follows:

- 1) Initially both charge pump control inputs are set to open the associated charge pump switch transistors. This step is carried out to isolate the current sources from the external control pin.
- 2) A voltage  $V1$  is forced onto the external pin.
- 3) The external pin is connected to the loop filter node by activation of the TEST signal.
- 4) After settling, the corresponding output frequency  $F1$  of the VCO is measured.
- 5) A higher voltage  $V2$  is then forced onto the external pin.
- 6) After settling, the corresponding output frequency  $F2$  of the VCO is measured.

In the above sequence of events the values chosen for the forcing voltages will be dependant upon the application.

After taking the above measurements the VCO gain can be determined using the following relationship.

$$K_{VCO} = \frac{F2 - F1}{V2 - V1} (\text{Hz} / V)$$

Equation 19

In certain applications it may be necessary to determine VCO non-linearity, this can be determined by taking incremental measurements of the VCO gain between the points  $V1$  and  $V2$  in Figure 16.

## 2.2 Production Test Focused.

In many situations, due to the problems stated in previous sections the FLT may be the only test carried out on embedded phase locked loops. A particular test plan may therefore include the criteria that the PLL must lock within a certain time for a certain set of divider settings. Often to enhance the FLT results, structural decomposition and ad-hoc DfT techniques such as the ones outlined in the previous sections are used. The PLL is also generally provided with various DfT techniques incorporated into the digital structures, such as:

- Direct access to PFD control inputs and outputs.
- Direct control of feedback divider inputs.
- Direct clock propagation to feedback divider.
- Direct monitoring of feedback divider.

In addition, to these features, an embedded PLL will normally have a bypass mode that allows other on chip circuitry to receive clock signals from an external tester as appose to the PLL itself. This mode allows other on chip circuitry to be synchronized to the tester during system test. In this situation the PLL core is often placed in a power down mode. Particular examples of generic production test methodologies are provided in [18][19].

Ad-hoc DfT methods can be of use for PLL testing, however some of the associated problems, such as, noise injection, and analogue test pin access can introduce severe limitations, especially when considering test for multiple on-chip PLLs. In consequence, there has been recent interest into fully embedded BIST techniques for PLLs. An overview of BIST strategies is presented in section 3.

**2.2.1 Jitter Measurements.**

This section will provide an outline of typical jitter measurement techniques. Accurate jitter measurements generally require some form of accurate time based reference. Accuracy in this context refers to a reference signal that possesses good long-term stability and small short-term jitter as the reference signal jitter will add to the device under tests generated jitter and be indistinguishable in the final measurement. In consequence, the reference jitter should be at least an order of magnitude less than the expected output jitter of the device under test. For the following discussions it will be assumed that a good reference signal exists. It must be noted that much of the literature devoted to new jitter test techniques, appears to concentrate upon generation of accurate time based measurements, however the basic analysis principal often remain similar. Commonly used measurement and analysis techniques include period measurements and histogram measurements. These techniques are explained below.

*Period based jitter measurments:*

Period based measurements essentially consist of measuring the time difference between equally spaced cycles of a continuous periodic waveform. A graphical representation of the technique is shown in Figure 17.

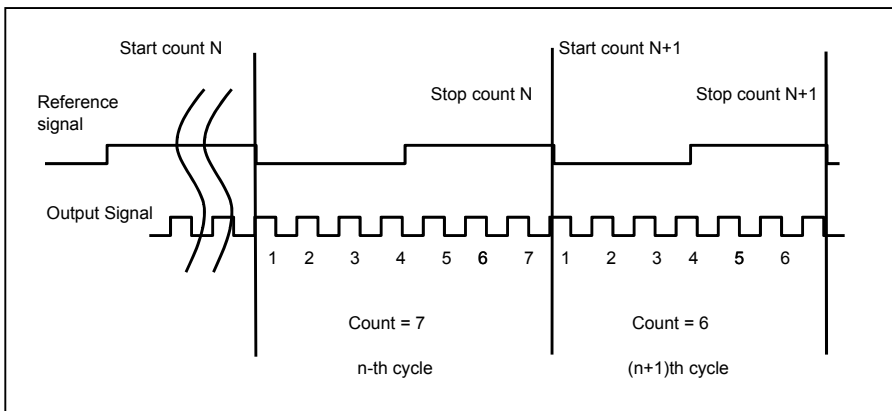


Figure 17 Representation of period based measurements.

This technique essentially carries out a frequency counting operation on the PLL output signal and will measure or count the number of PLL output transitions in a predetermined time interval (gate time) determined by the reference signal. The difference between successive counts will be related to the average period jitter of the PLL waveform. Obviously this method cannot be used to carry out the short-term cycle to cycle jitter measurements. Accuracy of this technique will require that the PLL output signal frequency is much higher than the gate signal.

The signals would be gated as shown in Figure 18 and would be used with fast measurement circuitry to initiate and end the measurements.

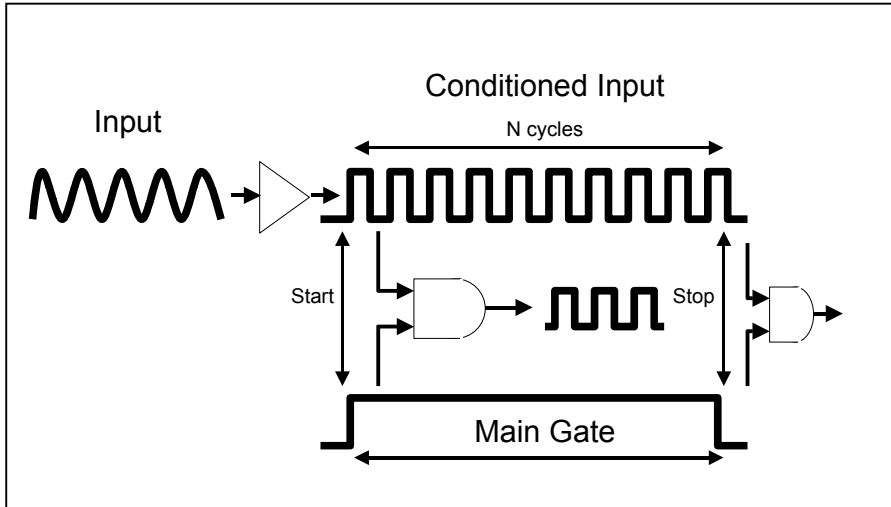


Figure 18 Illustrating gating of period measurement signals.

### *Histogram analysis*

Histogram based analysis is often carried out using a strobe based comparison method. In this method the clean reference signal reference signal is offset by multiples of equally spaced time intervals. That is the reference signal edge can accurately be offset from the ideal position by.

$$N \cdot \Delta T$$

Equation 20

Where N represents the maximum number of time delays that the reference signal edge can be displaced by and  $\Delta T$  is the minimum time resolution.

The measured signal is then compared to ascertain how many times its edge transition occurs after consecutive sets of the displaced edges. A Jitter histogram of the measured waveform is then constructed by incrementing N

and counting the occurrences of the rising edge over a predetermined set of measurements. A value of  $N = 0$ , will correspond to a non-delayed version of the reference signal. The measurement accuracy will be primarily dependant upon  $\Delta T$ , and  $\Delta T$  should be an order of magnitude below the required resolution. For example, 100ps measurement accuracy would require a  $\Delta T$  of 10ps.

An illustration of strobe edge placement for  $N=7$  is shown in Figure 19.

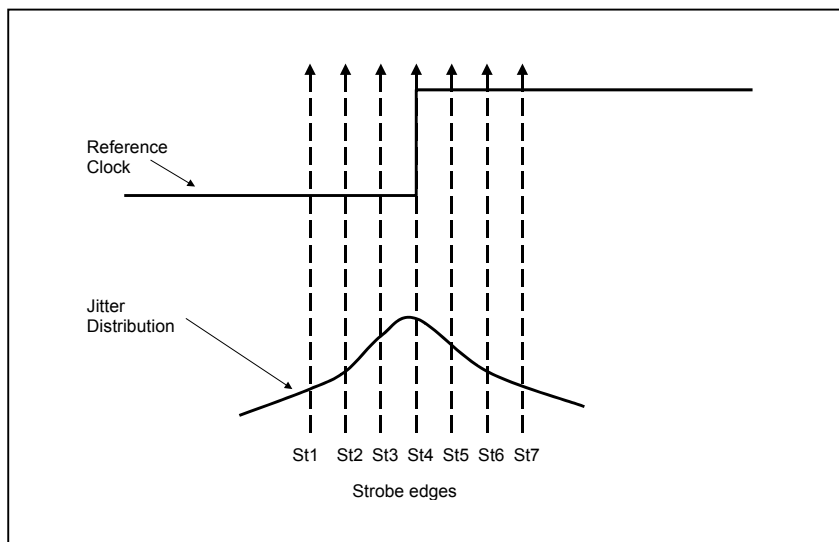


Figure 19 Example of strobe edge placement for 7 edges

As an example the count values could be collected from a given set of 100 measurements.

Strobe position number	Failure Count	Pass Count
St1	4	96
St2	15	85
St3	35	65
St4	50	52
St5	65	35
St6	85	15
St7	90	10

Table 2 Example values for histogram-based measurement.

The values from the table would then be used to construct the appropriate jitter histogram as shown in Figure 20.

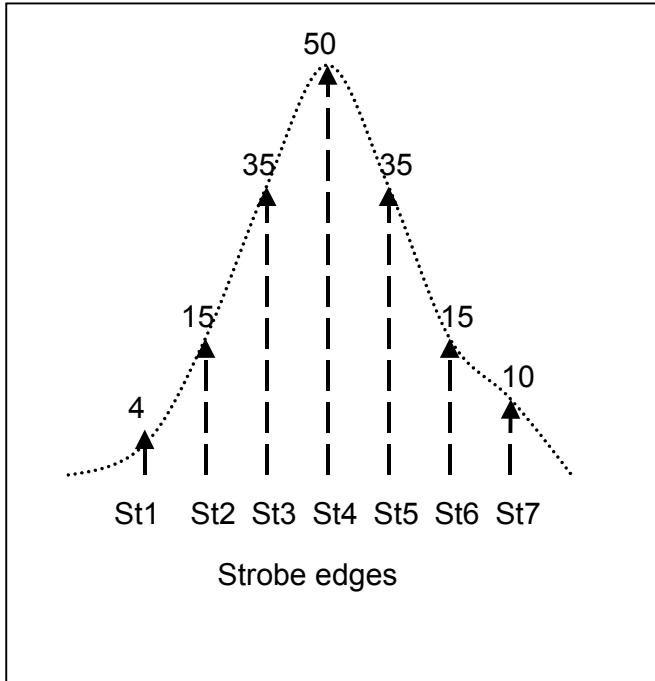


Figure 20 Jitter Histogram constructed from the values in table 2

It must be mentioned that various other techniques exist and are used to facilitate approximation of jitter such as, indirect measurements and Fourier based methods. For indirect measurements, a system function reliant on the PLL clock signal is tested, typical examples may include SNR testing of ADC or DAC systems. For Fourier based methods the signal of interest is viewed in the frequency domain as appose to the time domain, and the resultant phase noise plot is examined. Proportionality exists between phase noise within a given bandwidth and the corresponding jitter measurement, thus allowing jitter estimation. [23][24].

### 3. BIST TECHNIQUES.

Although the primary function of a PLL is relatively simple, previous sections have shown that there are a wide range of specifications that are critical to the stability and performance of PLL functions that need to be verified during Engineering and Production Test. These specifications range from Lock time and Capture range to key parameters encoded in the phase transfer function such as damping and natural frequency. Parameters such as jitter are also becoming more critical as performance specifications become more aggressive.

The challenge therefore associated with self-testing PLL's is to find solutions that can;

- be added to the design with minimal impact of the primary PLL function
- have minimal impact of the power consumption
- involve minimal silicon overhead
- can be implemented by non-specialists
- guarantee's detection of faults through either direct or indirect measurement of key specifications and
- be tolerant to normal circuit noise, component offsets process spreads, temperature and supply variations.

The following section identifies several BIST strategies proposed for PLL structures. Only the basic techniques are described here. The reader should consult the publications referenced for more information on practical implementation issues, limitations and potential improvements.

A fully digital BIST solution was proposed by Sunter & Roy [10]. This solution is restricted to semi-digital types of PLL and based on the observation that the open loop gain is linearly dependent on the key parameters associated with the PLL , that is:

$$G_{OL} = \frac{K_p K_v G(s)}{N.s}$$

Where :

$K_p$  - Gain of the phase detector which is a function of the charge pump current

$G(s)$  - frequency dependent gain of the low - pass filter or integrator

$K_v$  - gain of the VCO in radians/sec/volt

$N$  - digital divider integer

$s$  - Laplace variable

The BIST solution opens the feedback loop to ensure the output of the phase detector is independent of the VCO frequency. This is achieved by adding a multiplexor to the PLL input as shown in fig 21. A fully digital method is used to derive an input signal with a temporary phase shift. The method uses signals tapped from the divide by N block in the feedback loop to generate an output that is 180° out of phase relative to the input for 1-cycle of the reference clock only. This phase shift is activated on receipt of a logic “1” on the “Delay Next Cycle” signal.

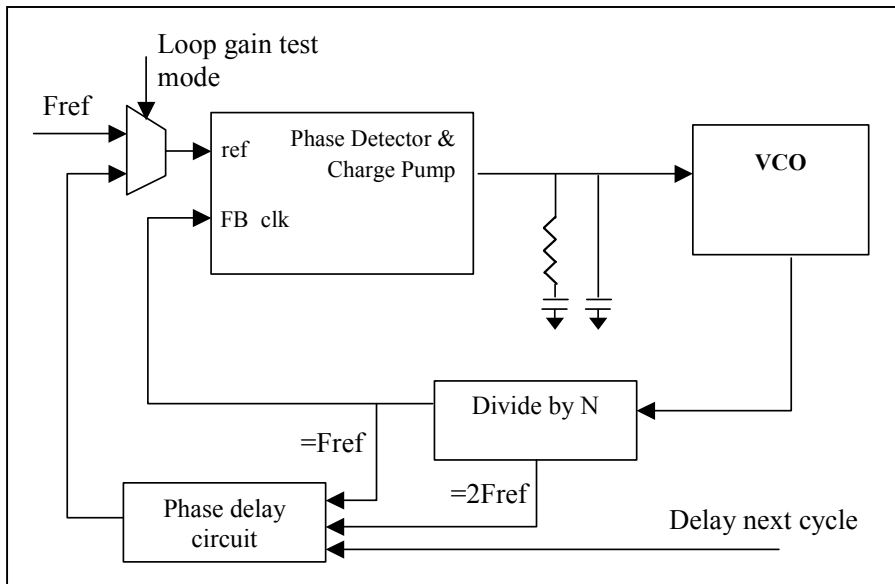


Fig. 21 Circuit for measuring loop gain

This phase shifted signal is applied to the phase detector via the input multiplexor. The strategy used eliminates problems in measuring very fast frequency changes on the VCO output that would result if a constant phase shift was applied. In this architecture, the VCO frequency will change only during the cycle where the phase is shifted. Following this cycle the VCO will lock again (zero phase shift on the input) hence it is relatively easy to measure the initial and final VCO frequencies and calculate the difference. The relationship between the change in VCO frequency as a function of the phase shift on the input, and the reference clock is:

$$\Delta\omega_{vco} = \frac{K_v \delta \cdot I_{cp}}{f_{ref} \cdot C}$$



and the open loop gain is given by:

$$G_{OL} = \frac{\Delta\phi_{FB}}{\Delta\phi_{FB}} = \frac{K_v \delta \cdot I_{cp}}{2\pi f_{ref}^2 \cdot NC}$$

So in summary, a digital circuit can be added to the divide by N block to generate a known phase shifted input for 1 cycle (stimulus generator) and a multiplexor added to the PLL input to allow the loop to be broken and the phase shifted signal from the stimulus generator to be applied. All that remains is the implementation of an on-chip solution to measure the output frequency change. This can be achieved digitally using a gated binary counter with a known reference frequency input.

Capture and Lock range measurements are also possible using this architecture by measuring the maximum and minimum frequencies of the lock / capture range. This is achieved by continuously applying a frequency error to force the output frequency to its maximum or minimum value at a controlled rate. The implementation involves connecting the PLL input to an output derived from the divide by N block with a frequency equal to, double or half the VCO output frequency. The VCO output frequency is continually monitored until the rate of change approaches a defined “small” value. This last frequency measurement is recorded. Lock time can also be measured in this testing phase by closing the PLL loop after this maximum or minimum frequency has been achieved and counting the number of reference clock cycles to the point at which the PLL locks.

An alternative architecture for on-chip measurement of the phase transfer function is described Burbidge & Richardson [25] and utilises an input multiplexor as above, a digital control function and a phase frequency detector with a single D-type flip flop added to its output as shown in Figure 22.

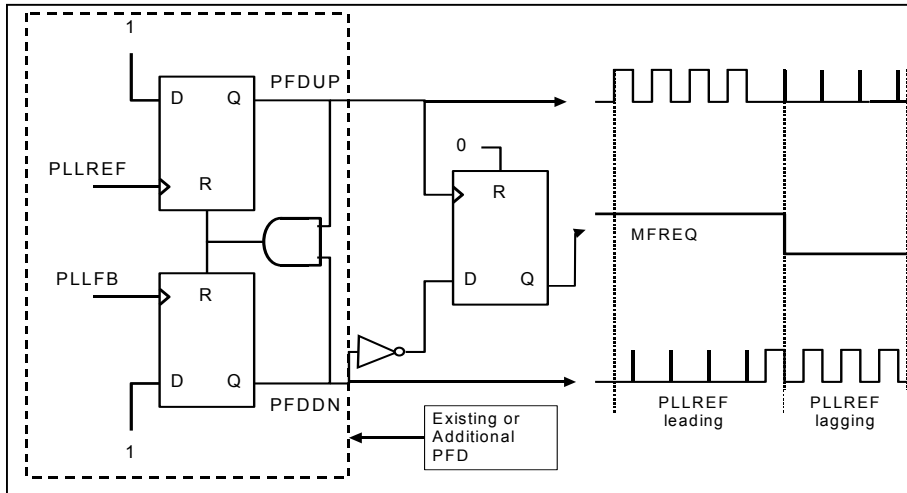


Figure 22 Sampling of output frequency

The purpose of this modified phase detector is to detect the peak output which corresponds to the response of the PLL to the peak value of the input phase. If a “strobe” signal is generated by the input stimulus generator when the input phase is at its peak, measurement of the time delay between the input strobe and the output change on the Q output of the D-type can generate the phase response at a fixed input frequency. In addition, the point at where this D-type output changes corresponds to the PLL being locked hence measurement of the output frequency at this point will allow the magnitude response of the PLL to be calculated at the reference frequency of the input stimuli. Repeating this process for different values of input frequency will allow the phase transfer function to be constructed. This modified phase detector and the methodology described above is used within the overall BIST architecture shown in Figure 23. The input multiplexor M2 is used to connect or break the feedback loop and apply identical inputs to the PLL forward path to artificially lock the PLL.

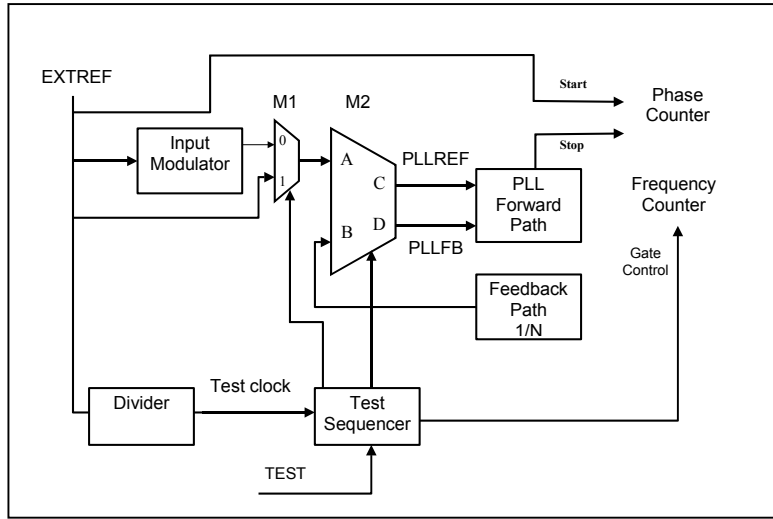


Figure 23 BIST architecture

The algorithm used to construct the phase transfer function is as follows:

Test Stage	M1	M2		Comments
(1) Ref set	0	A=C	B=D	Apply digital modulation with frequency FN Start Phase counter (counter referenced to EXTREF)
(2) Set Phase counter	0	A=C	B=D	Start phase counter at peak of input modulation
(2) Monitor Peak	0	A=C	B=D	Monitor for peak output signal frequency
(3) Peak occurred Lock PLL stop Phase counter	X	A=C	A=D	Holds the output frequency constant.
(4) Measure frequency and phase	X	A=C	A=D	Count output frequency and store. Store the result of the phase counter.
(5) Increase Modulation Frequency FN and repeat steps 1 to 4 until all frequencies of interest have been monitored.				

Table 3 - Test Sequence

Note that this technique requires an input stimulus generator that provides either a frequency or phase-modulated input with a strobe signal generated at the peaks. Either frequency modulation using a digitally controlled oscillator or phase modulation using multiplexed delay lines can be used.

A third method of achieving a structural self-test of a PLL structure was proposed by Kim and Soma [9] and involves injecting a constant current into the PLL forward path and monitoring the loop filter output which is usually a multiple of the input current injected and a function of the impedance of the forward path.

In this approach additional circuitry is placed between the PFD and CP with the primary objective of applying known control signals directly to the charge pump transistors. In the test the PLL feedback path is broken and control signals referenced to a common time base are applied to the charge pump control inputs. The oscillator frequency will be proportional to the voltage present at the loop filter node, which is in turn dependant upon the current applied from the charge pump. Thus if the output frequency can be determined information can be obtained about the forward path PLL blocks. The test proposal suggests that the loop divider is reconfigured as a frequency counter. The test basically comprises of three steps as follows. Initially closing both of the charge pump transistors performs a DC reference count, if the charge pump currents are matched the voltage of the loop filter node should be at approximately half the supply voltage. The measurement from this test phase is used as a datum for all subsequent measurements. In the second stage of the test the loop filter is discharged for a known time. Finally the loop filter is charged for a known time. For all of the test stages the output is measured using the oscillator and frequency counter and is stored in a digital format. In all of the tests the output response is compared against acceptable limits and pass or fail criteria are evaluated.

This BIST strategy covers most if not all analogue faults and can be extended to test the phase detector by increasing the complexity of the timing and control of the input vectors to the PLL.

Finally it should be noted that methods to measure jitter either directly or indirectly are currently being addressed. In [10] a method is proposed that has the additional advantage of utilizing minimal additional digital functions for implementation. To date however there are few other credible on-chip solutions. This is an important goal as frequencies continue to rise.

#### 4. SUMMARY AND CONCLUSIONS.

This chapter has summarized the types of PLL used within electronic systems, the primary function of the core blocks and key specifications. Typical test strategies and test parameters have been described and a number of design-for-testability and built-in-self-test solutions described.

It is clear that as circuit speeds increase and electronic systems rely more heavily on accurate and stable clock control and synchronization, the integrity and stability requirements for of PLL functions will become more aggressive increasing test time and test complexity. Methods of designing PLL's to be more accurately and more easily tested will hence become more important as the system-on-chip industry grows.

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