Chapter 7

TEST OF A/D CONVERTERS

From converter characteristics to built-in self-test proposals

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Abstract: Converter testing is a complex process. Test specifications are application dependent and in most cases require sophisticated stimulus generation and, response analysis equipment. The processing of sampled data to generate specification measurements also requires complex DSP algorithms. Furthermore, test complexity increases with speed, resolution and technology advances. This chapter summaries the key test specifications, conventional methods of verifying these specifications and potential built-in self-test solutions.

1. INTROCUTION

Analogue-to-digital (A/D) converters are one of the most frequently used mixed-signal functions creating an interface between sensing and actuation devices in the industrial control, transportation, consumer electronics and instrumentation industries and conversion of analogue voice and video data in the computing and communications communities. In control applications, the trend is towards medium speed (10-100 kHz) and high resolution (>16 bits) with test requirements focused towards linearity testing. In communications applications, trends are similar, however, dynamic performance tends to be critical, especially in voice processing applications. Consumer goods are another important application where high conversion speed (up to 100's of MHz) and low-medium resolution (8-12 bits) is the norm.

Of interest therefore for the test engineer is the optimization of test programs towards verification of the key application specifications. The problems include the range of specifications requiring verification and the very different implementations used (e.g. ΣΔ vers. flash). Today, most test

strategies are based on DSP testing where a known stimulus is injected into the device and its digital output processed using, for example, fast Fourier transform techniques to extract dynamic specifications, such as total harmonic distortion and inter-modulation distortion. The cost of implementing these measurements is becoming excessive. As an example, to measure signal-to-noise and distortion ratio of a converter with a 90 dB resolution will typically require around 8,000 samples which translates to around 0.1 to 0.2 seconds of test time when acquisition and processing tasks are taken into account. Total harmonic distortion measurements to an 80 dB resolution will require double this. Taking into account that in many cases these measurements must be carried out for two or more gain settings and possible input signal amplitudes, test time can rapidly grow to several seconds. These estimates should be considered in the context of total test time for a system-on-chip or mixed signal IC which ideally needs to be below a second. Note also that the converter will generally occupy only a small area of the device.

These issues illustrate the importance of utilizing the best possible methods available for converter testing. This chapter will present not only the conventional techniques for testing converters but a selection of new ideas and test implementations that target both test time reduction and the demand for high cost analogue test equipment.

2. A/D CONVERSION

The process of A/D conversion is a transformation of a continuous analog input waveform into a sequence of discrete digital words. An A/D converter usually requires a sample-and-hold operation at the front end of the signal path to ensure that the analog signal remains constant during the conversion process. The conversion process itself varies between different A/D converter architectures, that include serial, folding, ΣΔ and interpolating A/D converters [1, 2].

The converter's transfer characteristics are commonly represented by a staircase function. Figure 7-1 illustrates the transfer function of an ideal N-bit A/D converter, where N is the converter's resolution. This corresponds to the number of digitized bits. For linear converters the full-scale (FS) input range from V_{min} to V_{max} is segmented into 2^N equally sized bins (so called code bins) of nominal width Q, also frequently referred to as 1 LSB (least significant bit):

$$Q = \mathrm{FS} \big/ 2^N = \left(V_{\max} - V_{\min}\right) \big/ 2^N = 1\,\mathrm{LSB} \qquad (1)$$

The ideal code bin width Q, usually given in volts, may also be given as a percentage of the full-scale range. By standard convention, the first code bin starts at voltage V_{min} and is numbered 0, followed by the first code transition level *T[1]* to code bin 1, up the last code transition level $T[2^N\text{-}1]$ to the highest code bin $[2^N\text{-}1]$ which reaches the maximum converter input voltage V_{max} [3]. In the ideal case, all code bin centers fall onto a straight line with equidistant code transition levels, as illustrated in Figure 7-1. The analog equivalent of a digital A/D converter output code k corresponds to the location of the particular ideal code bin center V_k on the horizontal axis.

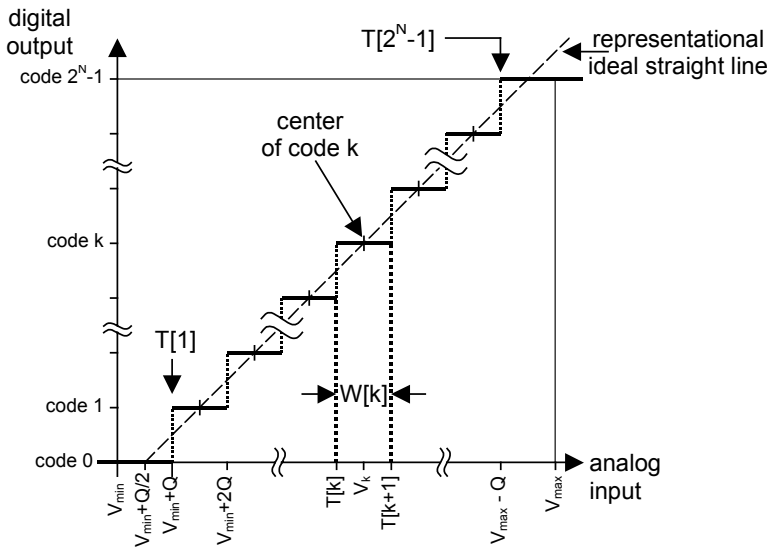

Figure 7-1. Ideal *N*-bit A/D converter transfer function

The quantization process itself introduces an error corresponding to the difference between the A/D converter's analog input and the equivalent analog value of its output, which is depicted over the full-scale range in Figure 7-2. With an rms value of $Q/\sqrt{(12)}$ for a uniform probability distribution between $Q/2$ and $-Q/2$ and an rms value of $FS/(2\sqrt{(2)})$ for a full-scale input sine wave, the ideal or theoretical signal-to-noise ratio (SNR) for an N-bit converter can be given in decibels as:

$$\mathrm{SNR}_{ideal}(\mathrm{dB}) = 10\log_{10}\left[\frac{\left(FS/2\sqrt{2}\right)^2}{\left(Q/\sqrt{12}\right)^2}\right] = 10\log_{10}\left[\left(2^N\sqrt{\frac{12}{8}}\right)^2\right] \quad (2)$$
$$= 20\log_{10}\left[2^N\right] + 20\log_{10}\left[\sqrt{\frac{12}{8}}\right] = 6.02N + 1.76$$

For real A/D converters, further errors affect the conversion accuracy and converter performance. The following sections will introduce the main static and dynamic performance parameters that are usually verified to meet the specifications in production testing. Standardized performance parameters associated with the A/D converter transient response and frequency response can be found in [3].

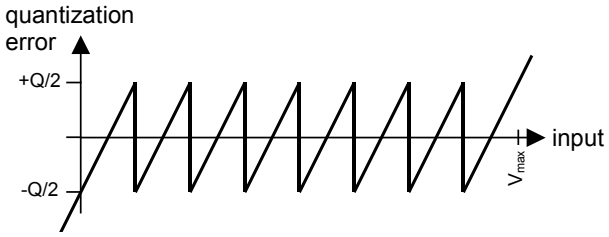

Figure 7-2. A/D conversion quantization error

2.1 Static A/D Converter Performance Parameters

Apart from the systematic quantization error due to finite converter resolution, A/D converters have further static errors mainly due to deviations in transition levels from the ideal case and are affected by internally and externally generated noise. One of the characteristic parameters which can indicate conversion errors is the real code widths. A particular code bin width, *W[k]*, can be determined from its adjacent code transition levels *T[k]* and *T[k+1]*, as indicated in Figure 7-1:

$$W[k] = T[k+1] - T[k] \qquad \text{for } 1 \le k \le 2^N - 2 \quad (3)$$

where code transition level *T[k]* corresponds to the analog input voltage where half the digital outputs are greater or equal to code *k* while the other half are below code *k*.

In addition to assessment of converter performance from transition levels and code bin widths, the real transfer function may also be approximated by a straight line for comparison with the ideal case. The straight line can be determined though a linear regression computation where the regions close to the upper and lower end of the transfer function are ignored to avoid data corruption due to overdriving the converter (input voltage exceeds the real full-scale range). The following main static performance parameters are introduced and described below: gain and offset, differential non-linearity and integral non-linearity.

The basic effect of *offset* in A/D converters is frequently described as a uniform lateral displacement of the transfer function, while a deviation from ideal *gain* corresponds to a difference in the transfer function's slope after offset compensation. With regard to performance verification and test, offset and gain can be defined as two parameters, V_{OS} and G, in a straight line fit for the real code transition levels, as given on the left hand side in equation (4) [3, 4]. The values for offset and gain can be determined through an optimization procedure aiming at minimum matching error $\varepsilon(k)$ between gain and offset adjusted real transition levels and the ideal values (right side of equation (4)).

$$G \times T[k] + V_{OS} + \varepsilon[k] = Q \times (k-1) + T[1]_{ideal} \text{ for } 1 \le k \le 2^N - 1 \quad (4)$$

where G is the gain, V_{OS} the offset, Q the ideal code bin width, $T[1]_{ideal}$ the ideal first transition level, and $T[k]$ the real transition level between codes k and k-1. The value for V_{OS} corresponds to the analogue equivalent of the offset effect observed at the output.

However, different optimization techniques yield slightly different values for offset, gain and the remaining matching error. For example the matching may be achieved through mean squared value minimization for $\varepsilon(k)$ for all k [3], alternatively, the maximum of the matching errors may be reduced. Simpler offset and gain measurements are often based on targeting an exact match in equation (4) for the first and last code transition levels, $T[1]$ and $T[2^N-1]$ ($\varepsilon(1)$ and $\varepsilon(2^N-1)$ equal to zero) referred to as *terminal based* offset and gain. An example for this case is illustrated in Figure 7-3. An alternative methodology is to employ the straight line approximation of the real transfer function mentioned above. Offset and gain values are then determined through matching this real straight line with the ideal straight line, which again can deviate slightly from the optimization process results [3].

Differential nonlinearity (DNL) is a measure of the deviation of the gain and offset corrected real code widths from the ideal value. DNL values are given in LSBs for the codes 1 to (2^N-2) as a function of k as:

$$\mathrm{DNL}[k](\mathrm{LSB}) = \frac{(W[k]-Q)}{Q} \qquad \text{for } 1 \le k \le 2^N - 2 \quad (5)$$

where *W[k]* is the width of code *k* determined from the gain and offset corrected code transition levels as given in equation (3), and *Q* the ideal code bin width. Note that neither the real code bin widths nor the ideal value are defined at either end of the transfer function. As an example, a differential nonlinearity of approximately +¼ LSB in code *m* is included Figure 7-3. The *absolute* or *maximum DNL* corresponds to the maximum value of |DNL[*k*]| over the range of *k* given in equation (5). A value of -1 for DNL[*k*] corresponds to a *missing code*.

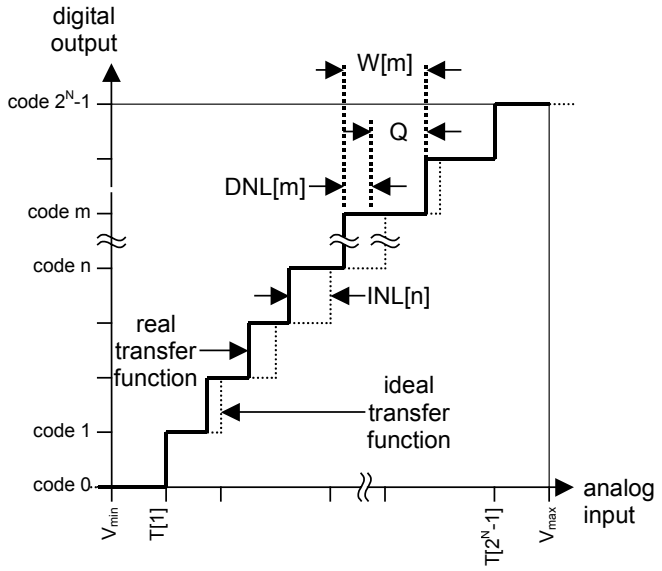

Figure 7-3. Terminal-based DNL and INL in A/D converter transfer function

Integral nonlinearity (INL) quantifies the absolute deviation of a gain and offset compensated transfer curve from the ideal case. INL values are given in LSBs at the code transition levels as a function of *k*:

$$\mathrm{INL}[k](\mathrm{LSB}) = \frac{\varepsilon[k]}{Q} \qquad \text{for } 1 \le k \le 2^N - 2 \quad (6)$$

where *ε(k)* is the matching error from equation (4) and *Q* the ideal code bin width, both given in volts. Alternatively, INL[*k*] values can also be given as a percentage of the full-scale input range. As an example, Figure 7-3 also

depicts a integral nonlinearity of approximately +⅔ LSB in code *n*. Plots of INL[*k*] values over *k* provide useful information on the converter performance, as the overall shape of the INL[*k*] curve enables some initial conclusions on the predominance of even- or odd-order harmonics [5]. However, the exact values for the INL do depend on the type of gain and offset correction methodology applied, which should be documented. The *absolute* or *maximum INL*, usually provided as an A/D converter specification, corresponds to the maximum value of |INL[*k*]| over the range of *k* given in equation (6).

Some additional performance characteristics are defined for A/D converters. An A/D converter is said to be *monotonic*, if the output is either consistently increasing or decreasing with an either consistently increasing or decreasing input. If the change at input and output are of the same direction, the converter is *non-inverting*. When the change at the input and output are of opposite direction, the converter is *inverting*. An A/D converter can also be affected by *hysteresis*. This is a condition where the computation of the transfer function yields different results for an increasing and a decreasing input stimulus that are beyond normal measurement uncertainties. For more details see [3].

2.2 Dynamic A/D Converter Performance Parameters

A/D converter performance is also expressed in the frequency domain. This section introduces the main dynamic performance parameters associated with the converter's output spectrum, while the determination of their values in converter testing described in section 3.4.

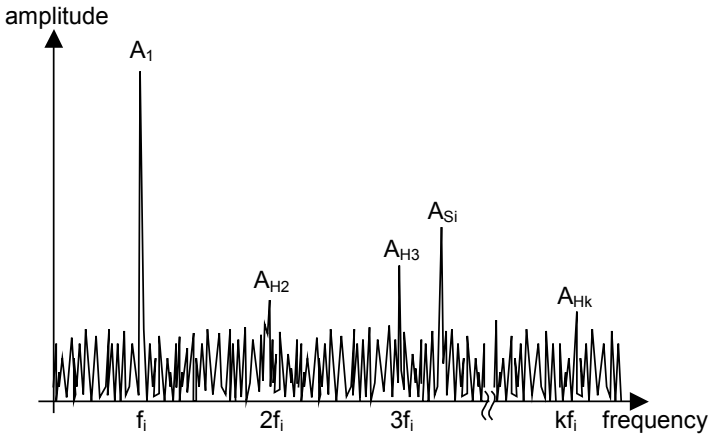

Figure 7-4. A/D converter output spectrum

Figure 7-4 illustrates an A/D converter output spectrum, a plot of frequency component magnitude over a range of frequency bins. Such a spectrum can be obtained from a spectrum analyzer or a discrete Fourier transform (DFT) [6] through analysis of the A/D converter response to a spectrally pure sine wave input of frequency f_i. The original input signal can be identified as the fundamental of amplitude A_1. The second to k^{th} harmonic distortion component, A_{H2} to A_{Hk}, occur at non-aliased frequencies that are integer multiples of f_i. Additionally, non-harmonic or spurious components, such as A_{Si} in Figure 7-4, can be seen at other than the input signal or harmonics frequencies. The main dynamic performance parameters given below can be extracted from the output spectrum in the form of ratios of rms amplitudes of particular spectral components, which also relates to signal power ratios. The calculation of these from the results of a DFT is outlined in section 3.4.1. Note that the input signal frequency and amplitude, and in some cases the sampling frequency, have an impact on the actual performance parameter value, and have to be provided with test results and performance specifications.

The *signal-to-noise and distortion ratio* (SINAD) relates the input signal to the noise including harmonics. The SINAD can be determined from rms values for the input signal and the total noise (including harmonics), which also relates to the power, P, carried in the corresponding signal component. The SINAD is given in decibels as:

$$\mathrm{SINAD(dB)} = 20\log_{10}\left[\frac{\mathrm{rms}\left(signal\right)}{\mathrm{rms}\left(totalnoise\right)}\right] = 10\log_{10}\left[\frac{P_{signal}}{P_{totalnoise}}\right] \quad (7)$$

The *effective number of bits* (ENOB) compares the performance of a real A/D converter to the ideal case with regard to noise [7]. The ENOB is determined through:

$$\mathrm{ENOB} = N - \log_2\left[\frac{\mathrm{rms}\left(totalnoise\right)}{\mathrm{rms}\left(idealnoise\right)}\right] \quad (8)$$

where N is the number of bits of the real converter. In other words, an ideal A/D converter with a resolution equal to the ENOB determined for a real A/D converter will have the same rms noise level for the specified input signal amplitude and frequency. The ENOB and SINAD performance parameters can be correlated to each other as analyzed in [3].

Total harmonic distortion (THD) is a measure of the total output signal power contained in the second to k^{th} harmonic component, where k is usually in the range from 5 to 10 (depending on the ratio of the particular harmonic

distortion power to the random noise power) [8]. The THD can be determined from rms values of the input signal and the harmonic components and is commonly expressed as the ratio of the powers in decibels:

$$\mathrm{THD(dB)} = 20\log_{10}\left[\sqrt{\sum_{i=2}^{k} A_{Hi(rms)}^2} \Big/ A_{1(rms)}\right] = 10\log_{10}\left[\frac{P_{harmonic}}{P_{input}}\right] \quad (9)$$

where $A_{1(rms)}$ is the rms for the signal and $A_{Hi(rms)}$ the rms for the i^{th} harmonic. THD is given in decibels and usually with respect to a full-scale input (dBFS). Where the THD is given in dBc, the unit is in decibels with respect to a carrier signal of specified amplitude.

The *spurious free dynamic range* (SFDR) quantifies the available dynamic range as a ratio of the fundamentals amplitude to the amplitude of the largest harmonic or spurious component and is given in decibels:

$$\mathrm{SFDR(dB)} = 20\log_{10}\left[\frac{A_1}{\max\{A_{H(\max)}, A_{S(\max)}\}}\right] \quad (10)$$

where $A_{H(max)}$ and $A_{S(max)}$ are the amplitudes of the largest harmonic component and spurious component, respectively.

While the dynamic performance parameters introduced above are essential for an understanding of A/D converter test methodologies (section 3), an entire range of further performance parameters is included in the IEEE standard 1241 [3], such as various signal-to-noise ratios specified for particular bandwidths or for particular noise components. Furthermore, some performance parameters are defined to assess intermodulation distortion in A/D converters with a two-tone or multiple-tone sine wave input.

3. A/D CONVERTER TEST APPROACHES

This section introduces A/D converter test methodologies, for static and dynamic performance parameter testing. The basic test setup and other prerequisites are briefly described in the next section. For further reference, an introduction to production test of integrated circuits, ranging from test methodologies and design-for-test basics to aspects relating to automatic test equipment can be found in [9]. Details on DSP-based testing of analog and mixed-signal circuits are provided in [10, 11].

3.1 Setup for A/D Converter Test

The generic test setup is illustrated in Figure 7-5. In generic terms, a suitable stimulus supplied by a test source is applied to the A/D converter under test via some type of test access mechanism. The test stimulus generator block corresponds to one or more sine wave, arbitrary waveform or pulse generator(s) depending on the type of test to be executed. Generally, the response is captured for processing in a test sink again facilitating a test access mechanism.

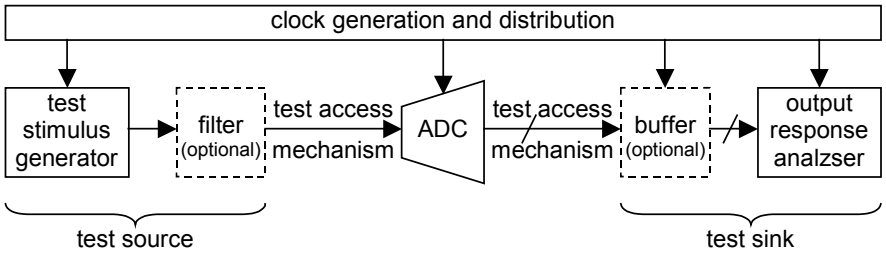

Figure 7-5. A/D converter test setup

In a conventional A/D converter test setup, test source and test sink are part of the external automatic test equipment (ATE) and are centrally controlled. The ATE interfaces with the IC via a device interface board; functional IC input/output pins and IC-internal interconnects may be facilitated as a test access mechanism. However, in the majority of cases some other means of test access has to be incorporated in the early stages of IC design due to access restrictions, such as limited pin count or converters being deeply embedded in a complex system-on-chip (SOC). Systematic design methodologies which increase test access, referred to as design-for-testability (DfT), are standardized at various system levels. The IEEE standard 1149.1, also known as boundary scan, supports digital IC and board level tests [12]. Its extension to analog and mixed-signal systems, IEEE standard 1149.4, adds an analog test bus to increase access to analog IC pins and internal nodes [13]. For SOC implementations, an IEEE standard for interfacing to IC-internal subsystems, so-called embedded cores, and documentation of their test requirements is expected to be approved in the near future [14].

3.2 Capturing the Test Response

The action of collecting a set of A/D converter output samples and transferring it to the output response analyzer is commonly referred to as

taking a data record. The aim is to accumulate consecutive samples, however, for high-speed converters interfacing restrictions may require output decimation [3]. This is a process in which only every i^{th} sample of a consecutive sequence is recorded at a lower speed than the A/D converter's sampling speed.

On the other hand, the A/D converter maximum sampling frequency restricts the rate at which a waveform can be digitized and therefore the measurement bandwidth. When sampling periodic waveforms, it is generally desirable to record an integer number of waveform periods while not re-sampling identical points at different cycles. This can be assured by applying coherent sampling, equation (11), where additionally the number of samples in the record, M, and the number of cycles, N, are in the ratio of relative prime numbers [10].

$$f_i = f_s * N/M \tag{11}$$

Where f_s is the sampling frequency and f_i the input waveform frequency.

With such a sampling scheme it is possible to systematically rearrange consecutive samples taken over multiple periods to an equivalent data record for a single period taken at higher speed. This technique is called *equivalent time sampling* or time shuffling and is illustrated in the Figure 7-6.

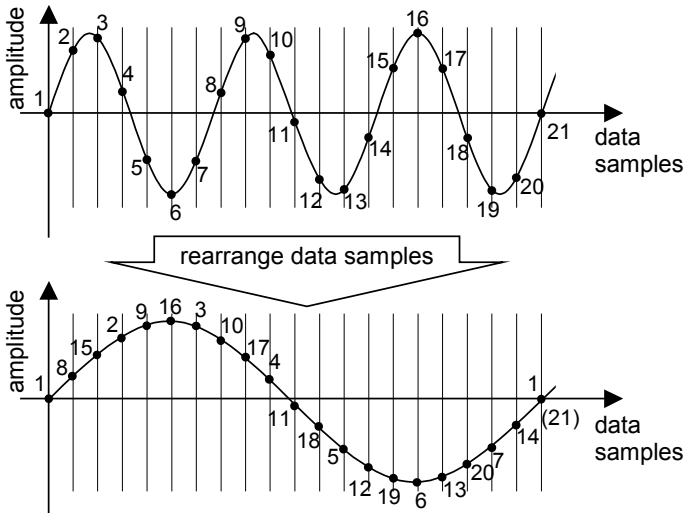

Figure 7-6. Equivalent time sampling

Similarly it is possible to employ output decimation to achieve two special cases of coherent sampling. Firstly, in *beat frequency testing*, with

N=M+1 in equation (11), the difference between sampling and input signal frequency is very small. Rearranging of samples is not required in the data record where successive samples step slowly through the periodic waveform as illustrated in Figure 7-7a. Secondly, in *envelope testing*, where N=1+M/2 and M is a multiple of 4, the sampling frequency is nearly twice the input frequency stepping sequentially through both halves of the input waveform phases as illustrated in Figure 7-7b.While the latter sampling schemes allow a quick visualization of the waveforms shape, the sampling techniques introduced can be employed in the test methodologies described in the next sections.

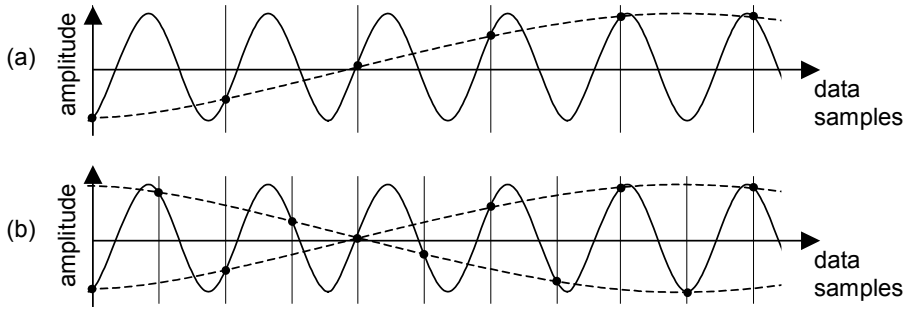

Figure 7-7. (a) Beat frequency testing and (b) envelope testing

3.3 Static Performance Parameter Test

A/D converter performance can be verified in terms of static performance parameters, introduced in section 2.1, through assessment of the transfer function. One way to compute the transfer function is to apply a DC voltage to the A/D converter that is stepping through an analog voltage range slightly larger than the full-scale input range. For each step a number of data pairs (input voltage / output code) have to be computed. The transfer function can then be approximated as the curve of the mean output code over corresponding input voltage. The input voltage step size and the number of output codes averaged for each input voltage step depends on the ideal code bin width, the level of random noise and the required measurement accuracy, which can be assessed through computation of the standard deviation of the output.

In static performance production test, however, the use of continuous signals is more desirable. The following sections introduce two A/D converter test methodologies widely in use today which measure code transition levels, namely feedback-loop testing and histogram testing [3, 10,

11, 15]. From those values, static performance parameters are determined as described in section 2.1 which can then be compared to the test thresholds.

3.3.1 Feedback-loop Test Methodology

In 1975 Corcoran et al. published a test methodology for A/D converters that incorporates a feedback loop to force the A/D converter input voltage to oscillate around a desired code transition level [16]. On the test source side, an analog integrator is employed which continuously integrates either a positive or a negative reference voltage, V_{ref+} and V_{ref-}, for stimulus generation (Figure 7-8a). The reference voltage to integrate is toggled depending on a comparison result between the A/D converter's output code, C, and a set desired output code, D, after each conversion. If $C < D$, the positive reference voltage is connected to the analogue integrator to set a positive slope in the test stimulus. If $C > D$, the negative reference voltage is chosen to obtain a negative slope in the test stimulus. Once the input stimulus has reached the desired code transition level $T[D]$, the feedback from the digital comparator enforces oscillation around $T[D]$ at the converter input. Measuring the average voltage at the A/D converter input yields the value of the particular code transition level.

Several further adaptations of this technique, also referred to as servo testing, have been described in literature and were also included in IEEE standards [3, 17]. For example, the test source can be based on D/A conversion of a counter output, as illustrated in Figure 7-8b, where the D/A converter resolution is larger than the A/D converter resolution. Instead of toggling an analog reference voltage, the content of the counter can be incremented or decremented to obtain a positive or negative slope in the test stimulus. Alternatively, an accumulator may be chosen instead of a counter which allows increasing or decreasing the D/A converter input by an adjustable amount [18]. In either case, additional low-pass filtering may be incorporated to increase the effective test stimulus resolution. The test evaluation may be performed by measuring the average A/D converter input voltage, as above, or by extrapolating that voltage from the average D/A converter input through digital processing.

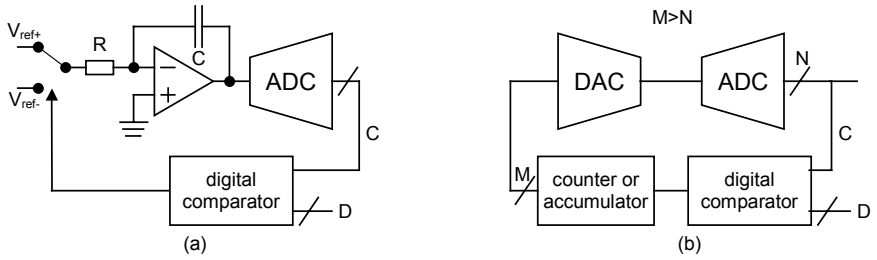

Figure 7-8. Feedback-loop configurations, (a) integrator (b) D/A conversion

The test can be automated easily. Starting at the first code transition level with $D = 1$, the desired output code D is sequentially incremented each time the average A/D converter input corresponding to *T[D]* has been determined. The loop is continued until the last transition level with $D = 2^N-1$ is computed. If test time restrictions prevent measurement of all transition levels, a basic linearity test may be performed for code words formed by a set number of most significant bits while DNL testing is only applied to a limited number of codes [19].

In feedback-loop A/D converter testing, stimulus accuracy is crucial; the positive and negative slope rates must especially be equal, as any mismatch directly affects the ratio of code occurrences at either side of the code transition level. Also, the effect of test stimulus slope (and step size in D/A conversion) on the dynamics of the feedback loop must be analyzed in more detail [5, 15, 18]. Regarding test application time, the number of conversions required to reach a particular code transition level and to settle the feedback loop has to be assessed. This is especially true for high-speed A/D converters, where the conversion delay may be smaller than the delay through the feedback loop. Stable oscillation around a code transition level may not be achievable in this case.

3.3.2 Histogram Test Methodology

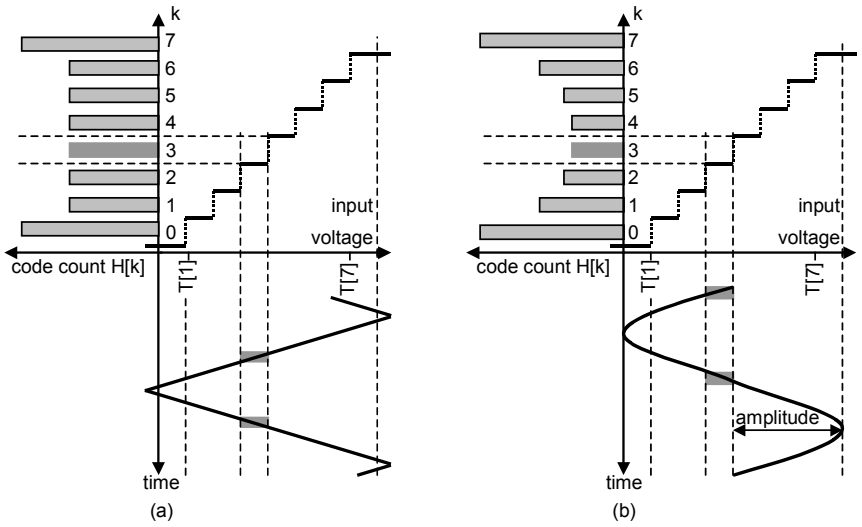

Figure 7-9. Histogram generation (a) linear (b) sine wave

In histogram testing, A/D converter code transition levels are not measured directly but determined through statistical analysis of converter activity [20]. For a known periodic input stimulus, the histogram of code occurrences (code counts) is computed over an integer number of input waveform periods. There are two types of histograms employing test stimuli of different characteristic [21]. Firstly, there is the *ramp histogram*, also called linear histogram, computed for a linear - typically triangular – waveform. Secondly, the *sine wave histogram*, frequently referred to as dynamic histogram, is collected for a sinusoidal input waveform. The computation is illustrated for both types for an ideal 3-bit converter in Figure 7-9. Note that in the illustration the triangular waveform overdrives the A/D converter causing higher code counts in *H[0]* and *H[7]*, while the sinusoidal wave only touches the boundaries of the full-scale range.

Generally, histograms support analysis of the converter's static performance parameters. A missing code *m* is easily identified as the corresponding code count *H[m]* is equal to zero. Also offset is easily identified as a shift in the code counts and gain directly relates to average code count. However, the converter linearity is assessed via the determination of code transition levels.

For ramp histograms, where ideal values for *H[2]* to $H[2^N-2]$ are equal, code transition levels can be given as in the first part of equation (12), where *C* is an offset component and *A* a gain factor which is multiplied with the

accumulated code count up to the transition to code k [3]. As the widths of the extreme codes, 0 and 2^N-1, cannot be defined, their code counts are usually set to zero ($H[0] = H[2^N-1] = 0$). In these cases, C and A can be determined as shown in equation (12), where the first code transition level, $T[1]$, is interpreted as the offset component. The gain factor defines the proportion of the full-scale input range for a single sample in the histogram, where H_{tot} is the total number of samples in the entire histogram.

$$T[k] = C + A\sum_{i=0}^{k-1} H[i] = T[1] + \frac{T[2^N - 1] - T[1]}{H_{tot}} \sum_{i=0}^{k-1} H[i] \tag{12}$$

For sine wave histograms, code transition levels have to be computed differently as ideal values for $H[2]$ to $H[2^N-2]$ are not equal [22]. With a stimulus $v[t] = A*\sin[\omega t+\phi]+C$, the transition levels can be given as [3, 4]:

$$T[k] = C - A\cos\left[\left(\pi\sum_{i=0}^{k-1} H[i]\right) \Big/ H_{tot}\right] \tag{13}$$

where offset component C and gain factor G correspond to the input sine wave's offset and amplitude.

For either type of histogram, high stimulus accuracy is essential as most deviations (ramp linearity, sine wave distortion) have a direct impact on the test result. For high frequency stimuli, tests may also detect dynamic converter failure. The choice of sine wave histograms can be advantageous, as stimulus verification and high frequency signal generation are easier to achieve [11]. An advantage of ramp histograms is that generally a lower number of samples is required due to constant ideal code counts. The number of code counts is an important test parameter, as it is directly proportional to test application time and depends on required test accuracy and confidence level. In [23] an equation is derived for the number of samples required for random sampling of a full-scale sine wave histogram. This number can be reduced through controlled sampling and overdriving of the converter; a relationship is derived in [4].

A shortcoming of histogram testing in general is the loss of information associated with the accumulation of code counts only and not their order of occurrence. Imagine a situation where code bins were swapped, leading to a non-monotonic transfer function. There will be no effect on a ramp histogram and detection for a sine wave histogram depends on the code locations. A more realistic converter failure escaping histogram testing, is the occurrence of code sparkles. Usually this is a dynamic effect where an output code of unexpected difference to its neighbors occurs. However, such

effects can become detectable via accumulation of each code's indices (locations) in a so-called *weight* array, which can be computed in addition to the histogram accumulated in a *tally* array [10].

3.4 Dynamic Performance Parameter Test

Generally, the aim in dynamic performance parameter testing is to identify the signal's components at the A/D converter output, such as the converted input signal, harmonics, and random noise, and to compute performance parameters introduced in section 2.2. For the majority of these parameters and determination of signal components, a transformation from time domain to frequency domain is required. A/D converter testing employing discrete Fourier transformation is described in the next section. However, some dynamic performance parameters can also be determined in the time domain from an A/D converter model generated to match a data record taken from a real converter. So-called sine-fit testing is introduced in section 3.4.2. For either technique, it is assumed that a single tone sine wave stimulus is applied to the A/D converter.

3.4.1 Frequency Domain Test Methodology

This section focuses on the application of frequency domain test to A/D converters. It is beyond the scope of this chapter to provide an introduction to Fourier transformation [6] or to discuss general aspects of DSP-based testing and spectrum analysis [10, 11] in great detail.

A signal can be described in time or frequency domain where the Fourier analysis is employed to move from one domain to the other without loss of information. For coherent sampling of periodic signals with the number of samples taken in the time domain being a power of two, the discrete Fourier transformation can be computed more efficiently through fast Fourier transformation (FFT) algorithms. If coherent sampling of all signal components cannot be guaranteed, a periodic repetition of the sampled waveform section can lead to discontinuities at either end of the sampling interval causing spectral leakage. In such cases windowing has to be applied, a processing step in which the sampled waveform section is mathematically manipulated to converge to zero amplitude towards the interval boundaries, effectively removing discontinuities [24]. In either case, the A/D converter output signal is decomposed into its individual frequency components for performance analysis. The frequency range covered by the spectrum analysis depends on the rate of A/C converter output code sampling, f_s. The number of discrete frequency points, also referred to as frequency bins, is determined by the number of samples, N, processed in the FFT. While accounting for

aliasing, signal and sampling frequencies have to be chosen to allow sufficient spacing between the harmonics and the fundamental component. The graphical presentation of the spectrum obtained from the analysis, frequently referred to as FFT plot, illustrates the particular signal component amplitude with its frequency on the x-axis (Figure 7-10). The number of frequency bins is equal to $N/2$ and their widths are equal to f_s/N.

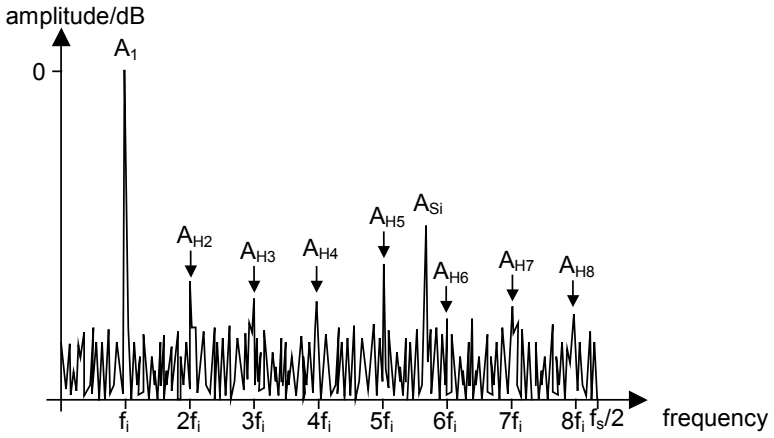

Figure 7-10. A/D converter output spectrum

The following spectrum features can be identified in Figure 7-10: Firstly the fundamental component, A_1, corresponding to the input signal, secondly the harmonic distortion components, A_{H2} to A_{H8}, thirdly large spurious components, such as A_{Si}, and finally the remaining noise floor representing quantization and random noise. Dynamic performance parameters, such as SINAD, THD and SFDR, can be calculated from the particular signal components' real amplitudes (not in decibels) or the power contained in them, as given in section 2.2 and described in [25] including multi-tone testing.

3.4.2 Sine Wave Fitting Test Methodology

Fitting a sine wave function to the data recorded when a sinusoidal stimulus is applied to the A/D converter allows assessment of the general performance. In [3], sampling of at least five stimulus cycles is quoted as a rule of thumb, where it also has to be born mind that conversion errors may be concealed with increasing record size due to averaging effects. Again, sampling and input stimulus frequency should be selected to record data that is uniformly spaced over a single period of the waveform. However, sampling of a non-integer number of cycles does not cause problems which

have been mentioned for spectrum analysis above. In any case, the mathematical model of the fitted sine wave relates to the data y_n sampled at time instants t_n as:

$$y_n = A\cos(\omega t_n + \theta) + C \qquad \text{for } n = 1,\ldots,M \tag{14}$$

where A is the amplitude, θ the phase and C the offset of the fitted sine wave of angular frequency ω. When the frequencies of the input stimulus and the sampling and therefore parameter ω of the fitted function are known, the remaining three sine wave parameters can be calculated through minimization of the rms error between the data record and the model (*three-parameter least square fit*, [3]). When the frequencies are unknown or not stable, then the *four-parameter least square fit* has to be employed. Here, an iteration process beginning with an initial estimate for the angular frequency surrounds the least square minimization process. The value for ω is updated between loops until the change in obtained sine wave parameters remains small. The three parameter and four parameter fitting process is derived and described in far more detail in [17].

The performance parameter that is usually computed for the fitted A/D converter model is the ENOB [7], equation (8). Some further performance analysis can be achieved by test execution under different conditions, such as various input stimulus amplitudes or frequencies as described in [26]. A potential problem is that this test methodology does not verify the converter performance over its entire full-scale input range, as the test stimulus amplitude has to be chosen to avoid clipping. Localized conversion error, affecting a very small section of the transfer function, may also escape unnoticed due to the averaging effect of the fitting process.

4. A/D CONVERTER BUILT-IN SELF-TEST

Built-in self-test (BIST) for analogue and mixed signal components has been identified as one of the major requirements for future economic deep sub-micron IC test [27, 28]. The main advantage of BIST is to reduce test access requirements. At the same time the growing performance gap between the circuit under test and the external tester is addressed by the migration of tester functions onto the chip. In addition, parasitics induced from the external tester and the demands on the tester can be reduced. Finally, analogue BIST is expected to eventually enable the use of cheaper, digital only or so-called DfT-testers that will help with the integration of analogue virtual components - including BIST - for digital SOC applications. Here the aim is to enable the SOC integrator to avoid the use of expensive

mixed signal test equipment. Also, for multi-chip modules, on-chip test support hardware helps to migrate the test of analogue circuitry to the wafer level. It is expected that the re-use of BIST structures will significantly reduce escalating test generation costs, test time and time-to-market for a range of devices. Full BIST has to include circuitry to implement both test stimulus generator (TSG) and output response analyzer (ORA). This section briefly summarizes BIST solutions that have been proposed for performance parameter testing of A/D converters, some of which have been commercialized.

Most BIST approaches for A/D converter testing aim to implement one of the converter testing techniques described in section 3. In [29] it is proposed to accumulate a converter histogram in an on-chip RAM while the test stimulus is generated externally. The accumulated code counts can be compared against test thresholds on-chip to test for DNL; further test analysis has to be performed off-chip. This test solution can be extended towards a full BIST by including an on-chip triangular waveform generator [30]. In a similar approach, the histogram-based analog BIST (HABIST™), additional memory and ORA circuitry can be integrated to store a reference histogram on-chip for more complete static performance parameter testing of A/D converters [31]. This commercialized approach [32] also allows the use of the tested A/D converter with the BIST circuitry to apply histogram-based testing to other analogue blocks included in the same IC. As illustrated in Figure 7-11, the on-chip integration of a sine wave or saw tooth TSG is optional. The histogram is accumulated in a RAM where the converter output provides the address and a read-modify-write cycle updates the corresponding code count. The response analysis is performed after test data accumulation and subtraction of a golden reference histogram. As for the TSG, on-chip implementation of the full ORA is optional.

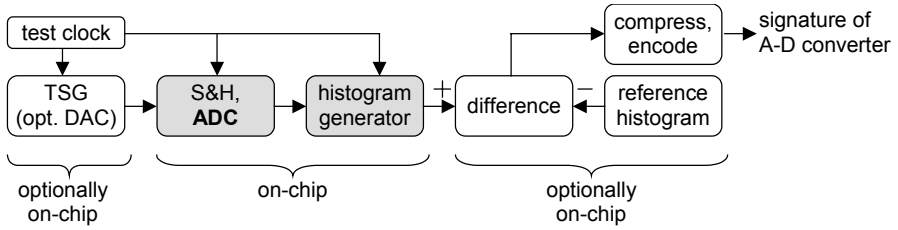

Figure 7-11. HABIST™ scheme applied to A/D converter (ADC)

Also the feedback-loop test methodology has been considered for a straightforward BIST implementation [33]. The oscillating input signal is generated through the charging or discharging of a capacitor with a positive or a negative reference current *I*, generated on-chip (Figure 7-12). Testing

for differential and integral nonlinearity is based on the measurement of the oscillation frequency on the switch control line (*ctrl*) similarly to feedback-loop testing (section 3.3.1).

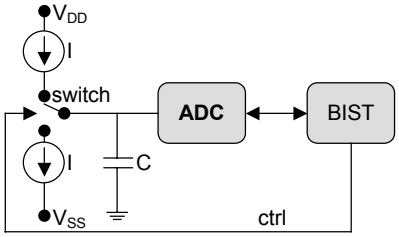

Figure 7-12. Oscillation BIST applied to A/D converter (ADC)

The dynamic performance of an A/D converter can be assessed through spectrum analysis or sine wave curve fitting as described above. It has been proposed to add an on-chip TSG and to facilitate an available DSP core to implement a BIST scheme for either of these test techniques [34]. Similarly, a BIST approach for mixed signal ICs containing a DSP, memory, and both, A/D and D/A converters has been proposed which computes an FFT and evaluates test results on-chip [35].

A BIST scheme to test an A/D-D/A converter chain for dynamic performance without the availability of a DSP is proposed in [36]. For high resolution A/D converter testing, the response analysis is conducted by integrating evenly distributed $n/4$ samples for each quarter of a ramp response (S_0 to S_4 in Figure 7-13a/b). The coefficients of a fitted third order polynomial can be calculated from these four sums and relate to DC offset and gain, and 2^{nd} and 3^{rd} order harmonic distortion expected for a sine wave input. While the integration is conducted by BIST circuitry, the on-chip extraction of coefficients, performance parameters and the comparison to test thresholds is optional. The expected ramp input stimulus can be approximated by a low pass filtered four-segment staircase-like stimulus, as illustrated in Figure 7-13c [37]. The BIST circuitry generates a pulse-width modulated waveform with five different duty cycles. These are applied to an off-chip low pass filter in turn to generate a rising and a falling step for each quarter of the converter's input range. The integration process is conducted during the rising / falling edges of the exponential (approximately 17% of the step width, as illustrated by shaded regions in Figure 7-13c) to achieve a relatively linear output code distribution.

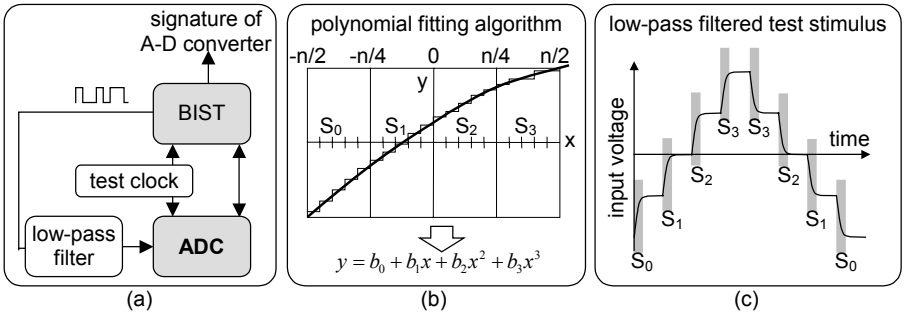

Figure 7-13. A/D converter BIST employing polynomial fitting algorithm

While the advantages of analog and mixed-signal BIST solutions are clear, drawbacks due to limited test sets, excessive area overhead or a low confidence in test results have hampered wide industrial use. BIST techniques summarized above are mostly limited to particular A/D converter architectures. Histogram-based BIST, for example, may result in excessive area overhead for high-resolution converters. The polynomial fitting algorithm BIST scheme is aimed at high-resolution converter testing, but relies on the assumption that a third order polynomial accurately fits the test response.

More work may be required to identify converter performance parameters crucial for testing. Test requirements and realistic failure modes will depend on particular converter architectures. An example study can be found in [38].

5. SUMMARY AND CONCLUSIONS

This chapter has discussed the key parameters and specifications normally targeted in A/D converter testing, methods for extracting these performance parameters and potential solutions for either implementing full self-test or migrating test resources from external test equipment to the device under test. Table 1 provides a summary of the advantages and limitations of five of the main test methods used in A/D converter testing.

Table 7-1. Summary of A/D converter test approaches

Technique	Performance parameters tested	Major advantages	Main limitations
Histogram-based	Static performance (offset and gain error, DNL, INL, missing codes, etc.)	Well-established, Complete linearity test	Long test time, amount of data, No test for dynamic performance, Test stimulus accuracy
Servo-loop	Static performance (offset and gain error, DNL, INL)	Accurate measurement of transition edges (not based on statistics)	Test stimulus accuracy Measurement accuracy
Sine-wave curve-fitting	DNL, INL, missing codes, aperture uncertainty, noise	Tests for dynamic performance	Input frequency is a sub multiple of sample frequency, Lack of convergence of algorithm, Measurement accuracy
Beat frequency testing	Dynamic characteristic	Quick and simple visual demonstration of ADC failures	No accurate test
FFT-based	Dynamic performance (THD, SINAD, SNR, ENOB)	Tests for dynamic performance, Well-established	No tests for linearity

The field now faces major new challenges, as the demand for higher resolution devices becomes the norm. The concept of design reuse in the form of integrating third party designs is also having a major impact on the test requirements as in many cases system integrators wishing to utilize a high performance converter functions will not normally have the engineering or production test equipment required to test these devices. The concept of being able to supply an A/D converter with an embedded test solution that requires only digital external test equipment is hence a major goal.

In the case of on-chip test solutions proposed or available commercially, limitations need to be understood before investing design effort. Histogram testing, for example, will require a large amount of data to be stored and evaluated on-chip while requiring long test times. For servo-loop based solutions, the oscillation around a single transition level may be difficult to achieve under realistic noise levels. Sine-wave fitting will require some significant area overhead for the on-chip computation, as do FFT-based solutions, and may still not achieve satisfying measurement accuracy and resolution. Further work is therefore required to quantify test times, associated cost and measurement accuracies and generate quality test quality metrics.

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