The Application of neuMOS Transistors to Enhanced Built-in Self-Test (BIST) and Product Quality

R. Nicholson, A. Richardson
Faculty of Applied Sciences, Lancaster University, Lancaster, LA1 4YR, UK.

Abstract

The neuMOS transistor is a comparatively new device developed in 1991 at Tohoku University, Japan, which is currently showing great promise in the direction of enhanced circuit functionality, particularly in Neural Network applications. In this paper we examine the possibilities of applying the inherent enhanced functionality of the neuMOS transistor to analogue and digital BIST. A novel concept is introduced which can extend existing sw-opamp structures. Finally, potential outgoing quality enhancement in VLSI neuMOS circuits over the CMOS equivalents are considered.

1 Introduction

NeuMOS transistors are an enhanced transistor configuration developed at Tohoku University in 1991 [1]. The device has a structure based on EEPROM or EPROM, utilising a floating gate above the standard MOS channel to which any number of control gates are capacitivly coupled. The drain-source current is controlled by the linear weighted sum of the voltages applied to each of the input gates, which provides functionality not dissimilar to that of a biological neurone – hence the name of the device and its inherent suitability to neural network applications [2, 3, 4].

However, the enhanced functionality of these devices has been shown to yield considerable area and power advantages over standard MOS circuits in VLSI design [5, 6, 7, 8, 9, 10, 11]. There is also an inherent suitability to multi-valued logic architectures [12, 13, 14, 15, 16, 17, 18]. These characteristics make neuMOS transistors a very attractive alternative to simply reducing MOS feature size and packing density in the quest to achieve 'intelligent' processing on integrated circuits [16].

When applied to analogue designs, the neuMOS transistor has several properties which open new possibilities in low voltage operation (by realising effective threshold voltages of zero) [19, 20], precision matching [21, 22], current mode designs [23], and enhanced/simplified designs [24].

In section 2 of this paper, the neuMOS transistor is described in more detail. Section 3 will present a novel concept used to extend existing sw-opamp structures. Section 4 presents some thoughts on enhanced quality of neuMOS circuits.

2 The neuMOS transistor

Figures 1 to 3 show the layout of the device, in a standard double poly CMOS process, the equivalent circuit of the device and the circuit symbol. Note that the device can be manufactured in a single poly process utilising a metal layer for the input gates, however this can often lead to large aspect ratios [7].

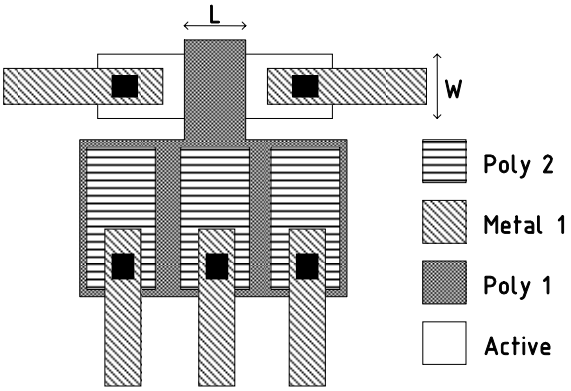

Figure 1: neuMOS layout

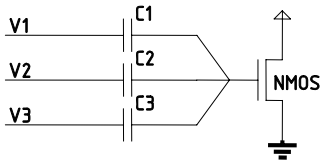

Figure 2: Equivalent Circuit

In this device, the source to drain current is controlled by the potential on the floating gate, which in turn is governed by the voltages on the control gates combined by their relative weightings according to:

$$\phi_F = \frac{C_1V_1 + C_2V_2 + ... + C_nV_n}{C_1 + C_2 + ... + C_n + C_o}$$

Where C_o is the capacitance between the floating gate and channel.

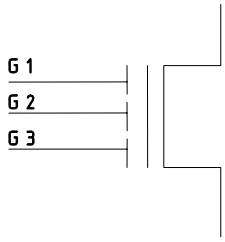

Figure 3: neuMOS circuit symbol

Detailed models have been derived for operation both above-threshold [1] and subthreshold [21, 22, 23]. For the qualitative analysis presented in this paper these are not required for understanding.

Three important points should be noted with regard to the use of neuMOS transistors:

- The devices must be 'UV erased' after manufacture in order to remove any residual charge created in the floating gate during production.
- There is a dependence between the drain source current and the drain voltage of the device which is more pronounced than in a standard MOSFET. This can be minimised be either careful selection of aspect ratios or use of cascode devices (in structures such as current mirrors, differential pairs etc.)
- A standard building block of binary/multi-valued neuMOS circuits is the neuMOS inverter (figure 4) [1]. This structure can consume static power (depending on the state of the inputs), care must be taken to avoid/prevent this if Iddx testing is to be implemented on any part of the IC.

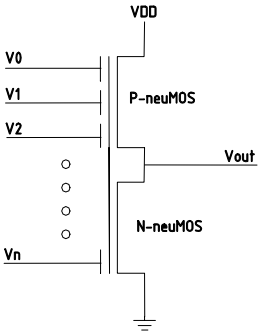

Figure 4: neuMOS inverter

3 neuMOS sw-opamp Structure.

The sw-opamp (switched opamp) is a modified op-amp DfT structure, and was first presented [25,29] in 1993 by A. H. Bratt et. al. of Lancaster University, UK. The purpose of the design is to facilitate application of analogue test vectors to internal analogue system nodes whilst simultaneously isolating the block under test from the circuits driving it.

The simplest method to isolate a functional block to be tested from the proceeding (driving) block is by [26] using a transmission gate (figure 5).

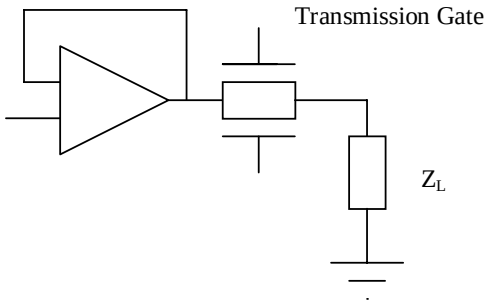

Figure 5: Simple Isolation Scheme

This scheme has serious drawbacks [25] due to the inclusion of the transmission gate in the large signal path, especially if the load (Z_L) is high or the output drive capability of the op-amp low.

The sw-opamp concept [25] avoids these problems by modifying the output buffer of the previous stage in order to inject the test stimulus directly.

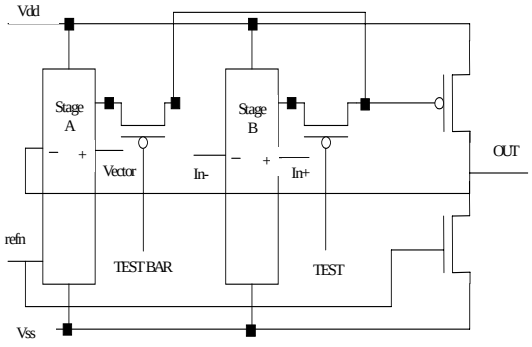

Figure 6: The sw-opamp concept

This is achieved by switching the op-amp into unity gain (buffer) configuration and providing a test voltage stimulus input. By replicating the input stage of the op-amp and inserting single pass transistors in the small-signal path between the input stage and the output stage, as

shown in figure 6 [25], the impact on performance in normal operating mode is minimal.

In conjunction with an overall system test methodology, this concept has proved very successful in several BIST implementations [27, 28]

The concept can be expanded, however, if the neuMOS input stage shown in figure 7 (with a basic output stage) is implemented.

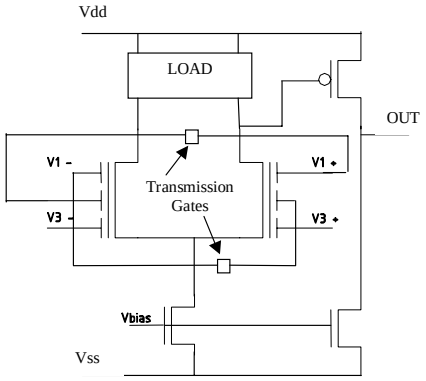

Figure 7: neuMOS amplifier

Figure 7 shows a basic operational amplifier (compensation not shown), but with the input MOSFET transistors replaced with 3-input neuMOS transistors. In addition, there are two complementary transmission gates shown which are used for test functions. Inputs V1 are the standard inputs, inputs V3 are test stimulus inputs.

The test circuitry has no performance penalty whilst in normal operating mode, yet provides very good test functionality.

Possible test modes are:

1. Activating both transmission gates whilst the circuit is active with 'real' signals to the amplifier through the V1 lines. In this way, the signals cancel (assuming a suitably high CMRR) and the output will settle at the offset voltage (which can be limit tested). Clearly, cancellation of the signals will not be perfect due to mismatches in the input gates of the neuMOS devices, and some signal degradation through the transmission gates. However, matching between neuMOS inputs is extremely good (the same as matching capacitors), so the mismatch problem is minimised. The impact of the transmission gates is expected to be small if the neuMOS gate areas are kept relatively small (but large enough for matching considerations). Finally note that because this technique relies on a high CMRR at signal frequencies, this in itself could be the basis for a test.
2. Whilst the input stage is cross coupled (described above), signals can be injected using the V3 lines (figure 7) to verify the amplifiers open-loop performance. The feedback network will not act on the test inputs, and the output resulting from the test inputs, although processed by the feedback network, will cancel on the cross-coupled input gates.
3. Leaving the input stage cross-coupled, by connecting V3- to the output, a unity gain amplifier with input V3+ is formed. This can now be used to inject a signal to the following circuit block in the same way the sw-opamp is used.
4. Whilst the circuit is functioning normally (i.e. not cross-coupled) it would be possible to inject a test stimulus using the V3 inputs which could allow some basic concurrent monitoring to be carried out, although this is heavily dependent on the specific feedback arrangement and the nature of the working signals being processed.

The main drawback of this circuit is that the common mode range of the amplifier must not be exceeded, which could be somewhat of a limitation if it is necessary to apply large signals to all the inputs. There is a solution to this problem, which is currently being investigated.

4 Outgoing quality enhancement through the use of neuMOS circuits.

Due to the increased functionality of the neuMOS transistor over the MOSFET, significantly fewer (but larger) active devices are required [7][11] to implement many complex logic functions. This leads to a considerable reduction in interconnect.

A typical layout will therefore exhibit considerably different probabilities of certain defects occurring compared to the more familiar MOSFET layout.

It is expected that metal layer shorts and opens will be dramatically reduced, gate oxide shorts similarly. Poly1 to Poly2 shorts (pin oxide defects) will be much more significant.

Assuming that poly1 to poly2 short defects will be dominant, we can now consider the manifestation of these defects in functional failures.

A Poly1 to Poly2 short will effectively destroy the properties of the neuMOS transistor by shorting the floating gate to one of the input gates. This will result in the shorted input gate being the sole controller of the neuMOS drain-source current, i.e. the neuMOS transistor will behave as a single input MOSFET. This, it is predicted, will be reasonably straightforward to detect as the normally highly functional neuMOS transistor will appear to fail almost totally. With so few active devices in the circuit, system failure is likely to result.

In summary, difficult to detect parametric faults are expected to be in the minority, with most defects causing clearly identifiable failures. If this turns out to be the case in commercial devices, it is likely that test escapes and reliability hazards will decrease increasing shipped product quality over the equivalent MOSFET implementation.

5 Conclusions

A qualitative analysis of the potential role of the neuMOS transistors in BIST for analogue and digital IC's has been given. A possible implementation of a neuMOS operational amplifier has been presented and it has been shown how this circuit can facilitate enhanced testability over an equivalent MOSFET testable op-amp, the sw-opamp. The paper concluded with a brief discussion into potential quality issues which may affect digital VLSI neuMOS circuits.

Future work will include substantiating the theories presented here with thorough simulation and prototype fabrication.

6 References

[1] T. Shibata + T. Ohmi *"A Functional MOS Transistor Featuring Gate-Level Weighted Sum and Threshold Operations"* IEEE Trans. on Electron Devices, 1992, vol. 39, no. 6, pp 1444-1455.

[2] T. Shibita. et. al. "A neuron-MOS Neural Network Using Self-Learning-Compatible Synapse Circuits" IEEE JSSC, 1995, vol. 20, no. 8, pp 913-922

[3] S. Kondo et. al. "Superior Generalization Capability of Hardware-Learning Algorithm Developed for Self-Learning Neuron-MOS Neural Networks" Jpn. J. Appl. Phys, 1995, vol. 34, part 1, no. 2B, pp 1066-1069

[4] H. Kosaka et. al. "An Excellent Weight-Updating-Linearity EEPROM Synapse Memory Cell for Self-Learning Neuron-MOS Neural Networks" IEEE Trans. On Electron Devices, 1995, vol 42, no. 1 pp135-143

[5] T. Shibata and T. Ohmi "Neuron MOS binary-logic integrated circuits – Part 1: Design fundamentals and soft-hardware-logic circuit implementation" IEEE Trans. Electron Devices, 1993, Vol. 40, pp510-576

[6] T. Shibata and T. Ohmi "Neuron MOS binary-logic integrated circuits – Part 2: Simplifying techniques of circuit configuration and their practical applications" IEEE Trans. Electron Devices, 1993, Vol. 40, pp974-979

[7] W. Weber et. al. "On the Application of the Neuron MOS Transistor Principle for Modern VLSI Design" IEEE Transactions on Electron Devices, 1996, Col. 43, no. 10 pp1700-1708

[8] H. Kwon et. al. "Low Power Neuron-MOS Technology for High-Functionality Logic Gate Synthesis" IEICE Trans Electron., 1997, Vol. E80-C, no.7, pp924-930

[9] K.Kontani et. al. "Clocked Neuron-MOS logic circuits Employing Auto Threshold Adjustment" ISSCC dig. Tech. Papers, 1995, FA 19.5, pp320-321.

[10] N. Yu, " A Real-Time Center-of-Mass Tracker Circuit Implemented by Neuron MOS Technology" IEEE Trans. Cir and Sys. II, 1998, vol. 45, no. 4, pp495-503

[11] K. Ike et. al, "A Module Generator of 2-Level Neuron MOS circuits" Computers and Electrical Engineering, 1998, vol. 24, pp33-41

[12] K. Kotani "Clock-Controlled Neuron-MOS logic gates" IEEE Trans Cir Sys ptII, vol. 45, no.4, 1998, pp518-522

[13] K. Ogawa et. al. "Multiple-Input Neuron MOS operation Amplifier for Voltage-Mode Multi-Valued Full Adders" IEEE Trans Cir Sys ptII, vol 45, no.9, 1998, pp1307-1311

[14] K. Kotani et. al. "Impact of high Precision Processing on the Functional Enhancement of Neuron-MOS Integrated Circuits" IEICE Trans. Electron, vol E79-C, no. 3, 1996, pp407-415

[15] T. Ohmi et. al. "Trends for future Silicon Technology" Jpn. J. Phys, vol. 33, part 1, no. 12B, 1994, pp6747-6755

[16] T. Ohmi et. al. " Intelligence implementation on Silicon Based on 4-Terminal device Electronics" Microelectron. And Reliab. Vol 37, 1997, no. 9, pp1315-1328

[17] T. Ohmi et. al. "Functionality Enhancement in Elemental devices for implementing Intelligence on Integrated Circuits" IEICE Trans Electron vol. E80-C, no. 7, 1997, pp 841-848

[18] T. Shibata et. al. "Event Recognition Hardware Based on Neuron-MOS Sofy-Computing Circuits" Comput. Elect. Eng. Vol. 23, no 6, pp 415-429, 1997

[19] J. Ramirez-Angulo "Low Voltage Circuits Building Blocks using Multiple Input Floating Gate Transistors", IEEE Tran . Cir. Sys ptI, vol 42, no. 11, 1995, pp971-974

[20] K. Tanno "Neuron-MOS Vt Cancellation Circuit and its Application to a Low-Power and High-Swing Cascode Current Mirror" IEICE Trans. Fund. Vol. E81-A, no. 1, 1998, pp110-117

[21] K. Yang "The Multiple Input Floating Gate MOS Differential Amplifier; an Analogue Computational Building Block" Proc. ISCAS, San Diego, 1992 pp 1212-1216

[22] K. Yang "A Multiple Input Differential Amplifier based on Charge Sharing on a Floating Gate MOSFET" Analogue int. Cir. And Sig. Processing, vol 6, 197-208, 1994, pp21-32

[23] B. Minch “Translinear Circuits using Subthreshold Floating-Gate MOS Transistors” Analog. Int. Cir and Sig Processing 9, 167-179, 1996, pp167-179
[24] H. Mehrvarz “A Novel Multi-Input Floating-Gate MOS 4-Quadrant Analogue Multiplier” IEEE JSSC vol. 31, no. 8, 1996, pp 1123-1131
[25] A. Bratt et. al. “Design-For-test Structure to Facilitate Test Vector Application with Low Performance Loss in Non-Test Mode” Elec. Letters 1993, vol. 29, no 16, pp1438-1440
[26] B. Wilkins et. al. “Towards a Mixed-Signal Testability Bus Standard” ETC, 1993
[27] D. Vazquez et. al. “Practical DfT strategy for fault diagnosis in active Analogue Filters”, Elect. Letters, 1995, vol. 31, no. 15, pp1221-1222
[28] D. Vazquez et. al. “A High-Q Bandpass Fully Differential SC Filter with Enhanced Testability” IEEE JSSC, vol. 33, no. 7, 1998, pp976-986
[29] A Bratt, A.H., Richardson, A.M., Harvey, R.J. and Dorey, A.P. "A Design-for-test Structure for Optimising Analogue and Mixed Signal IC Test.” *IEEE European Design and Test Conference*, pp. 24-34, Paris, March 6th-9th 1995.