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Reconfiguration-Based Built-In Self-Test
for Analogue Front-End Circuits

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Abstract

Previous work has shown that it is feasible to implement a fully digital test evaluation function to realise partial self-test on an automatic gain control circuit (AGC). This paper extends the technique to INL, DNL, offset & gain error testing of analogue to digital converters (ADC's). It also shows how the same function can be used to test an AGC / ADC pair. An extension to full self-test is also proposed by the on-chip generation of input stimuli through reconfiguration of existing functions.

1   Introduction

Design for Test (DfT) and Built-In Self-Test (BIST) for analogue and mixed signal circuits have received the growing attention of industry in order to alleviate increasing test related difficulties. Testability is predicted to become a primary design specification and has to be addressed in the early design stages, as escalating test time & costs need to be controlled and quality levels improved. In addition to improved fabrication testability, BIST offers an extension towards in-field verification while also allowing test re-use and providing a promising approach to automate mixed signal test generation.

This paper describes an extension of an on-chip, fully digital test evaluation function [1,2] to an AGC (Automatic Gain Control circuit) ADC pair. On-chip ramp stimulus generation technique are proposed that are based on reconfiguration of available mixed signal cells to implement a full BIST function.

2   State-of-the-Art in Analogue and Mixed-Signal Built-In Self-Test

Currently, functional testing is performed on analogue circuits after wafer processing, where every IC is checked against critical specifications [3, 4]. The optimisation of such circuit specific test programs is difficult and expensive. Generic DfT guidelines and practical mixed signal BIST which can be applied in the early design stages could pave the way to satisfying industrial demands for the use of digital only testers [5, 6] and a structural methodology for test program generation and optimisation. Increasing test costs, aggressive demands on time to market, and the need to improve product quality currently drive this change in test philosophy.

Various mixed signal BIST approaches have been published, such as ABIST [7], adcBIST [8], AUBIST [9], BIST for converters on a CODEC [10], HBIST [11], MADBIST [12], OBIST [13], & TBIST [14]; additionally a review on mixed signal BIST can be found in [15]. An overview of defect oriented testing and DfT optimisation of mixed signal ICs is presented in [4, 16, 17, 18].

3   Analogue Front-End Circuit

The demonstrator analogue front-end contains an automatic gain control circuit (AGC) followed by a 6 bit ADC (Figure 1). In functional mode, the gain set S is incremented or decremented by a digital control loop that monitors the ADC output. A typical application of this kind of circuit is the digitisation of sound signals in consumer products. In many applications, this type of function is used on devices where D-A converters (DAC) have also been implemented. In these cases the DAC can be re-used for on-chip stimulus generation. To generate a ramp stimulus, a binary counter can be connected to the DAC inputs to obtain a step function at its output. It has to be ensured that the DAC resolution and the linearity of the stimulus are sufficient to apply ramp tests to analogue cells. A detailed DfT study on an AGC circuit has been presented in [19,1] leading to the proposal for a new on-chip test evaluation structure for AGC gain step size testing [2].
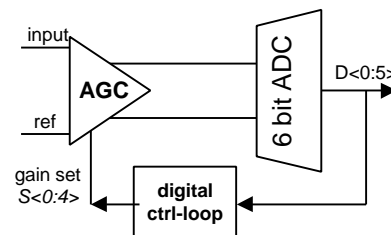

Figure 1: Analogue front-end

4   Output Response Analysis

Figure 2 & Figure 3 show the blocks that have to be added to the front-end design at the top level to enable on-chip test evaluation. The circuitry can be used to verify the gain step size and output voltage swing (OVS) for the AGC (Figure 2) and can be reconfigured to test the ADC (Figure 3) for integral and differential non-linearity (INL & DNL).
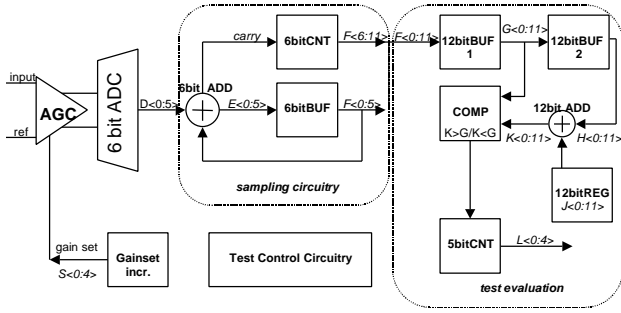
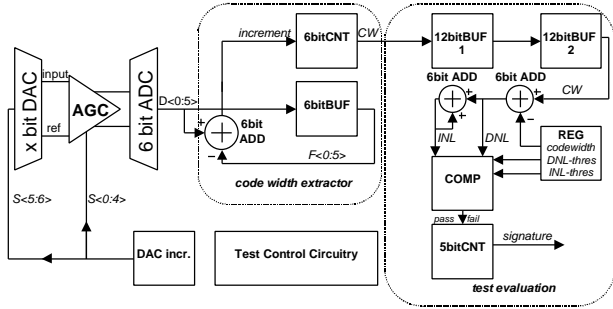Figure 2: Test evaluation structure for AGC test

Figure 3: Test evaluation structure for ADC test

For the AGC tests, the sum of a set number of ADC output patterns is calculated within the *sampling circuitry*. The sample taken can then be compared against a previous sample and the difference can be checked to be larger (or smaller) than a set threshold within the *test evaluation* block. Test parameters can be set by initialising the contents of the registers and counters. These blocks will be embedded in a digital scan chain that will also be used to read out the test signature.

For the ADC tests, the *code width extractor* (Figure 3, reconfigured *sampling circuit* from Figure 2) computes the width for each code word (CW, Figure 4) when a ramp stimulus is applied to the ADC input. The test evaluation circuitry subtracts the ideal code width (1/8 Full Scale in Figure 4) from the measurement to obtain the DNL; the INL can be computed by simply adding the DNL's during the ramp test. For ADC's, the offset error is defined as the deviation from the ideal location of the first transition level, and most usually the gain error as the deviation from the ideal of the last transition level (while offset error is reduced to zero, Figure 4). The computation of those transition levels enables testing for gain & offset error when a ramp stimulus is applied.

If the ramp stimulus is generated on-chip by reconfiguration of a DAC, fault masking effects have to be taken into account, especially for ADC testing.

The reconfigurable digital only test evaluation structure allows the generation of a simple pass/fail output for the gain step size test, the verification of the AGC's

OVS, and DNL, INL, gain, and offset of the ADC. The circuitry has the following advantages compared to conventional testing:

- *ATE supplies only speed control and test access*
- *Compatible with the use of digital access structures, e. g. IEEE 1149.1 test access port*
- *Synthesisable from Verilog/VHDL*
- *Requires only minor changes and in some cases no changes to the AGC*
- *Simple pass/fail result*
- *Easily enhanced through the addition of diagnostic features*
- *Reconfiguration technique minimises area overhead and potential yield loss.*
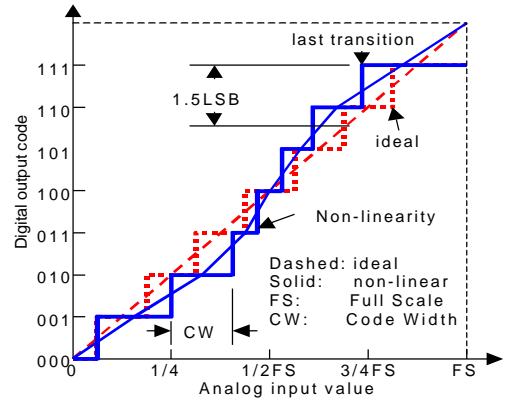

Figure 4: Non-linearity & code width of 3-bit ADC

4.1 AGC Gain Step Size Test

The test routine has been described above. For the implementation of this test, the cells *6bitADD*, *6bitCNT* and *6bitBUF* are used to add a set number of ADC output codes (*D<0:5>*, see Figure 2) while a DC voltage is applied to the AGC input. *F<0:11>* holds the sum of the samples taken. *12bitADD* adds the test threshold (*J<0:11>*), set in a *12-bit register*, to the previous sample (*H<0:11>*) which has been buffered in *12bitBUF2*. The sum (*K<0:11>*) is compared to the new sample (*G<0:11>*) held in *12bitBUF1*. If $G>H+J$, the minimum gain step has been proven present. Every time the gain set (*S<0:4>*) is increased by *gainset_incr* the comparator output is added to form *L<0:4>* in *5bitCNT*. When the test is completed, *L* has to be equal to 32. The use of two 12-bit registers allows testing each gain step for a minimum and maximum size. When the test threshold (*J<0:11>*) holds the maximum gain step size, it has to be proven that $G<H+J$.

Four test parameters can be set by the use of a scan chain. *N* defines the number of ADC outputs that have to be added in the sampling circuitry (2^N, for $1 \leq N \leq 5$). *GI* defines the gain step increase and can be varied between 1 and 7 (for more details see [2]). The minimum or

maximum difference (*I*) in the samples taken can be set in the *12-bit register*, while *MinMax* has to be set high/low to test for a minimum/maximum difference. The expected test time is:

$$t_{gainsteptest} = t_{ADCclk} \cdot 2^N \cdot 32,$$

where t_{ADCclk} is the ADC clock period, 2^N the number of ADC output codes sampled, and "32" is the number of gain sets.

Noise effects are eliminated by summing a set number of ADC outputs using the result as the parameter processed within the test evaluation block. The more output codes summed, the better noise cancellation.

Offset effects have also been cancelled, as they influence every sample set in the same way. Only if the offset drives the ADC input out of the valid input range, will the sample sum become faulty (smaller than it should be). However, this would result in a decreased gain step, and also the following gain steps will be too small. The magnitude of tolerable offset can be taken into account by properly selecting the DC input voltage of the AGC and its reference voltage.

By implementing this top-level test evaluation circuitry, the expected test time for the AGC can be reduced by about 70% without a decrease in test coverage.

For analogue front-ends where the AGC's OVS does not fit the ADC input range, techniques have been proposed in [2] to increase the resolution for the DC testing.

4.2 AGC Ramp Test

Most faults affecting the AGC can be detected by testing the OVS of the AGC, as they cause a 'stuck at voltage' or 'stuck at voltage range' at the AGC output. The test response to a ramp stimulus applied to the analogue input of the AGC can be evaluated on-chip by the circuitry described above.
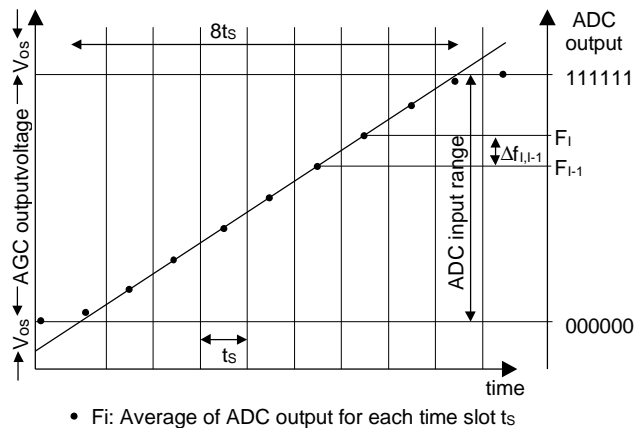

- Fi: Average of ADC output for each time slot t_S

Figure 5: AGC ramp test evaluation

For each time slot t_S, the ADC output is sampled (Figure 5). The samples F_i represent the average of the ADC output for each section. The *test evaluation* block (Figure 2) is then used to count the number of time slots where the difference ($Df_{I,I-1}$) between the sample taken (F_I) and the previous sample (F_{I-1}) is in a specified range. The contents of *5bitCNT* can be directly related to the OVS of the AGC.

The ADC sampling frequency, the number of ADC outputs to be sampled in the *sampling circuitry*, and the thresholds for *test evaluation* can be set by initialising the contents of the registers and counters.

To test the AGC output voltage swing, the required measurement resolution has a significant impact on the test time. The resolution is mainly influenced by the number of ADC output samples that have to be taken (see Figure 5). The authors propose to add 64 ADC outputs in order to extract a precise and noise tolerant averaged response over each time slot t_s. The test time can be give as:

$$t_{ramp} = t_{ADCclk} \cdot 2^N \cdot s,$$

where t_{ADCclk} is the ADC clock period, 2^N the number of ADC outputs to add, and *s* the number of time slots (32 maximum). The OVS can be calculated from the test signature *L* (see Figures 2&3):

$$OVS_{meas} = l \cdot j$$

where *l* is the decimal representative of the test signature and *j* the minimum difference (set in *12bitREG*, Figure 2).

4.3 ADC Test Evaluation

As illustrated in Figure 3, the on-chip test evaluation circuitry can be reconfigured to evaluate the test response of the ADC. When a ramp stimulus is applied to the ADC, the code width can be computed. To extract DNL for each ADC input, the ideal code width has to be subtracted form the measured code width. The INL can be determined by adding the DNL from the first up to the current code. The digital comparator (COMP in Figure 3) can then be used to verify whether the INL & DNL are within their specifications. The test signature can either contain the number of test failures during the ADC ramp test or the test can be aborted in order to determine which code caused a test failure for INL or DNL. By computing the first and last transition level, gain and offset errors can be extracted. The difference between the first transition level and the ideal transition (1/2 LSB) is equal to the offset error. By subtracting the offset error from the last transition level and calculating the difference to the ideal last transition, the gain error can be obtained.

Future work will address noise filtering techniques and fault masking effects when on-chip stimulus generation techniques are implemented.

5   Reconfiguration-Based Ramp Stimulus Generation

Figure 6 illustrates the AGC cells. The analogue front-end can be reconfigured to obtain a voltage scaling 5-bit DAC (*AGC_DAC*) followed by an opamp of constant gain. To enable the use of the *AGC_DAC* for on-chip ramp stimulus generation, it is essential to reconfigure the *AGC_DAC* in such a way that it provides a linear transfer characteristic. Note that the AGC would normally be designed to obtain a linear increase in its gain (in dB). For this purpose one internal AGC node must be accessible at the system level (not externally), and one resistor of the *AGC_DAC* resistor ladder must be disabled.
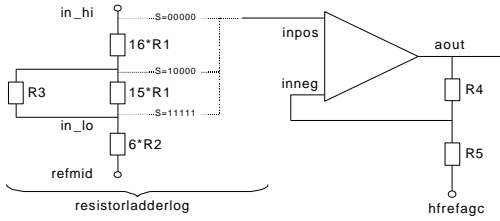
Figure 6: Simplified AGC Block Diagram

To generate a ramp stimulus of sufficient linearity (and resolution) to test the 6-bit ADC (following the AGC), the resolution of the 5-bit *AGC_DAC* has to be increased to obtain precise measurements of the code widths. The following sections provide an overview of techniques that can be used to increase the *AGC_DAC* resolution for test purposes. In each case, the aim is to increase the resolution by providing 2 additional bits (can be expanded) to the 5-bit *AGC_DAC*. It is desirable for BIST to make use of existing cells to limit the area overhead.

5.1   Switching *AGC_DAC* Resistor Ladder Potentials

It is possible to add resistors (*R_upper* & *R_lower* in Figure 7a) to the upper and lower end of the *AGC_DAC* resistor ladder (31*R, Figure 7a). By changing the values of *R_upper* and *R_lower* through control of two bits, (*s5* & *s6*, as illustrated in Figure 7b) the *AGC_DAC* reference voltages (*in_lo* and *in_hi*) can be provided with switchable bias to cover the complete ADC input range (*adc_lo* to *adc_hi*). In this case, for each value of *s5* & *s6* the potentials at the *AGC_DAC* resistor ladder will cover a quarter of the ADC input range. A 7-bit (effective) DAC can be obtained by using the *AGC_DAC* structure for the 5 LSB's and using *s5* & *s6* as the MSB's.

Figure 7 illustrates how to switch the *AGC_DAC* resistor ladder potentials (*in_hi* to *in_lo*) across the ADC input range (*adc_lo* to *adc_hi*). Diagram (b) shows one possible implementation where only 3 resistors (of identical value) and some switches (transmission gates) have to be added. More elegant is the use of a preceeding reconfigurable DAC, as described in the following section.
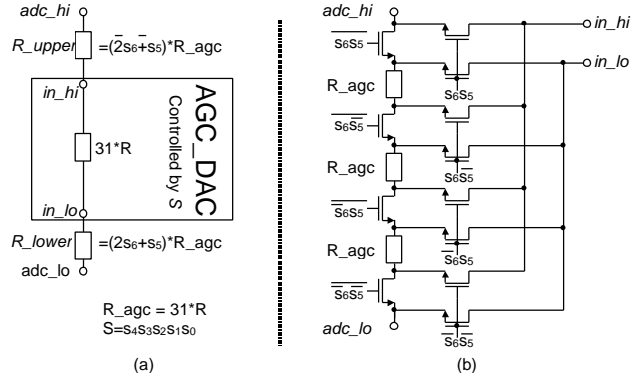
Figure 7: Switching *AGC_DAC* resistor ladder

5.2   Cascoded Structures

To increase the resolution of the DAC used for on-chip ramp stimulus generation, the *AGC_DAC* could be followed or preceded by a voltage scaled low resolution DAC. Similar to the *AGC_DAC*, a 2-bit voltage scaled DAC can be placed in front of the *AGC_DAC*, where the 2-bit DAC will have to be reconfigurable to provide two output voltages which then control the nets *in_hi* and *in_lo* (Figure 8). A separate 2-bit DAC will allow the *AGC_DAC* resistor ladder potentials to be switched across the ADC input range in four sections. For each section the voltage across one resistor (*R_dac* in Figure 8) will be used to reference the *AGC_DAC* resistor ladder.

Effectively the 2-bit DAC (controlled by the 2 MSB's) and *AGC_DAC* (controlled by the 5 LSB's) combine to a 7-bit converter. As in Figure 7, the NMOS transistors would be replaced by transmission gates. Alternatively the same approach could be used to implement a 2-bit DAC following the *AGC_DAC*.
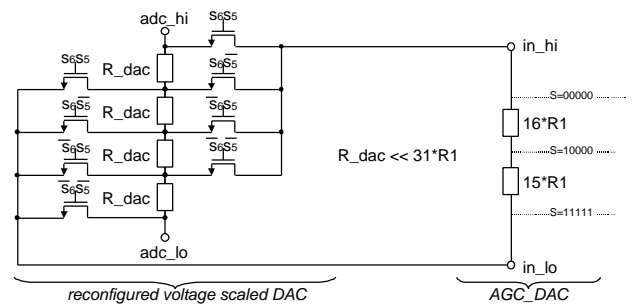
Figure 8: Preceding voltage scaled DAC

5.3   Voltage Storage Element

Any kind of DAC could precede the *AGC_DAC*. If the DAC has got only one analogue output voltage, control of *in_hi* & *in_lo* can be achieved by sampling and storing the DAC output for a set digital input and then incrementing the digital input to generate a second output voltage. This second output voltage and the stored value could then control *in_hi* & *in_lo*.

5.4   Use of ATE

If the *AGC_DAC* inputs *in_hi* and *in_lo* are both accessible, DC voltages could be provided from the external ATE (Automatic Test Equipment) in the same way that they would be provided by an on-chip DAC. Also accessible inputs of a preceding DAC could be used to increase the combined DAC-*AGC_DAC* resolution. The whole ramp stimulus generator can be followed by a RC network to improve the linearity of the ramp even further.

6   Conclusions

A partial BIST structure has been designed to implement on-chip test evaluation for an AGC gain step test, the verification of the AGC output voltage swing and verification of ADC specifications (INL, DNL, gain, offset). This study has shown that digital solutions to partial self-test are feasible for analogue front-ends of this type and that in many cases reconfiguration of digital control loops may well be a highly optimal BIST enhancement.

The test evaluation circuitry can be implemented at the macro level using digital logic only and hence will require minimal design effort if synthesis techniques are used. This solution has been shown to improve the AGC test time by up to 70% without any degradation in fault coverage. Where the proposed solution is implemented in parallel with careful design for fault tolerance, very high fault coverage is feasible.

To extend the partial BIST to a full BIST for analogue front-ends, a number of techniques have been proposed to generate a ramp stimulus on-chip. These techniques involve re-using existing components with either DC signals from the tester or from a separate on-chip DAC. The use of these techniques can improve the accuracy of the BIST ramp stimuli.

7   References

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