Defect Oriented Test Development Based on Inductive Fault Analysis

R. J. A. Harvey[1], A. M. D. Richardson[1], and H. G. Kerkhoff[2]

[1]SECaMS,
University of Lancaster,
Lancaster,
Lancashire,
LA1 4YR,
UK.
Tel. +44 1524 65201
Fax. +44 1524 594207

[2]MESA Research Institute,
University of Twente,
Department of Electrical Engineering,
P.O. Box 217,
7500 AE Enschede,
The Netherlands,
Tel. +31 53 89 26 41
Fax. +31 53 34 19 03

Abstract

This paper describes a method of developing a Defect Oriented Test (DOT) strategy by using Inductive Fault Analysis (IFA) and layout dependent fault models extracted from process defect statistics. The results of a quantitative prediction of the effectiveness of several test strategies, such as functional, IDDQ, and a low voltage power supply method, on a current-mode Digital to Analogue Converter are discussed and show that no single test method is superior.

1 Introduction

In the modern semiconductor manufacturing industry there is an increasing demand to produce high quality ICs. The root cause of this pressure stems not only from industry aiming to minimise yield loss for economic advantages, but also to reduce the number of shipped defective ICs. In the former, optimisation of yield is primarily a problem for the fabrication line, however the latter is equally important and currently can only be achieved by high quality testing.

In order to minimise the number of test escapes, it is important to be able to model all of the probable faults which may occur during manufacture. The typical methodology is to devise a test which will detect all of the faults as each is embedded in the IC, and can be done by a process of circuit simulation. These faults are represented by carefully developed fault models. Such a methodology routinely has two simulation stages. The first is the prediction of where faults are likely to occur in the topology of the circuit and how these faults can be mapped to the electrical connectivity, and secondly, an electrical circuit simulation to generate an optimised test vector set.

This use of defect oriented testing coupled with Inductive Fault Analysis (IFA) [1-3] and process defect statistics, has become an important research method in developing test methodologies for the

next generation of ICs. In this short paper a defect oriented simulation approach is used to evaluate the effectiveness of a number of test methods for a 10-bit current-mode Digital to Analogue Converter (DAC) manufactured in a sea-of-gates process. Figure 1 shows the basic principle of successive current division using a standard R-2R ladder network. Figure 2 shows how an individual current division stage is implemented, a description of which can be found in [4].

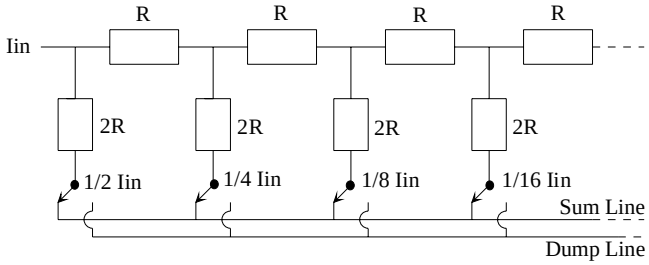


Figure 1: The R-2R ladder current division principle used by the DAC.

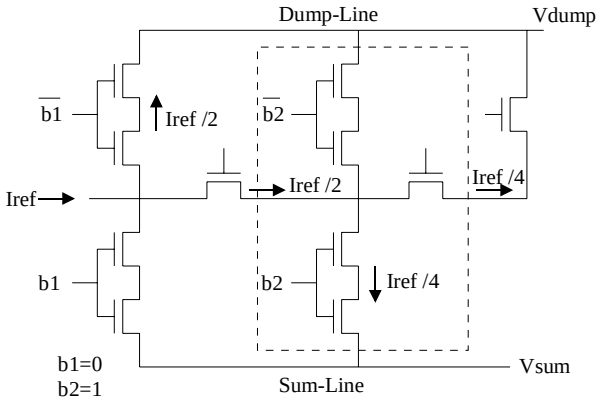


Figure 2: Implementation of the current division principle used in figure 1.

2 IFA Analysis

2.1 Layout Defects

To determine the spatial positions of defects and to extract corresponding electrical faults, the software tool VLASIC (VLSI Layout Simulation for Integrated Circuits) [5-7] is used. VLASIC was originally developed as a catastrophic fault yield simulator which uses a Monte Carlo algorithm to scatter spot defects onto the layout, in accordance with a set of defect statistics derived from the target process. These defect statistics are defined by distribution coefficients in spot size and spatial position, and can report one of eighteen different physical defects (eg. oxide pinholes, missing metal, extra polysilicon etc.) which manifest as either a short or open circuit due to the addition or subtraction of material. In analysing the DAC one-hundred-thousand defects are inserted into the layout, resulting in a graded fault list and a list of the associated electrical nodes involved. Automatic netlist insertion of these faults is achieved by the use of a fault model consisting of a range of resistances [8,9] and a post-

processing program. Systematic fault simulation using the circuit simulator ELDO [10] generates result lists interpreted by further post-processing. Although VLASIC reports the existence of open circuits, they are neglected in this experiment because of two reasons. Firstly, the number of open circuit faults in the target process are found to be small in comparison with other types, and secondly, complex geometry changes in the layout due to missing material are difficult to relate to the circuit netlist.

In following the process of scattering defects onto the DAC layout, a defect type list is shown in table 1. Note the quantisation of defect type numbers, which is due to best estimates obtained from process monitors for a similar fabrication line, and are supplied by Philips. Clearly the dominating defects are due to extra first metal and extra second metal. Also of significance are the extra polysilicon defects followed closely in number by polysilicon to first metal pinholes.

Defect Type	Occurrence Number
POSMF Extra First Metal	**43478**
NEGMF Missing First Metal	434
POSCA Extra Active-First Metal Contact	434
NEGCA Missing Active-First Metal Contact	217
POSCP Extra Poly-First Metal Contact	434
NEGCP Missing Poly -First Metal Contact	217
POSPG Extra Poly	**4347**
NEGPG Missing Poly	434
POSAA Extra Active	2173
NEGAA Missing Active	434
POSMS Extra Second Metal	**43478**
NEGMS Missing Second Metal	434
POSVA Extra First Metal-Second Metal Contact	434
NEGVA Missing First Metal-Second Metal Contact	434
PIN1 Poly-First Metal Oxide Pinhole	**2173**
PIN2 First Metal-Second Metal Oxide Pinhole	434
PING Gate Oxide Pinhole	0
PINJ Junction Leakage	0
Total Number of Defects	**99989**

Table 1: Showing VLASIC reported defects when scattering one-hundred-thousand defects onto the DAC Layout.

2.2 Extracted Faults

Figure 3 shows the type and number of electrical faults extracted from the defects listed in table 1. Fault class NEWGD occurs when extra polysilicon spans an active region, and fault class SHORTD occurs when there is a short between the source and drain of a device.

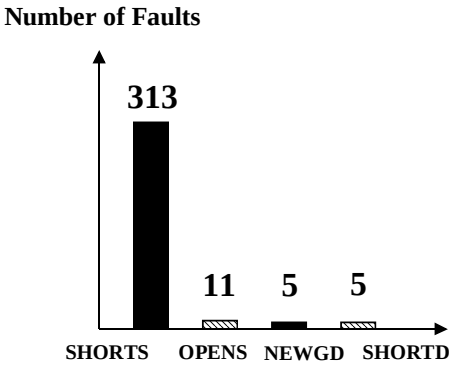


Figure 3: Graph showing fault type proportions resulting from all defects.

The dominant fault type is clearly the shorts, as is in agreement with the statistics obtained from real fabrications lines. Referring to figure 4, which represents a floor plan of the four most significant bits of the IC, figure 5(a) shows the corresponding area of the layout having superimposed the spatial arrangement of faults. Manually editing figure 5(a) for fault density, figure 5(b) clearly shows two parallel clusters. The lower cluster corresponds to devices of the current divider stages, and the higher cluster corresponds to the area where the metal node I_{sum} runs in parallel with the metal node I_{dump}. Although not evident from inspection of the sea-of-gates layout because of the apparent uniform density of tracks and connectivity, a clear disadvantage results from these two tracks being approximately 3μm apart and running parallel for the whole length of the layout.

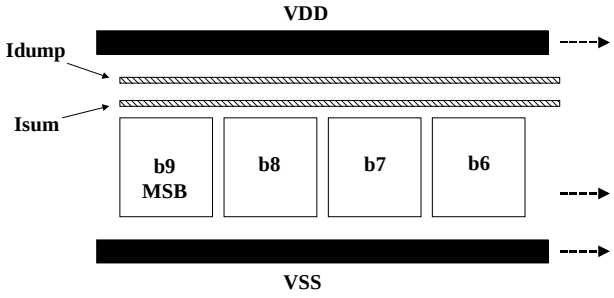
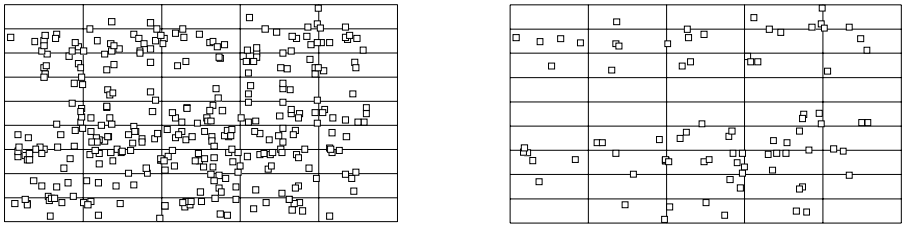


Figure 4: Schematic floor plan showing VDD and VSS, the position of current dividers associated with
the four most significant bits, and the long adjacent parallel nodes I_{sum} and I_{dump}.



(a) (b)

Figure 5: (a) Showing the topological fault distribution over the segment of the layout drawn in figure 4.
(b) Showing (a) after simple processing to accentuate the highest fault density regions.

3 Analysis of Test Strategy

The defect distribution and extracted fault can now be used to assess test-effectiveness for the DAC. In large production environments the test-time is always an economical constraint, and as such a number of faster DC tests may be used as an initial screen in preference to more expensive transient response methods. Recent work has shown the advantage of using power supply current as a test quality metric for purely digital circuitry [11], and it is hoped that the knowledge gained can be applied to analogue and mixed-signal designs. In addition, a novel test strategy based on changing the bias condition of the circuit by controlling power supply voltage has been shown to be a useful method [9,12]. In this work estimation of fault coverages are made by assuming changes from the fault-free circuit operation of ±100mV for the voltage sensing test, and ±100μA for the current sensing test; these values are considered larger than process variations [13]. Fault coverages are also calculated with thresholds of ±10mV and ±10μA for comparison.

3.1 DC Voltage Test

Using a test set of all bits high, a first test assessment was made by monitoring the output response of the DAC using two levels of power supply voltage. Figure 6 shows that by changing the threshold of test, the estimated fault coverage increases by 10%. No apparent advantage is to be gained by reducing VDD from 5V to 3V, however a number of faults are able to be detected when VDD=3V which are not seen at VDD=5V.

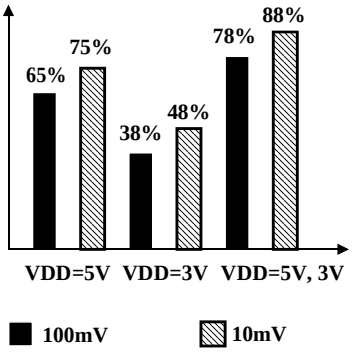


Figure 6: Graph showing estimated fault coverages for the DAC using a DC voltage test strategy with test thresholds of ±100mV and ±10mV for values of VDD=5V and VDD=3V.

3.2 Two Vector IDDQ Test

Using a limited test set of all bits high and all bits low, figure 7 shows that a power supply current test is not as successful as the voltage test. The highest fault coverage is achieved by having all bits low,

and there is no evident advantage in combining the results from the two test sets, or by lowering the threshold of measurement.

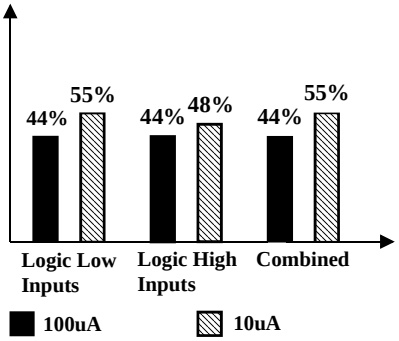


Figure 7: Graph showing estimated fault coverages for the DAC by monitoring power supply current using two test sets of all bits high and all bits low.

3.3 Functional Test

A functional test for the DAC is exhaustive and involves applying all combinations of input for the 10-bits. Fault simulation using a large number of test vectors is difficult to achieve due to simulator convergence problems and excessive simulation time. A different strategy is therefore needed for fault simulation, and is described in the next section.

3.3.1 Circuit Partitioning

Previous work [9] has shown that for complex mixed-signal circuits, fault simulation time can be reduced by circuit partitioning and the writing of accurate behavioural models. The DAC lends itself well to partitioning by already having a regular structure of current dividers, as shown in figure 8.

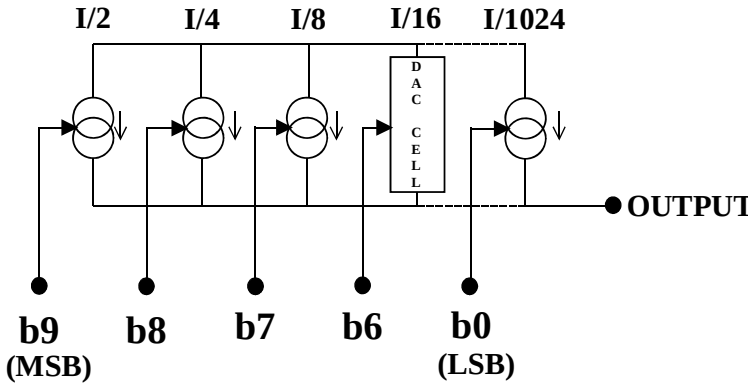


Figure 8: To illustrate the construction of the DAC from individual current dividers.

Hybrid fault simulations where performed by replacing each current divider with a simple controllable current source behavioural model written in SPICE using the ELDO circuit simulator, except the block

which is to have a target fault inserted. In order to achieve this analysis it is necessary to isolate one of the current divider stages as shown in figure 8 and perform another fault extraction analysis, confining the defects to a cell. Reported faults for one stage can be assumed to have the same likelihood of occurrence in all stages of the DAC.

3.3.2 Fault Coverage

Intensive use of computer time allows an estimation of DC fault coverage to be made for two types of analyses. In the first analyses, incremental combinations of the 10-bit input are used as test vectors and a measurement of the DC output voltage of the circuit is made after the systematic introduction of faults into each cell in-turn. The results are post-processed to calculate fault coverage at the two levels of threshold used in previous experiments. Simultaneously a measurement of power supply current is recorded and is used to calculate the IDDQ fault coverage. A second analysis involving the same procedure but using VDD=3V and a logic high defined at 3V for each bit, was unsuccessfully attempted. It was found that the majority of simulations would not converge, and although some hybrid netlists were eventually made to converge, a significant portion remained unsimulatable. This analysis was therefore neglected.

Figure 9 shows estimated fault coverages using a full functional test. It is seen that although these tests are found to be no better than the simple DC tests described in sections 3.1 and 3.2, a large difference in fault coverage occurs between the two thresholds of measurement.

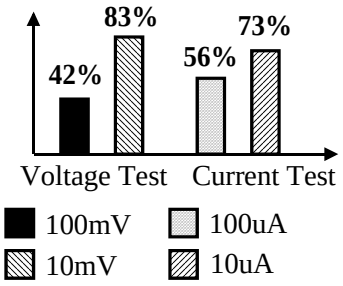


Figure 9: Graph showing estimated fault coverages for the DAC using a functional test strategy for various threshold of measurement.

4 Analysis of Power Supply Control

Sections 3.1 and 3.2 show the usefulness in utilising the power supply as a test vector to detect a number of defect oriented faults which are otherwise masked. Control of the power supply to alter the biasing conditions of devices is easily accomplished within the testing strategy reported in this paper. Present and future work is concentrating on the identification of faults and a thorough explanation of these effects. A rigorous treatise of this method, which will contain an extension of these techniques to other generic circuits types, will be reported in future additions to this work.

5 Conclusions

A test evaluation methodology based on defect oriented fault models has been used on a 10-bit current-mode DAC manufactured in a sea-of-gates technology. It has been shown that an estimation of fault coverage for this circuit can be made for a particular testing strategy, however this work reports on the use of three DC tests associated with the measurement of output voltage and power supply current.

The first two methods use simple test stimuli for the 10-bits, whereas the third method uses all combinations of these inputs to mimic a rigorous functional test. All estimations of fault coverages have been made at two thresholds of measurement, and show that neither the voltage sensing nor the current sensing methods have any advantages over each other. An enhanced estimated fault coverage of 88% has been made with the voltage sensing method by combining the results from this analysis with another analysis at a reduced power supply voltage of 3V. Future work will concentrate on the mechanisms of this novel test at the device level.

The third test was undertaken to simulate functional operation by performing a DC analysis for all combinations of input for every fault. A method of circuit partitioning and hybrid fault simulation using a high-level model is used to speed-up fault simulation time. It is found that the best fault coverage is achieved by monitoring the output voltage using a measurement threshold of 10mV, and it is noted that fault coverage values are considerably higher for the small measurement threshold for both power supply current monitoring and output voltage measurements. Clearly a reduced test vector set can be defined by identifying and dropping the 10-bit sets which are unable to detect any faults.

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