Accurate *A Priori* Signal Integrity Estimation Using A Multilevel Dynamic Interconnect Model for Deep Submicron VLSI Design

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Abstract

A multilevel dynamic interconnect model was derived for accurate a priori signal integrity estimates. Cross-talk and delay estimations over interconnects in deep sub-micron technology were analyzed systematically using this model. Good accuracy and excellent time-efficiency were found compared with electromagnetic simulations. We aim to build a dynamic interconnect library with this model to facilitate the interconnect issues for future VLSI design.

1. Introduction

With the increasing sophistication of design automation tools, the areas of logic design and physical design have seen a distancing from each other. The fabless design shop is responsible for the HDL design and synthesis, passing over a netlist to the foundry for physical design. The success of this approach is largely based on the predictability of timing after placement and routing. That is, the interconnect loading has relatively small effect on timing results so that crude interconnect capacitance estimates can be used in synthesis and few, if any, timing problems would be evident after physical design.

With deep sub-micron technologies, however, there is a distinct danger of this traditional methodology breaking down due to poor interconnect estimations and susceptibility to cross-talk noise. Therefore, as sketched in Fig.1 (a), state-of-the-art VLSI design needs a complex post-layout interconnect parasitic extraction for signal integrity, or timing and noise analysis [1]. The most accurate extraction technique requires 3D electromagnetic (EM) simulation that is extremely memory and time consuming [2]. In addition, due to the fact that the extraction can only be performed on the circuit layout while the existing pre-layout capacitance models are poor, many iterations are required to get a high performance design to work. This is very inefficient particularly when future giga-scale integration or system-on-chip (SoC) is targeted.

A much more time efficient design cycle would be one shown in Fig.1 (b) where the noise and timing analysis is completed before placement and routing while post-layout extraction is merely for final circuit functionality verification [1]. Currently this is not feasible because the actual interconnects exhibit very different behavior from their pre-layout models [1-3]. Therefore, faster and accurate pre-layout interconnect models are urgently called for. These models should dynamically represent complex 3D multilevel interconnect structures, or in other words, should allow change of wiring cross section, spacing, and use of shielding to control the interconnect delay and cross-talk noise. While much attention has been paid to post-layout extraction techniques, little effort has been made to derive an accurate and dynamic model for interconnects which can be used as rule-based parasitic estimates for *a priori* signal integrity analysis [3-4]. In this paper, we present a multilevel, dynamic interconnect model, and show how it allows accurate signal integrity estimation. The model can include the parasitic effects of a complicated interconnect structure including inter-level cross-talk capacitance, inter-wire cross-talk capacitance, and inter-wire inductance. Due to its time efficiency and capability of dealing with complicated 3D structures, the model can be applied in pre-layout tools for timing and noise analysis over a variety of partitioning and wiring plans.

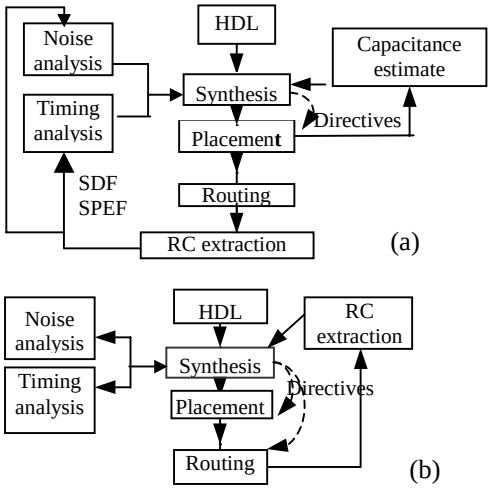

Figure1. (a) State-of-the-art ASIC design flow that includes noise analysis in post-layout verification, and (b) future design flow in which synthesis, interacting with both noise and timing analysis, directs both placement and routing.

2. Multilevel dynamic interconnect model

Fig.2 is a three-dimensional view of the interconnect model. The highly doped substrate has been assumed a perfect conductor plane. Due to the fact that coupling capacitance terms die out rapidly with distance in the presence of isolating metal structures, only those terms between adjacent lines are adopted. Basic components are the fringing capacitance c_f, the mutual capacitance

c_m, and parallel plate capacitance c_p. The ground capacitance term per unit length of a wire is given by:

$$c_s = c_f + c_p + c'_f \quad (1)$$

Here c_f is the portion of the fringing capacitance to that side (if any) where no adjacent line exists, and c_f' is the portion of the fringing capacitance to that side (if any) which has an adjacent line. The terms of c_f and c_m for each metal layer are obtained from a two-dimensional field solver combined with curve fitting for a variety of wire widths and spacings.

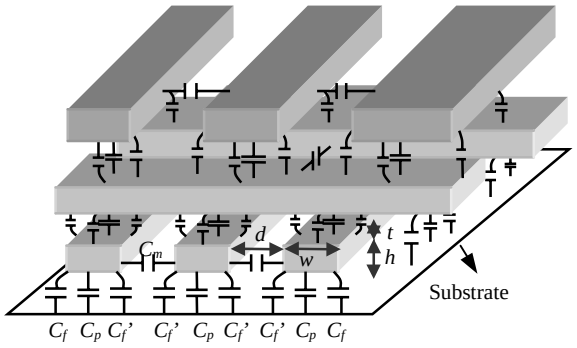

Figure 2. Three-dimensional view of the multilevel interconnect model and its basic capacitance components.

The inputs to the field solver were material parameters and the process profile obtained from the technology file, and the specified wire geometry parameters that changed for each computation. After generation of a database, empirical formulas for geometry dependent c_f and c_m were developed using a curve-fitting method. The relationship between the fringing capacitance terms due to field sharing between adjacent wires is given by Eq. (2) [5].

$$c'_f = c_f \left[1 + (h/d)^{\beta}\right]^{-1} \quad (2)$$

Here β is a wiring cross section associated constant obtained from the curve fitting. The cross-over capacitance between two wires (wire 1 and wire 2) is given by:

$$C_{cross} = w_1(c_{f1-2} + c'_{f1-2}) + \varepsilon_k\left(\frac{w_1 w_2}{h}\right) + w_2(c_{f2-1} + c'_{f2-1}) \quad (3)$$

where c_{f1-2} and c_{f2-1} (or c'_{f1-2} and c'_{f2-1} if adjacent lines exist) are the fringing capacitance terms from wire 1 to wire 2 and wire 2 to wire 1 respectively, and w_1 and w_2 the widths of the corresponding wires.

Complex 3D interconnect parasitic capacitances can thus be estimated using this model. Self and mutual inductance values per unit length of the wires were extracted from the capacitance matrix using the same interconnect array but in a homogenous media:

$$l_s = \frac{\varepsilon_o \mu_o}{2}\left(\frac{1}{c_s^o} + \frac{1}{c_s^o + 2c_m^o}\right) \quad (4)$$

$$l_m = \frac{\varepsilon_o \mu_o}{2}\left(\frac{1}{c_s^o} - \frac{1}{c_s^o + 2c_m^o}\right) \quad (5)$$

where ε_o and μ_o are the permittivity and permeability of free space, c_s^o and c_m^o are the self and mutual capacitance terms for the corresponding wires but the inter-level dielectrics are now replaced with air. However, mutual inductance terms between crossing interconnection lines are not supported in this approach.

3. Model verification and cross-talk analysis

We have developed a number of empirical formulas by curving fitting of the EM simulated data. One of the more simple but also very useful set of formulas is:

$$c_f = \varepsilon_r \varepsilon_o \left[0.075\left(\frac{w}{h}\right) + 1.4\left(\frac{t}{h}\right)^{0.222}\right] \quad (6)$$

$$c_m = c_f - c'_f + \varepsilon_r \varepsilon_o \left[0.03\left(\frac{w}{h}\right) + 0.83\frac{t}{h} - 0.07\left(\frac{t}{h}\right)^{0.222}\right]\left(\frac{h}{d}\right)^{1.34} \quad (7)$$

Eqs. (6) and (7) are a modification of Sakura's formulas [6]. They can even be extended to technology-independent capacitance evaluations.

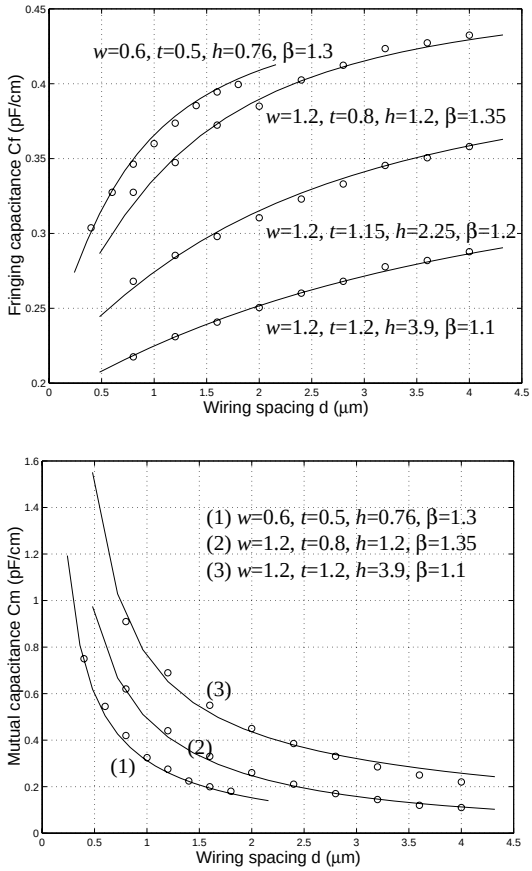

Figure3. Comparison of space-dependent fringing capacitance c_f and mutual capacitance c_m between model data (lines) and EM simulated data (circles) in three parallel interconnect lines.

Sakura's equations are well respected and have been widely used before. It is worth mentioning however that his equation, which he called the coupling capacitance, does not consider the charge proximity effect between the coupled wires and hence cannot be used directly. Careful checking with a field-solver reveals that this can result in as much as a four-fold error. For the same reason, his self-capacitance equation is also inaccurate when coupled wires are considered. However, the sum of

his self- and mutual capacitance terms is very accurate. In Eqs. (6) and (7) we have included the charge proximity effect. With Eqs. (1) to (7), we can hence estimate the parasites for any set of coupled wires. Fig.3 shows the estimated capacitance terms and the relevant curve fitting coefficients for some interconnect wires using these equations. For the geometry of most deep sub-micron interconnects, typical errors are less than 5% when compared with EM simulations.

We present comparisons between our interconnect model (called the RCL model hereafter), and two other models to verify its accuracy. A brief description of the different models is given below:

- *RCL model*
  The model of this paper, which consists of distributed LRC networks.
- *RCL(f) model*
  This model consists of distributed LRC networks, where the LRC parameters are extracted based on full wave analysis and hence include frequency dependent effects such as metal skin effect and substrate loss. This is the most accurate interconnect model today but very time-consuming [7].
- *RC model*
  This model is the same as the *RCL* model but without inductance. The model is less accurate but is widely used in state-of-the-art VLSI design.

We have analyzed signal coupling of two coupled 7mm-long global wires over which 100 higher level metal wires lay perpendicularly and evenly. In this example, an impedance-matched driver (46Ω in this case) drove the aggressor wire that was loaded by a CMOS inverter, while the victim conductor is almost floating. As shown in Fig.4, the new model shows improved accuracy compared with the conventional *RC* model and good agreement with the *RCL(f)* model. There is also good agreement with the simple RC representation when f < 1 GHz. At high frequencies, however, this results in an optimistic estimate, indicating the importance of incorporating the inductance in the model.

We have defined a saturated cross-talk between two parallel wires (wire *i* and wire *j*) that can be used as a reference in a rule-based model for a rough cross-talk estimation. The saturation cross-talk on wire *j* is given by [8]:

$$K_v = 20 \log\left((C_{ij})^{-1} \sum_{k=1}^{n} C_{jk} \right) (dB) \qquad (8)$$

where C_{ij} is the total mutual capacitance between wires *i* and *j*, and the sum in parenthesis is the total self-capacitance of wire *j*. This estimation can predicate the worst case cross-talk with reasonable accuracy as shown in Fig.4. However, due to the inductance effect, it is valid only when the driver impedance is equal or larger than the wire impedance Z_o. Fig.5 shows the influence of finite driver impedance on cross-talk where Z_s and Z_v represent the output impedance values of the drivers of the aggressor and the victim wires respectively.

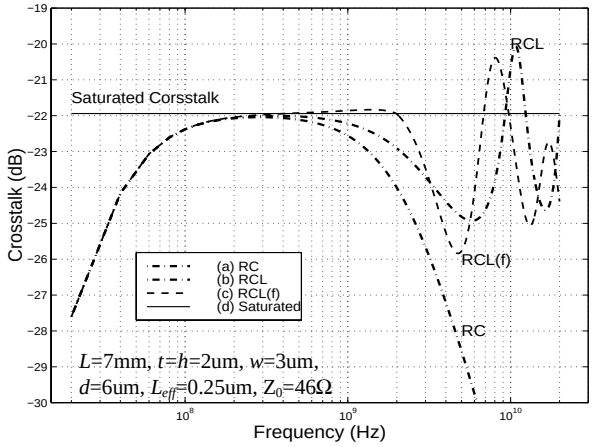

Figure 4. A comparison of crosstalk predicted by various interconnect models. (a), (b) and (c) overlap when f<300MHz. Driver impedances of the aggressor and the victim conductors are Z_0 and $100Z_o$.

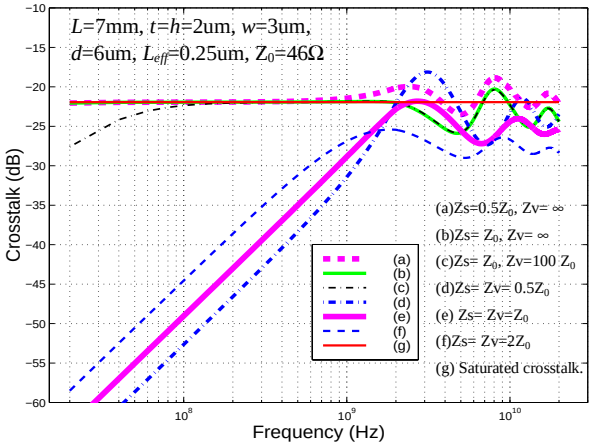

Figure 5. Crosstalk predications at various driver sizes for source and victim conductors using the multilevel interconnect model.

The model can also be applied in time-domain analysis. For example, we ran simulations on a 1.5 mm long bus in a hypothetical 0.05 μm process with a random data stream and obtained the eye diagram at the output. Fig. 6 (a) shows the case where the adjacent interconnect are grounded, essentially acting as shielding planes. A clearly defined eye opening is evident. Fig. 6 (b) shows the case where the adjacent interconnects carry their own data streams, each different from each other and that carried by the central interconnect. Now the eye opening has almost completely closed. If cross-talk is not taken into account in some way in the interconnect model, the resulting design will totally fail.

4. Signal propagation and timing evaluation

Interconnect delay increases quadratically with length on RC lines and linearly on LC lines. High-speed operation at GHz frequencies requires that the wires be optimized as faster LC responses. Theoretical analysis [9] shows that the critical wire length for LC behavior is given by :

$$L_c = 2th\left[(1+\alpha)\rho\sqrt{\varepsilon_k\varepsilon_0}cK_c\right]^{-1} \quad (10)$$

with α a ratio of return and signal path resistance and K_c a fringing factor. They are limited by the process parameters. Wires longer than L_c have the RC delay as the dominant delay.

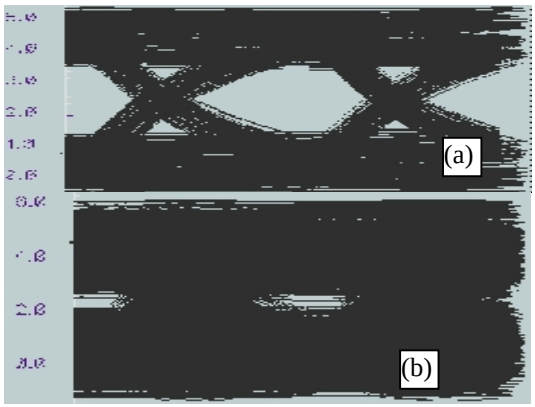

Figure 6. Eye diagrams for 1.5 mm long interconnect in a hypothetical 0.05 μm technology. (a)Adjacent interconnect grounded, (b) Adjacent interconnect carrying different data streams

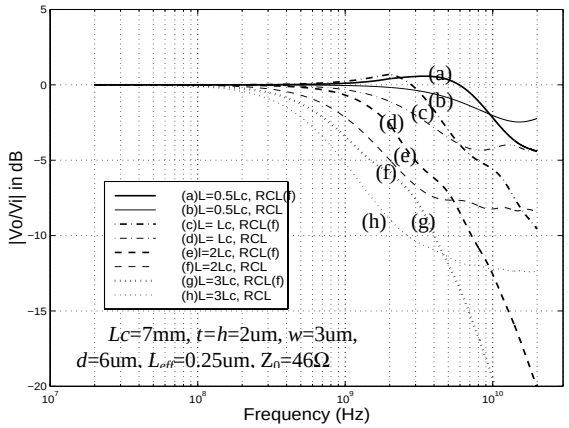

Figure 7. A comparison of frequency domain responses of signal propagation over interconnect lines using the *RCL(f)* model and the *RCL* model.

Frequency domain responses of signal propagation over interconnect lines with different lengths were analyzed using our model. A comparison between our model and the *RCL(f)* model is shown in Fig.7. In this figure, the driver has effective impedance of Z_o. Good agreement is evident up to frequencies of a few GHz. Shorter the line, the more accurate the prediction.

In order to see more clearly the impact on signal propagation, we present in Fig.8 the corresponding time domain response curves to a step with a 200ps rise-time. Typical error for delay prediction is less than 5% when $L=L_c$ but larger than 12% when $L=3L_c$. The rise time of the output signal is slowed down considerably when $L>L_c$. The results shown that when the new model is applied to signal delay estimation, it is accurate enough if $L<L_c$ and $t_r(t_f)>t_{tof}$ (the time-of-flight) compared with simulations based on the EM field solver. Fortunately, this would usually be the case for future VLSI design in CMOS at low giga-hertz clock frequencies, whereas the sophisticated *RCL(f)* model must be used for higher speed designs in BiCMOS and SiGe technologies.

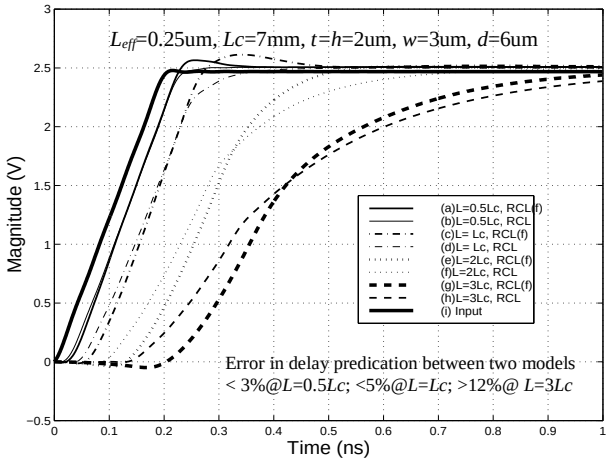

Figure 8. A comparison of interconnect delay using the *RCL* model and the *RCL(f)* model in time domain for different line lengths.

5. Conclusions

An accurate model for interconnect is of paramount importance in designing VLSI circuits in DSM. The usefulness of this model lies in its ability to represent all aspects associated with interconnect including in particular, crosstalk. We have presented a model that allows accurate pre-estimates of the behavior of interconnect in DSM for a design flow as in Fig.1(b). Because of the relative simplicity of this model when compared to EM field solvers, the simulation time of the circuit is much less. Though simple the model is accurate enough to result in a drastic reduction of the number of iterations through the design cycle, and hence total design time.

[1] K. L. Shepard, "The challenge of high-performance, deep-submicron design in a turnkey ASIC environment," in *Proc. of IEEE ASIC conference*, pp.183-186, 1998 .

[2] E. Chiprout, 'Hierarchical interconnect modeling', *Int. Elec. Dev. Meeting Techn. Dig.*, pp.125-128, 1997

[3] M. Lee, "A multilevel parasitic interconnect capacitance modeling and extraction for reliable VLSI on-chip clock delay evaluation," *IEEE JSSC*, vol.33, No.4, 1998

[4] J. H..Chen, J. Huang, L. Arledge, P.C.Li, and P. Yang, "Multilevel metal capacitance models for CAD design synthesis systems," *IEEE EDL*-13, pp.32-34, 1992

[5] E. T. Lewis, "An analysis of interconnect line capacitance and coupling for VLSI circuits," *Solid-State Electron*., vol.27, pp.742-749, 1984

[6] T. Sakura and K. Tamaru, " Simple formulas for two- and three-dimensional capacitance," *IEEE Trans. Electron Devices*, vol.ED-30, pp.183-185, 1983

[7] E. Chiprout, "Interconnect and substrate modeling and analysis: an overview," *IEEE J. Solid-State Circuits*, vol.33, no.9, pp.1445-1452, 1998

[8] L. -R. Zheng, H. Tenhunen, "Noise margin constraint for interconnectivity in deep submicron low power and mixed-signal VLSI circuits," *in Proc. ARVLSI*, pp.123-136, 1999

[9] L. -R. Zheng, B. X. Li, H. Tenhunen, "Global interconnect design for high speed ULSI and system-on-package," in *Proc. IEEE ASIC/SOC conference*, pp.251-256, 1999