On Signalling Over Through-Silicon Via (TSV) Interconnects in 3-D Integrated Circuits

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***Abstract*—This paper discusses signal integrity (SI) issues and signalling techniques for Through Silicon Via (TSV) interconnects in 3-D Integrated Circuits (ICs). Field-solver extracted parasitics of TSVs have been employed in Spice simulations to investigate the effect of each parasitic component on performance metrics such as delay and crosstalk and identify a reduced-order electrical model that captures all relevant effects. We show that in dense TSV structures voltage-mode (VM) signalling does not lend itself to achieving high data-rates, and that current-mode (CM) signalling is more effective for high throughput signalling as well as jitter reduction. Data rates, energy consumption and coupled noise for the different signalling modes are extracted.**

I. Introduction and related work

Three-dimensional (3-D) integration of circuits based on die and wafer stacking represents an opportunity to bypass the interconnect bottleneck commonly encountered in traditional scaling, while also allowing for integration of heterogeneous technologies [1]. The 3-D integration technologies that offer the most potential involve stacking at the wafer or die level, with interlayer interconnects being routed directly through the substrate and on-chip interconnect stack. The key performance benefit in 3-D ICs is provided by the reduced overall interconnect length and the electrical characteristics of TSVs, which are much faster than on-chip wires. In order to realise this potential, it is of paramount importance to maximise the data-rate over TSVs, as they are even more of a scarce resource than on-chip wires, especially as the number of dies in the stack grows. Therefore, it is imperative that signalling conventions for TSVs are tailored to their electrical characteristics, taking into account the low resistance and high coupling to other TSVs, which increase cross-talk on delay effects and adversely impact signal integrity (SI) as we show in a previous paper [2].

The majority of work published so far on TSVs in 3-D integration has focused on technological aspects and electrical characterization of isolated structures. An initial work that looks at SI effects in 3-D ICs is [3], which discusses crosstalk between interconnects on different layers within a 3-D IC for different substrate types. Pak et al. in [4] investigate the effect of TSV parasitics on data rate with increasing number of dies in the stack as well as material and structural parameter variations and the variation of crosstalk amplitude with different shielding arrangements within a densely packed arrangement of TSVs. In [5] inter-layer I/O circuits to cope with different parasitic loads in the TSV and microbumps and achieve optimum power and signal drive are discussed.

The analysis of signalling conventions for TSVs, which to the authors' best knowledge has not been addressed at all in the literature to date, is the topic of this paper; we examine voltage-mode (VM) and current-mode (CM) signalling techniques for TSVs in order to maximise data rate and preserve SI, and present results for a 65 nm technology based on Spice simulations. The TSV parasitics are extracted from a field solver, while device models are based on predictive technology parameters [6]. We show how CM signalling supports a higher data-rate and reduces jitter at the cost of increased energy consumption, and quantify the trade-off between energy and latency for these modes of signalling over TSV interconnects. The main contribution of this paper is in providing analysis results and design guidelines for signalling over TSVs, necessary for chip designers to better understand signal characteristics in 3-D ICs in the design planning phase.

In section II field-solver extracted parasitics for the TSVs are presented and used to propose an electrical model for delay and crosstalk estimation. Next the performance limitations and opportunities in VM signalling, including the judicious use of shielding is investigated. In section IV a simple CM receiver is employed in a TSV bus structure to show its potential for higher performance and improved SI in comparison to VM signalling. Design guidelines for the CM circuit are also proposed. Finally we present our conclusions.

II. TSV Parasitics and Electrical Model

For the purpose of extracting parasitics and subsequent analysis, a representative structure for a TSV is assumed to be a copper filled via with uniform circular cross-section and an annular dielectric barrier of SiO_2 with thickness 0.2 μm [7]. The dimensions vary depending on the process and application; we consider pitches of 25 μm and 35 μm in our study, well within the current capabilities of many processes [7], [8]. The cross-section is assumed to be uniformly circular, with a radius of 10 μm and length 50 μm. The substrate conductivity (σ) varies depending on the application, with values being typically around 10 S/m for RF processes, so that the relatively high resistance provides better isolation between

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σ (S/m)	pitch/(μm)	
	25	35
0	C_s=3.01fF,C_c=17.79fF L_s=17.13pH,L_m=23.27pH	C_s=2.85fF,C_c=8.90fF L_s=17.13pH,L_m=11.90pH
10	C_s=1.89fF,C_c=114.21fF L_s=17.13pH,L_m=23.27pH	C_s=3.37fF,C_c=88.57fF L_s=17.13pH,L_m=11.90pH
$100k$	C_s=564.81fF,C_c=0.04fF L_s=17.13pH,L_m=23.27pH	C_s=564.88fF,C_c=0.01fF L_s=17.13pH,L_m=11.90pH

TABLE I: TSV capacitances for different inter-via spacings and substrate conductivities ($R_{tsv} = 2.78m\Omega$)

components. However digital applications use a much more heavily-doped substrate, to ensure equipotentiality throughout the bulk substrate as much as possible, reducing the possibilities of latch-up [9]. In this work we have considered three different substrate conductivities: 100 kS/m, 10 S/m and zero, representing typical values used in digital and RF processes and a hypothetical highly resistive substrate respectively. The topology considered is three parallel coupled TSVs, a representative unit of any size row of TSVs. A field solver has been used to extract the electrical parameters (*resistance R, capacitance C and inductance L*) in the context of the equivalent circuit shown in Fig. 1.

The extracted parasitics for the structure of Fig. 1 are given in Table I. It can be seen that when the substrate conductivity is very high (i.e. a heavily-doped substrate) the total capacitance is the highest, with the majority of the capacitance being to ground, as can be expected since the substrate voltage is very nearly at 0 V. For a highly resistive substrate, the capacitance is the lowest, but the coupling component dominates, being 3 to 6 times greater than the self component. For a lightly-doped substrate, the total capacitance is in between these values, but the ratio of coupling to self capacitance is even higher, 60 and 90 for the different pitches. The *R* and *L* values of the TSV including the mutual component are not affected at all by substrate conductivity and can be estimated from the compact models proposed in [2], while the capacitive models proposed there can be used for highly resistive substrates.

In order to identify the appropriate electrical model for a TSV, we carried out simulations to determine the relative contribution of the *R*, *C* and *L* parasitic components of the TSV to the shape of the output waveform in typical delay and SI calculations. The driver and receiver are CMOS inverters implemented in a representative 65 nm technology through the use of predictive parameters [6]. In the simulations the TSV model was driven by an inverter sized to be 50$\times$ a minimum-sized inverter, and loaded by a minimum-sized inverter. In a

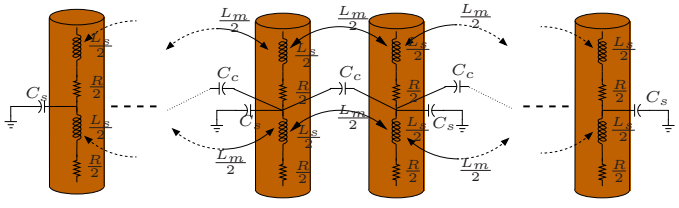


Fig. 1: Electrical model of coupled TSVs

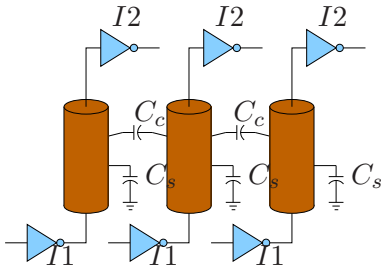


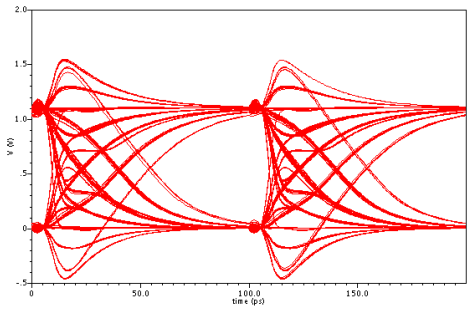
Fig. 2: Simulation setup to investigate effect of crosstalk

minimum-sized inverter the NMOS and PMOS transistors have channel lengths of 65 nm, and widths of 1.5$\times$ and 2.3$\times$1.5$\times$ the channel length respectively, with 2.3 being the n-type to p-type mobility ratio. The supply voltage for this technology is 1.1 V. The output waveform was simulated while sweeping the entire range of R, L and C values as determined by the field solver including any potential increments in resistance due to the skin effect. For rise times down to 1 ps, no discernible change could be observed when varying the inductance. Varying the capacitance revealed a significant spread in the 50% latency of the output waveform [10]. Simulations also reveal that over the entire considered range of TSV dimensions and substrate conductivities, the effect of inductive coupling on the victim net is not large enough to justify the modelling of parasitic mutual inductance in a three-parallel TSV system (Fig. 1) for delay and SI calculations. Capacitive coupling however needs to be considered at the outset. Therefore the simulation model for coupled TSVs reduces to a network of coupled capacitors representing self- and mutual-capacitances.

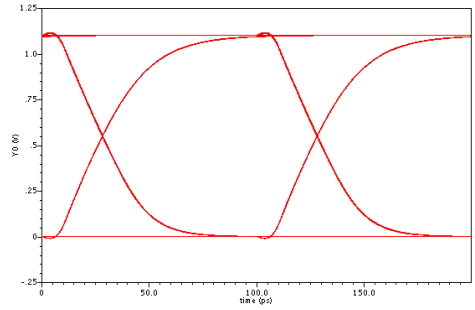
III. Voltage-Mode (VM) Signalling and Shielding

A simulation setup as shown in Fig. 2 was used to analyse the SI effects in VM signalling over TSVs. All TSVs (victim and aggressors) are driven by a 50$\times$ inverter (*I1*) and loaded by a minimum-sized inverter (*I2*). The victim and aggressor drivers were driven by pseudo-random bit sequences with rise/fall time and period of 10 ps and 200 ps respectively, and the resultant eye-diagram is plotted in Fig. 3(a). In this particular case the delay varies between 8 ps and 55 ps. As the TSV resistance is several orders of magnitude less than the output impedance of the driver, the TSV capacitance dominated by the coupling component dictates the delay.

Shielding is widely used in bus structures to alleviate crosstalk and consequent coupled noise and delay variation in interconnects, ideally by judiciously interspersing power and ground conductors with signalling conductors where possible. Shown in Fig. 3(b) is the eye diagram at the output when both neighbouring TSVs act as shields; the delay variation is eliminated. While shielding eliminates cross-talk to adjacent TSVs and reduces latency, its cost is reduced overall utilisation of TSVs, as every signal via cannot always be routed between power/ground lines. As we quantify in Table II, the improvement in latency is not sufficient to ensure a nett gain when considering an area-limited TSV resource.



(a) Without Shielding



(b) With both neighbours shielded

Fig. 3: Eye diagram at far-end of TSV for a pseudo-random bit sequence when $C_s = 3f$ and $C_c = 89fF$.

IV. Current-Mode (CM) Signalling

A circuit schematic of a basic CM signalling link is shown in Fig. 4 [11]. The driver is a typical inverter, but the receiver is composed of NMOS (*MN2*) and PMOS (*MP2*) transistors with drain and gate shorted so that they act as active load resistors connecting net *TSV_out* to ground and V_{dd} respectively. The inverter formed by *MN3* and *MP3*, *INV3*, restores rail-to-rail output. The receiver transistors (*MN2* and *MP2*) act as a voltage divider and the output voltage at the far end of the TSV changes between two levels dictated by the driver and termination resistances, as the input switches between logic 1 and 0. As the termination resistance approaches infinity, i.e. the receiver becomes a simple inverter, the swing becomes rail-to-rail and the system reverts to VM signalling. The speed improvement of CM signalling is due to the reduced swing, which results in less time being taken to charge and discharge the interconnect capacitance.

The design criteria to achieve functionality of this CM

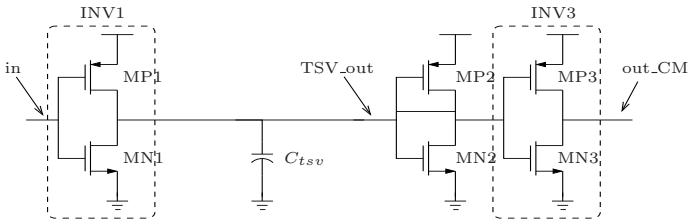


Fig. 4: Current-Mode (CM) signalling link

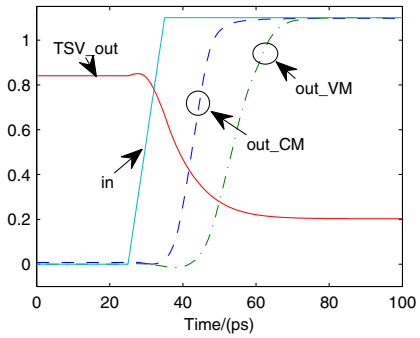
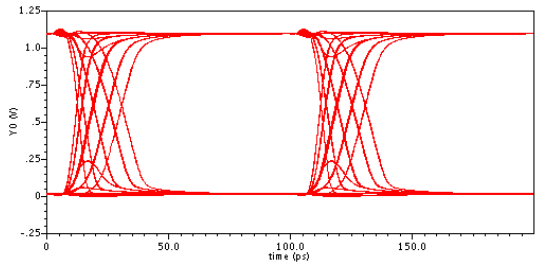


Fig. 5: Output voltage waveforms for the CM link shown in Fig. 4 and comparable VM link with $C_{tsv} = 100fF$ and $H_d = H_r = 50$

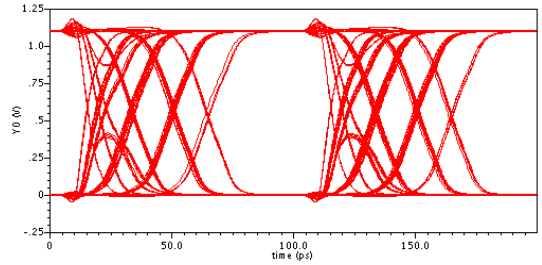
receiver is that sizing of the termination transistors and *INV3* should be carried out so that the reduced voltage swing is sufficient to switch *INV3*, providing rail-to-rail signal swing on net *out_CM*. Fig. 5 shows the input and output voltage waveforms of the CM link depicted in Fig. 4 with driver size H_d =50. Shown in the same plot is the output of a comparable VM link. In order to be able to compare between different signalling systems, the VM signal link comprises the same circuitry as the CM link except for *MN2* and *MP2*; the output after *INV3*, is called *out_VM* in this instance and plotted in the figure. The simulation results reveal that the CM link is 50% faster than the VM link.

In order to see the effect of coupling in CM signalling, a CM link flanked on either side by identical CM signalling links has been simulated. In CM signalling the coupled noise voltage on a silent victim discharges from both the receiver and driver side whereas in VM it discharges only from the driver side. Therefore the termination resistance (size H_r defined in terms of multiples of minimum sized devices) affects the coupled noise amplitude and pulse width. Increasing H_r from 5 to 50 reduces the noise amplitude from 0.47 V to 0.22 V. As the coupled noise in the VM link is 0.61 V, a 20% reduction in crosstalk noise can be observed with CM signalling. Fig. 6 shows the eye diagrams of the output after *INV3* for CM and VM signalling links. As can be seen, CM signalling reduces delay variation or jitter by approximately 50%.

The CM delay can be further reduced through reduction of the termination resistances (by increasing the size of *MN2* and *MP2*), which reduces the swing of the signal at the input of *INV3*. However there is a limit defined by the point at which the low voltage swing is inadequate to drive *INV3* to restore rail-to-rail swing; for $H_d = 50$, this limit is $H_r \leq 52$. Moreover, increasing H_r causes the static power dissipation to increase, as it creates a low resistance current carrying path from the supply rail to ground. This trade-off has been quantified in Fig. 7, where the worst-case delay and average energy consumption per cycle for CM signalling has been normalised to the worst-case delay and energy consumption in VM signalling.



(a)



(b)

Fig. 6: Eye diagrams for (a) CM and (b) VM after INV3, with $H_d = 50$, $H_r = 50$,$C_s = 3f$ and $C_c = 89fF$.

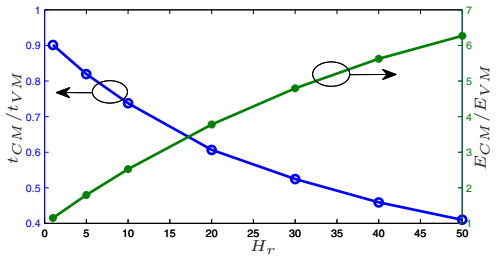


Fig. 7: Trade-off between worst-case latency and energy for CM signalling normalised to the values achieved by a comparable VM link.

A fair metric for comparison between the different signalling strategies we have examined is the data rate per unit area, defined by:

$$\text{Data rate} = \frac{1}{t_d}\frac{N_s}{N_T}, \tag{1}$$

where t_d is the worst-case delay, N_s the number of signal TSVs, and N_T the total number of TSVs (i.e. signal and shield lines). In the data rate analysis we have considered four parallel TSVs as a representative unit to compare the following signalling strategies: VM without shielding, VM with every other TSV being a shield (i.e. a pattern of ground-signal-ground-signal or GSGS), and CM with different receiver terminations. The results are given in Table II, which summarises the maximum achievable data rates as well as energy consumption per cycle.

V. Conclusions

In this work we have considered a host of signalling techniques including combinations of shielding, optimal VM signalling and CM signalling, and made a comparison using data-rate as a metric, in order to understand how to maximise it within the constraints of energy and area budgets. We have shown using realistic values for TSV parasitics and device models for a representative 65 nm technology that CM signalling is the most effective in mitigating coupled noise and provides a higher data-rate with a receiver circuit that has only two extra transistors. The cost of reduced latency and improved noise resilience is static power dissipation, which trade-off has been quantified, in order to aid the task of maximising data-rate within power and energy constraints.

		Data rate /(Gbps)	Norm. Energy/bit	Peak Noise /(mV)
VM	SSSS	18	1	612
	GSGS	17	1	0
CM	$H_r = 5$	20	1.8	471
	$H_r = 10$	22	2.52	427
	$H_r = 20$	27	3.78	357
	$H_r = 30$	31	4.80	303
	$H_r = 40$	36	5.63	259
	$H_r = 50$	40	6.27	220

TABLE II: Data rate per TSV and energy consumption for VM and CM signalling techniques

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