Exploration of Through Silicon Via Interconnect Parasitics for 3-Dimensional Integrated Circuits

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***Abstract*—This article discusses results from simulations of signaling in Through Silicon Vias (TSVs) with an emphasis on latency and signal integrity effects. Data from field solver simulations is used for TSV parasitics and employed in SPICE simulations. A reduced electrical circuit is proposed for lone TSVs as well as bundled structures and switch-factor based delay models are derived to calculate rise times in a 3x3 bundle. Furthermore Signal Integrity (SI) issues in coupled TSVs are briefly discussed.**

I. Introduction

3-D integration is a promising new technology that is currently being developed by a number of organizations worldwide. Circuits are stacked at the wafer, die, chip or package level to decrease the footprint, increase speeds, and allow for integration of various technologies on one chip, among other potential improvements [1]. One viable solution to provide connectivity between the layers is the Through Silicon Via (TSV). Holes are etched in the silicon and filled with copper surrounded by an adhesive layer and a dielectric barrier. TSVs can be implemented down to a diameter of less than 5µm and densities are currently increasing up to 1000 I/Os per device [2]. As limitations on wire bonding interconnects are becoming apparent in recent chip designs with increasing numbers of layers, the TSV provides an enticing alternative to 3-D stacking interconnects.

As the use of TSVs is a fairly recent concept, their effects on signaling within a 3-D circuit are not well documented. It is the goal of this paper to provide a preliminary assessment of the effect a TSV has on signal integrity within a realistic context. Using circuit models derived from field solver simulations [3], the parasitic effects of TSVs in various configurations and sizes can be simulated within a SPICE engine. As 3-D Integration is coming closer to the implementation phase, it is necessary for chip designers to better understand signal characteristics in TSVs to expedite the design process.

Explorations into signal effects caused by TSV parasitics are not widely covered in literature. There are several examples of TSV explorations such as an investigation into propagation delay in [4] and a further examination of parasitic modeling [5], [6], but to the authors' knowledge, comprehensive simulations for TSVs in a bundle have not been published and useful models for calculations of delay, SI and Power Integrity (PI) have not been widely released.

The organization of this paper is as follows: In section II, the trends associated with lone and bundled TSV parasitics are described and an appropriate equivalent electrical circuit is discussed. Next, the parasitic properties of the TSV are tested for their significance and a reduced order model is proposed. Section III examines the effects of parasitic crosstalk between TSVs in a 3x3 bundle and switch-factor based delay models that capture the effect of crosstalk on signal latency are presented. Section IV discusses Signal Integrity issues in a bundle, such as the effect of using grounded TSVs as shields, and finally section V ends with our conclusion.

II. TSV Parasitics

In order to investigate electrical properties for TSVs within a bundle, field solver simulations were carried out to determine parasitic and coupling values for realistic geometrical configurations. The equivalent electrical circuit diagram for a TSV is as shown in Figure 1. This is a conventional T-model wire segment including parasitic resistance, inductance and capacitance to ground as well as capacitive and inductive coupling to a neighboring TSV.

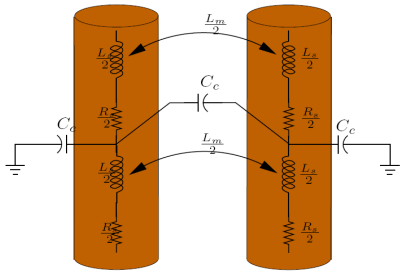

Figure 1. TSV Electrical Equivalent Circuit

The parasitics were extracted for TSV structures with radii of 5-40µm and lengths of 20-140µm. Mutual capacitance and inductance values were extracted for the same geometrical structures, with TSV pitches ranging from 50µm to 260µm in a 3x3 bundle. As with on-chip interconnects, the trends for wire capacitance, inductance and resistance are largely the same for TSVs. As the length of the via increases, resistance, capacitance and inductance also increases. As the width increases, the capacitance goes up but the inductance and resistance decrease. The capacitive parasitic terms in different sized bundles of TSVs are visible in the plots shown in Figures 2, 3 and 4.

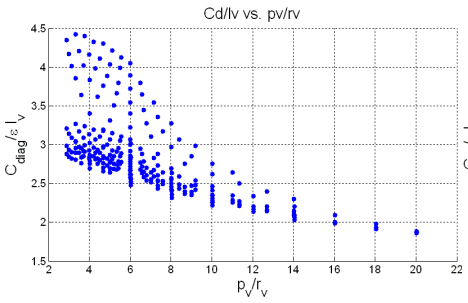

Figure 2. C_{diag}/l_v vs P_v/r_v

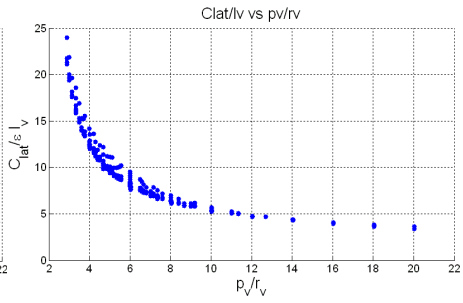

Figure 3. C_{lat}/l_v vs P_v/r_v

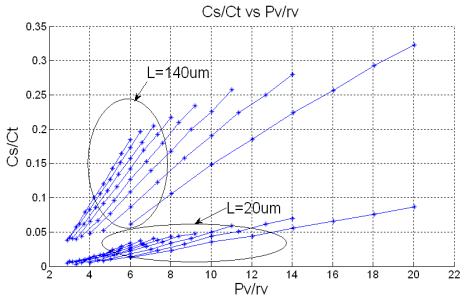

Figure 4. Cs/Ct vs Pv/rv

In all simulations displayed in this paper employing the circuit diagram in Figure 1, the TSV model was driven by an inverter size of 10 and loaded by a minimum sized inverter in 0.35µm technology. The driver was found to be the optimum size, given the TSV parasitics, by a series of sweeps and the minimum-sized inverter represents the pin load for each vertical interconnect. A 50ps rise time was employed throughout all of the simulations.

A. Significance of RLC Parasitics

Simulations were performed for the entire range of resistance, inductance and capacitance values as determined by the field solver. The resistance was swept from 0-500mΩ, and the output waveforms were plotted to observe variations in delay. As can be seen in Figure 5, the TSV resistance within the considered range of is so small that it has no observable effect on the output waveform. The inductance was then swept from 0-500pH, the extracted range, for rise times down to 1ps, revealing no significant contribution as seen in Figure 6. Finally, the capacitance was swept from 0-500fF showing a significant effect on latency of the output waveform, as seen in Figure 7. These results appear to show that the electrical model for a cylindrical TSV can be reduced to a purely capacitive model. The resistive and inductive parasitics are small enough to be neglected in any delay simulations, which reduces the complexity of the electrical model significantly.

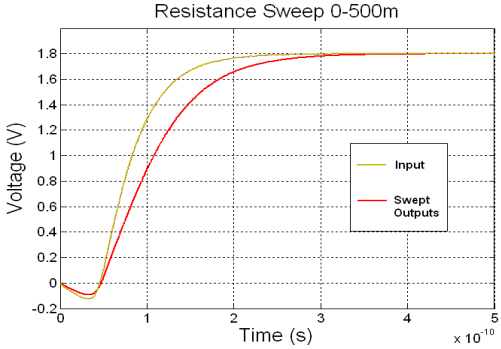

Figure 5. Resistance Sweep

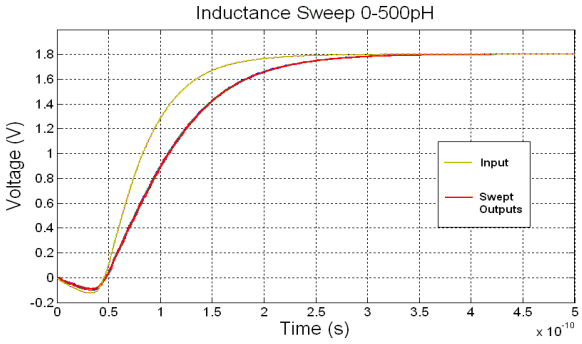

Figure 6. Inductance Sweep

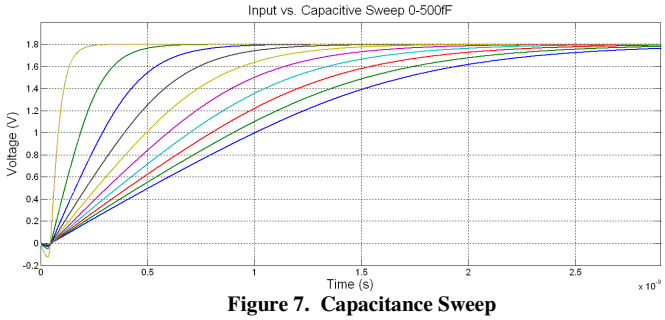

Figure 7. Capacitance Sweep

B. Distributed vs lumped model

In addition to parametric sweeps, simulations were conducted to determine if distributed models were necessary to attain accurate results. The model was segmented into 2, 5, and 10 sections and output waveforms examined to show no significant effect on the signal from increasing the number of segments within the parasitic range determined by the field solver. The relatively low resistive and inductive terms reduce the necessity for a distributed model for simulation of signals within the considered range.

III. CROSSTALK IN A 3X3 TSV BUNDLE

This section investigates the effects of crosstalk between TSVs organized in a 3x3 bundle. By employing electrical models derived from the field solver simulations, various switching patterns are simulated to analyze crosstalk effects between these structures. The coupling capacitance between two TSVs is a function of radius, length and inter-via spacing, as well as dielectric barrier thickness and permittivity, and increases monotonically with increasing radius and decreasing spacing. As capacitive and inductive coupling can have detrimental effects on bandwidth and signal integrity, the crosstalk between adjacent structures must be examined to determine the most efficient use of area and TSV sizing to maximize signal throughput and reliability.

As in the on-chip case, the capacitive coupling terms to nearest neighbors dominate over the coupling terms to non-adjacent lines, which are mostly insignificant. Within the set of nearest neighbors the lateral terms are more significant than the diagonal terms. This is observable in Figure 8 and is due to the fact that the diagonal neighbors are partly shielded by the lateral conductors and the non-adjacent lines are almost completely shielded by the ring of adjacent lines.

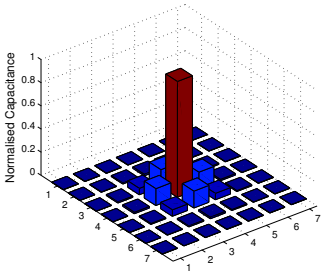

Figure 8. Mutual Capacitance

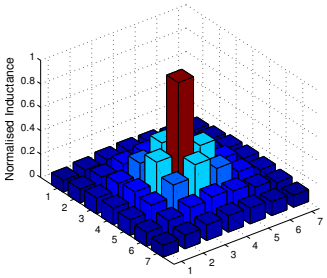

Figure 9. Mutual Inductance

In the case of inductance, the coupling is significant within the entire bundle because magnetic field lines tend to permeate the length and breadth of the global structure, again analogous to the on-chip case. This relationship can be observed in Figure 9.

The first simulations performed determine the individual contributions of mutual inductance and capacitance terms when 8 aggressors switch simultaneously on a silent victim net. For up to twice the maximum mutual inductance extracted by the field solver for the considered range, the coupling turns out to be insignificant for rise times down to 1ps. This is born out in Figure 10, which shows minor oscillations near the aggressor transition points. The capacitive coupling on the other hand is significant with a coupled noise amplitude of up to 15% of Vdd. Figure 11 shows a subset of waveforms within the considered geometrical range, illustrating this.

The effect of inductive coupling on the victim net does not appear to be large enough to justify the modeling of parasitic mutual inductance in a 3x3 bundle for signals. It is however possible that the simultaneous switching of many different aggressors, including non-adjacent ones in a larger bundle, can produce a more significant effect. This is due to the inductive coupling having measureable effects over a long range. Capacitive coupling however needs to be considered at the outset. Simulations were performed for a variety of TSV geometries and pitches to provide a clearer picture of the capacitive crosstalk within a 3x3 TSV bundle. Simulations were performed to highlight the effect of crosstalk on delay in a bundle when the 8 surrounding TSVs remain quiet, switch in the same direction and in the opposite direction.

The simulation result demonstrates significant crosstalk on delay effects in spite of the relatively low interconnect density. For example, within a TSV bundle with a pitch of 100µm and lengths and radii of 20µm and 40µm respectively, the 50% delay of the victim, 393ps, is greater than that for an isolated TSV, 157ps. For the selected geometrical configuration, the delay variation between best-case and worst-case switching patterns was 36ps to 135ps, a 4-fold difference over the minimum delay. As the interlayer connectivity in a 3-D IC has to be achieved by a high dimensional TSV bundle accounting for coupling effects will become paramount in designing high performance, reliable systems.

A. *Predicting delay in a TSV bundle*

Given that the investigations reveal a lumped capacitive equivalent circuit as being sufficiently accurate, the switching pattern dependant delay within a bundle can be accurately captured by a first-order Elmore delay model. For the entire range of geometrical configurations considered, the delay can be accurately estimated by (1) where the empirically determined switch factors for the various switching patters are defined in Table 1. Here C_s is the self capacitance, C_l the lateral coupling capacitance, C_d the diagonal coupling capacitance and R_D the driver resistance.

$$t_d = 0.69R_D(C_s + K_1C_l + K_2C_d) \quad (1)$$

Switching Pattern			K_1	K_2
Victim	**Lateral**	**Diagonal**		
↑	↑	↑	0	0
↑	→	→	3.4	5.2
↑	↓	↓	9.0	10.6

Table 1. Switch Factors for Delay Estimation

The minimum accuracy of this equation over the entire range was greater that 92%, principally due to the negligible parasitic resistance inherent in the TSV. These switch-factor-based delay equations facilitate the integration of TSV interconnects into established on-chip static timing methodology.

IV. SIGNAL INTEGRITY SIMULATIONS

In order to fully capture the effect of crosstalk on delay and coupled noise amplitude under real-world conditions, simulations were carried out with pseudo-random bit streams (PRBS) at the victim and aggressor inputs in a 3x3 bundle to generate the eye diagrams at the output. All drivers were size 10 inverters while every TSV was loaded with a minimum-sized inverter. The example geometry chosen was a bundle with radii, length and pitch of 15µm, 20µm, 50µm respectively.

The eye diagram in Figure 12 shows the response of the victim line when the PRBS speed is 10 GBPS with signal rise and fall times of 10ps. It is clear that the eye is very narrow and the variation in delay has widened to

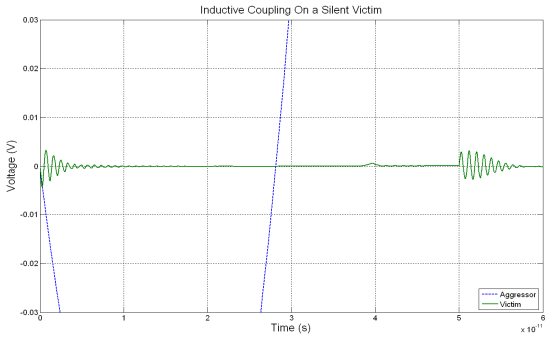

Figure 10. Inductive Contribution

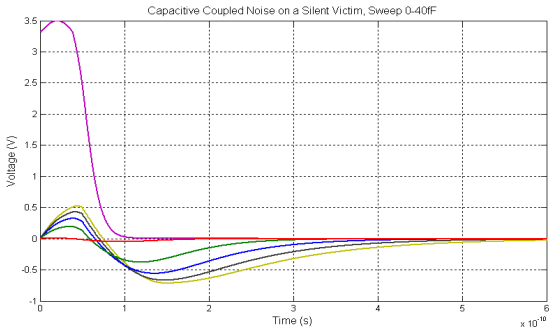

Figure 11. Capacitive Contribution

an unacceptable level. At this speed the crosstalk completely overpowers the signal on the victim.

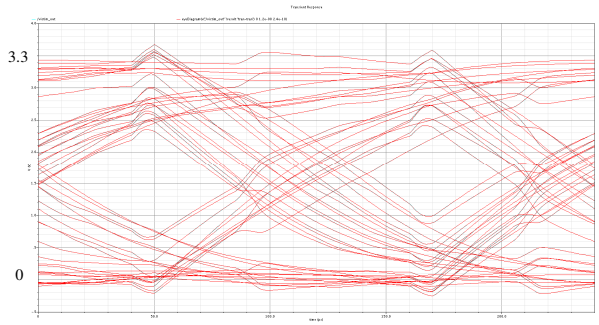

Figure 12. 10GBPS Victim Eye

Since the lateral (Northern, Southern, Eastern, and Western) neighbors in the bundle contribute the majority of the capacitive coupling, an obvious strategy to counteract capacitive crosstalk at high signaling speeds is to use these lines as shields. As seen in Figure 13, this effectively eliminates the majority of the coupling and allows for higher bit rates through the interconnect.

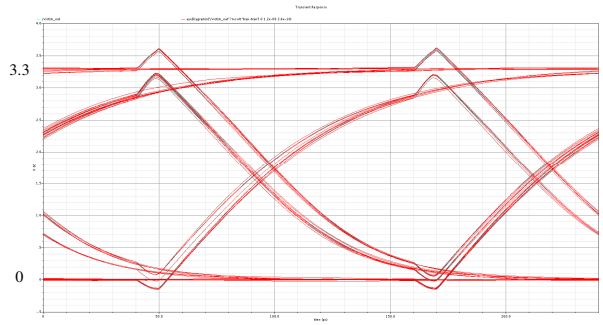

Figure13. 10GBPS Victim Eye Shielded

It is clear that that judicious shielding has opened up the eye and reduced the delay variation significantly. The main drawback to this method is that although higher bit rates can be achieved, significant area loss occurs due to the unusable grounded lines. Investigation into optimal configurations for TSV sizing, spacing and shielding has to be performed to determine best configuration for the highest bandwidth achievable in a 3-D device.

V. CONCLUSION

TSVs represent an important interconnection option for 3-D ICs but have not received significant attention in the literature with regard to their signaling characteristics. In this paper, parasitic extraction has been carried out using a field solver for typical geometrical configurations achievable in current processes in order to examine their variation with physical dimensions and carry out delay and signal integrity explorations. As suggested by field theory the significant capacitive coupling terms in a bundle are restricted to nearest neighbors, while the mutual inductance terms are significant throughout the bundle.

For the considered range, simulations show that resistance and inductance are mostly negligible for latency and SI considerations and therefore signal propagation through an isolated TSV as well as a TSV in a bundle can be analyzed by considering the capacitance alone. Tests were also carried out to determine if the via should be treated as a lumped or distributed model. The results show that no benefit is conferred by considering a distributed model due to the relatively low resistance and a single lumped section is sufficiently accurate.

Furthermore, crosstalk effects between TSV structures in a 3x3 bundle were examined. Capacitive crosstalk is far greater than inductive crosstalk, such that inductance can be ignored in most cases. Due to the reduced complexity of the TSV electrical model as proposed in this paper, simplified delay formulae based on the Elmore delay and empirical switch factors were proposed to estimate delay in a TSV bundle with a maximum error contained to within 8% over the entire simulated range. These equations allow for preliminary assessment of delay for worst, nominal and best case switching scenarios in accordance with well-established timing analysis practice. Finally, simulations were carried out using eye diagrams to further investigate SI issues, demonstrating the effect of capacitive coupling in a TSV bundle with random switching patterns. Shielding the lateral TSVs in a bundle was shown to increase signal reliability and allow for faster speeds through the structures. It is expected that this study will provide the basis for further explorations through the recommendation of the equivalent circuits as well as the investigations on the relative importance of the various parasitic terms, providing insight into signaling schemes over TSV interconnects.

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