Input Admittance Analysis of SEPIC Power Factor Correction Grid-Connected Rectifier

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***Abstract*—This paper validates the input admittance of a SEPIC power factor correction (PFC) rectifier derived from an average model and a switching model. The SEPIC PFC rectifier is implemented and analyzed using both switching and average models in accordance with the specifications provided. PR and PI controllers are integrated into both models to evaluate their performance in regulating the input current and output voltage. A frequency response estimation method is employed to characterize the input admittance, applying small-signal perturbations to determine the system's behavior over a broad frequency range. The results from the switching model show strong agreement with the average model for the input admittance, thereby validating the theoretical models. The open-loop input admittance exhibits three resonances at specific frequencies due to system dynamics, while the closed-loop configurations demonstrate variations in resonance and inductive behavior depending on the controller used. The findings indicate that the SEPIC PFC rectifier maintains external stability across both open- and closed-loop configurations when the parameters and controllers are appropriately designed. These results provide valuable insights into the design and control of SEPIC converters for power factor correction applications.**

***Index Terms*—Input admittance, power factor correction rectifier, SEPIC converter, frequency response.**

I. Introduction

Rectifiers, also known as AC-to-DC converters, are power conversion devices commonly used to interface DC loads, such as data centers, with the AC micro-grid system shown in Fig. 1(a). By ensuring efficient and reliable power conversion, rectifiers play a crucial role in delivering the stable DC power required by these loads. The stability of rectifiers can be categorized into two types: internal stability and external stability. Internal stability refers to the control loops within the rectifier, specifically those managing the DC-link voltage and the power factor correction (PFC). These control loops ensure that the rectifier operates efficiently and maintains the desired performance under varying load conditions.

External stability, on the other hand, refers to the interaction between the rectifier and the AC network to which it is connected [1]. This is often termed impedance stability, as it focuses on the compatibility between the rectifier's impedance and the AC network impedance. Maintaining external stability is essential to avoid input current oscillations, waveform distortion, and degraded power quality or instability in the

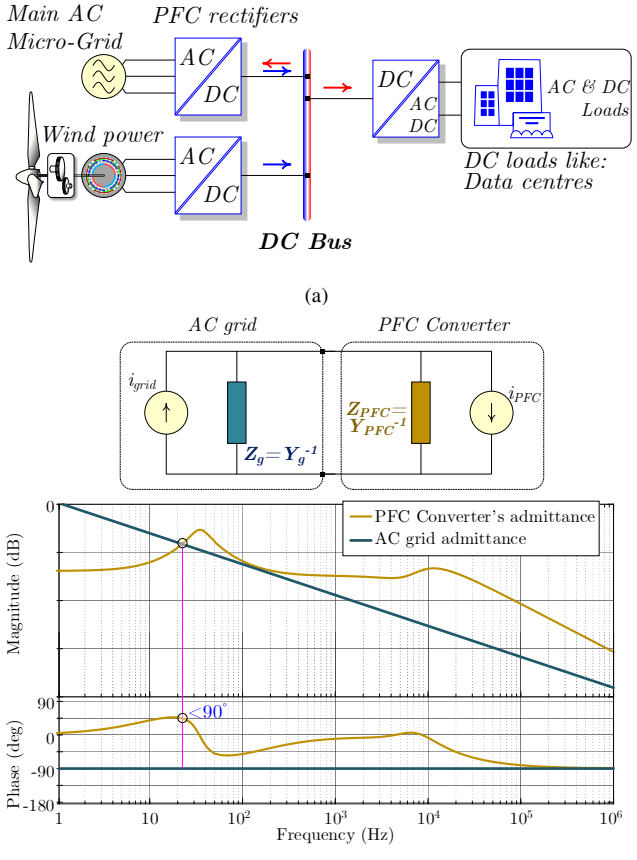


Fig. 1. (a) Micro-grid and (b) Admittance of grid and converter.

converter [2]. The stability of a grid-connected PFC converter depends on the interaction between its input admittance (Y_{PFC}) and the grid admittance (Y_g) as shown in Fig. 1(b). For the system to remain stable, Y_{PFC} must exhibit passive behavior, meaning its real part should remain nonnegative across all frequencies, and its angle must remain within $\pm 90°$. This ensures that the PFC behaves as an energy-dissipating or storing element. Instability can arise if Y_{PFC} becomes nonpassive, with a negative real part at certain frequencies, particularly if it intersects with Y_g in this region. Such an intersection can lead to oscillations and destabilize the PFC-grid system, highlighting the importance of maintaining a passive input admittance profile for the PFC converter. By analyzing the admittance characteristics of rectifiers, effective control systems can be implemented to maintain stability under varying load and input conditions [3], [4].

In PFC rectifiers, the relationship between the input voltage and the input current is inherently nonlinear due to the nature of the converter model, PFC, DC-link, and PLL control loops.There are two primary approaches to modeling the input impedance of a converter:

- Linear Time-Invariant (LTI) Modeling: This method involves linearizing the converter model in the frequency domain and transforming the system into the synchronous reference frame. It assumes steady-state DC operating points for analysis, making it well suited for symmetric three-phase systems. The LTI approach simplifies the dynamics by treating the system as time-invariant, which helps in understanding its behavior under small perturbations.
- Linear Time-Periodic (LTP) Modeling: Unlike LTI, the LTP approach incorporates harmonic linearization, which accounts for the periodic nature of converter systems. It examines the system's response to sinusoidal perturbations, capturing the effects of harmonics more accurately. This approach is particularly useful for systems where periodic switching or modulation introduces harmonics, as it provides a more detailed understanding of the system's dynamic behavior [5], [6].

Several studies have analyzed the impedance characteristics of boost PFC rectifiers [7]–[11], focusing on their performance and stability. However, a limitation of boost converters is that they operate exclusively in step-up mode, meaning they can only increase the input voltage. This restricts their versatility in applications that require both step-up and step-down voltage capabilities. In contrast, rectifiers that can operate in both step-up and step-down modes, such as the SEPIC converter, provide greater flexibility and are suitable for a wider range of applications, making them more advantageous in certain scenarios [12]–[17]. Despite their advantages, these rectifiers have not yet been thoroughly analyzed in terms of input impedance stability, highlighting a gap in the analysis of other converter types.

This paper analyzes the input impedance stability of the SEPIC PFC converter in both open-loop and closed-loop operations. The average model of the SEPIC rectifier is derived by linearizing the system and obtaining the transfer function that relates the input current and voltage. The input admittance of the switching model is then derived by applying a perturbation signal to the input voltage. Both models are analyzed under various conditions: without a control system (open loop), with the inner current control loop, and with both the inner current control loop and the outer DC-link voltage control loop. Finally, the input admittance is validated by comparing the results of both models.

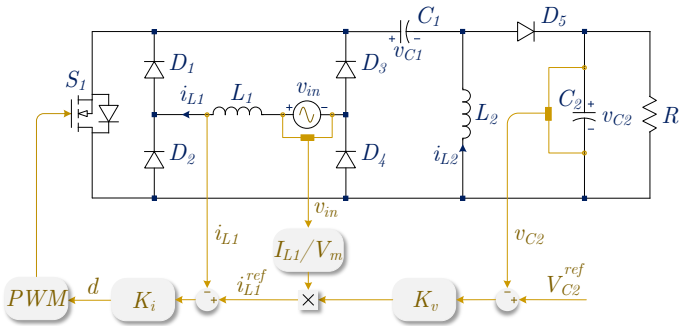


Fig. 2. Closed-loop model of the SEPIC PFC converter with a current PR controller and a DC-link PI controller.

The paper is divided into sections, including modeling the SEPIC PFC rectifier (II), deriving the average model of input admittance from the open-loop and closed-loop systems (III), confirming the average model of input admittance by switching model results (IV), and conclusion (V).

II. Modeling of SEPIC PFC Rectifier

The dynamic model of a SEPIC converter is crucial for designing an effective controller and analyzing impedance stability, ensuring that the rectifier remains stable under various operating conditions and disturbances.

To derive the dynamic model of a SEPIC converter, the following steps are required.

A. Nonlinear average model of the circuit

The SEPIC rectifier shown in Fig. 2 exhibits two switching states when operating in Continuous Conduction Mode (CCM). Therefore, by applying KVLs and KCLs the average model of SEPIC converter can be given as:

$$\begin{cases} L_1 \dfrac{di_{L1}}{dt} = D.v_{in} + (1-D)(v_{in} - v_{C1} - v_{C2}) \\ C_1 \dfrac{dv_{C1}}{dt} = -D.i_{L2} + (1-D)i_{L1} \\ L_2 \dfrac{di_{L2}}{dt} = D.v_{C1} + (1-D)(-v_{C2}) \\ C_2 \dfrac{dv_{C2}}{dt} = -D.\dfrac{v_{C2}}{R} + (1-D)(i_{L1} + i_{L2} - \dfrac{v_{C2}}{R}) \end{cases} \tag{1}$$

where L_1 and L_2 refer to inductors 1 and 2, while C_1 and C_2 represent capacitors 1 and 2. The duty cycle is denoted as D, and v_{in} represents the input voltage. The resistive load is characterized by R.

The current through L_1 is denoted by i_{L1}, and the current through L_2 is represented by i_{L2}. Similarly, the voltages across C_1 and C_2 are denoted by v_{C1} and v_{C2}, respectively.

B. Linearization

Substituting the dc part, X, and the ac part, $\hat{x}$, (where $x = X + \hat{x}$) into equation (1), the result can be calculated as:

$$\begin{cases} L_1 \dfrac{d(I_{L1}+\hat{i}_{L1})}{dt} = \\ \quad V_{in}+\hat{v}_{in}-(1-D-\hat{d})(V_{C1}+\hat{v}_{C1}+V_{C2}+\hat{v}_{C2}) \\ C_1 \dfrac{d(V_{C1}+\hat{v}_{C1})}{dt} = \\ \quad -(D+\hat{d})(I_{L2}+\hat{i}_{L2})+(1-D-\hat{d})(I_{L1}+\hat{i}_{L1}) \\ L_2 \dfrac{d(I_{L2}+\hat{i}_{L2})}{dt} = \\ \quad (D+\hat{d})(V_{C1}+\hat{v}_{C1})+(1-D-\hat{d})(-V_{C2}-\hat{v}_{C2}) \\ C_2 \dfrac{d(V_{C2}+\hat{v}_{C2})}{dt} = \\ \quad -\dfrac{(V_{C2}+\hat{v}_{C2})}{R}+(1-D-\hat{d})(I_{L1}+\hat{i}_{L1}+I_{L2}+\hat{i}_{L2}) \end{cases} \tag{2}$$

The nonlinear model of converter can be linearized as follows by separating the dc and ac components in equation (2) and assuming $\dfrac{d}{dt}X = 0$ and $\hat{x} \times \hat{y} = 0$.

$$dc: \begin{cases} L_1: \ V_{in}-(1-D)(V_{C1}+V_{C2})=0 \\ L_2: \ D.V_{C1}+(1-D)(-V_{C2})=0 \\ C_1: \ -D.I_{L2}+(1-D)(I_{L1})=0 \\ C_2: \ -\dfrac{V_{C2}}{R}+(1-D)(I_{L1}+I_{L2})=0 \end{cases} \tag{3}$$

$$ac: \begin{cases} L_1\dfrac{d\hat{i}_{L1}}{dt} = \hat{v}_{in}-(1-D)(\hat{v}_{C1}+\hat{v}_{C2})+(V_{C1}+V_{C2})\hat{d} \\ C_1\dfrac{\hat{v}_{C1})}{dt} = (1-D)\hat{i}_{L1}-D.\hat{i}_{L2}-(I_{L1}+I_{L2})\hat{d} \\ L_2\dfrac{d\hat{i}_{L2}}{dt} = D.\hat{v}_{C1}-(1-D)\hat{v}_{C2}+(V_{C1}+V_{C2})\hat{d} \\ C_2\dfrac{\hat{v}_{C2}}{dt} = -\dfrac{\hat{v}_{C2}}{R}+(1-D)(\hat{i}_{L1}+\hat{i}_{L2})-(I_{L1}+I_{L2})\hat{d} \end{cases} \tag{4}$$

Based on the DC component part of the average model, as described in equation (3), the voltages across the capacitors, C_1 and C_2, the currents through the inductors, L_1 and L_2, and the voltage gain ration, M_{CCM}, can be expressed as follows:

$$\begin{cases} V_{C1} = V_{in} \\ V_{C2} = \dfrac{D}{1-D}V_{in} \\ I_{L1} = (\dfrac{D}{1-D})^2(\dfrac{V_{in}}{R}) \\ I_{L2} = (\dfrac{D}{1-D})(\dfrac{V_{in}}{R}) \end{cases} \tag{5}$$

$$M_{CCM} = \frac{V_{C2}}{V_{in}} = \frac{D}{1-D} \tag{6}$$

C. Derivation of Transfer Functions

The Laplace transform of inductor current, $i_{L1}(s)$, can be calculated from equation (4) as follows:

$$i_{L1}(s) = G_{i/v}(s)V_{in}(s) + G_{i/d}(s)d(s) \tag{7}$$

where $G_{i/v}(s)$ and $G_{i/d}(s)$ represent the transfer functions relating the input current of the SEPIC PFC converter to the input voltage and the duty cycle, respectively.

$$G_{i/d}(s) = \frac{i_{L1}(s)}{d(s)} = \frac{z_3s^3+z_2s^2+z_1s+z_0}{p_4s^4+p_3s^3+p_2s^2+p_1s+p_0}$$

$$\begin{cases} z_0 = (V_{C1}+V_{C2})D+(1-D)(I_{L1}+I_{L2})R \\ z_1 = (1-D)(I_{L1}+I_{L2})L_2+(V_{C1}+V_{C2})C_2DR \\ z_2 = C_1L_2(V_{C1}+V_{C2})+ \\ \quad (I_{L1}+I_{L2})(C_1+C_2)(1-D)L_2R \\ z_3 = (V_{C1}+V_{C2})C_1C_2L_2R \\ p_0 = (1-D)^2R \\ p_1 = D^2L_1+(1-D)^2L_2 \\ p_2 = (C_1L_1+C_1L_2+C_2L_2)(1-D)^2R+C_2D^2L_1R \\ p_3 = C_1L_1L_2 \\ p_4 = C_1C_2L_1L_2R \end{cases} \tag{8}$$

$$Y_{ol}(s) = G_{i/v}(s) = \frac{i_{L1}(s)}{v_{in}(s)} = \frac{z'_3s^3+z'_2s^2+z'_1s+z'_0}{p'_4s^4+p'_3s^3+p'_2s^2+p'_1s+p'_0}$$

$$\begin{cases} z'_0 = D^2 \\ z'_1 = (1-D)^2C_1R+C_2D^2R \\ z'_2 = C_1L_2 \\ z'_3 = C_1C_2L_2R \\ p'_0 = (1-D)^2R \\ p'_1 = D^2L_1+(1-D)^2L_2 \\ p'_2 = (C_1L_1+C_1L_2+C_2L_2)(1-D)^2R+C_2D^2L_1R \\ p'_3 = C_1L_1L_2 \\ p'_4 = C_1C_2L_1L_2R \end{cases} \tag{9}$$

Furthermore, the transfer functions that relate the voltage across the dc link capacitor, C_2, to the current of the inductor, L_1, can be determined as follows:

$$G_{v/i}(s) = \frac{v_{C2}(s)}{i_{L1}(s)} = \frac{z''_3s^3+z''_2s^2+z''_1s+z''_0}{z_3s^3+z_2s^2+z_1s+z_0}$$

$$\begin{cases} z''_0 = (V_{C1}+V_{C2})(1-D)R \\ z''_1 = -(I_{L1}+I_{L2})RL_1D \\ z''_2 = (V_{C1}+V_{C2})(L_1+L_2)(1-D)RC_1 \\ z''_3 = -C_1L_1L_2(I_{L1}+I_{L2})R \end{cases} \tag{10}$$

III. Input Admittance of the SEPIC Rectifier

Considering the input admittance is crucial for understanding the converter's stability within the AC power system. Therefore, this section determines the input admittances of SEPIC rectifiers in both open-loop and closed-loop configurations.

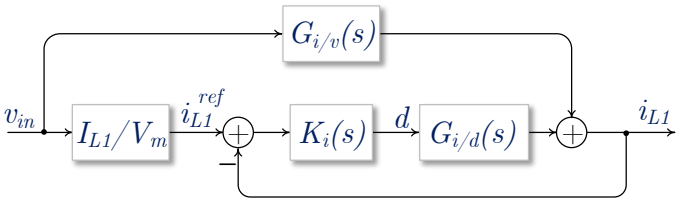


Fig. 3. Block diagram model of the SEPIC PFC converter with a current PR controller.

A. Open-Loop Admittance Modeling

The input admittance of the SEPIC converter in open-loop operation is given by equation (9). The initial gain of the input admittance can be derived by substituting $R = V_{C2}^2/P_{out}$ and (6) into (9).

$$Y_{ol}(0) = G_{i/v}(s)|_{s=0} = \frac{z_0'}{p_0'} = \frac{D^2}{(1-D)^2 R} = \frac{P_{out}}{V_{in}^2} \tag{11}$$

From equation (11), at very low frequencies, the input admittance is primarily influenced by the output power and the input voltage, which determine its gain. This implies that the admittance reflects the dependency of the system's input on its output power transfer and voltage conditions at low frequencies.

Additionally, from equation (9), at very high frequencies, the input admittance of the open-loop system asymptotically approaches $\frac{1}{sL_1}$, where L_1 is the inductance of the input inductor. This indicates that at high frequencies, the behavior of the input admittance is dominated by the inductive reactance of L_1, with the converter effectively behaving as an inductor.

B. Closed-Loop Admittance Modeling with PR Controller

Since the quality of the input current in PFC converters is critical to comply with standards for THD and PF, implementing a well-designed controller for the input current is essential. Based on this requirement, the current control loop in SEPIC PFC rectifiers employs a proportional resonant (PR) controller to ensure precise tracking of the sinusoidal reference signal. The transfer function of the PR controller is expressed as:

$$K_i(s) = k_{pi} + \frac{k_{ii}s}{s^2 + {w_0}^2} \tag{12}$$

where k_{pi} and k_{ii} are the proportional and integral gains, respectively, and ω_0 is the resonant frequency. The resonant term, also known as a generalized integrator, provides infinite gain at ω_0, enabling zero steady-state error for AC signals at this frequency [18], [19].

The closed-loop average model of the SEPIC PFC converter with a current PR controller is provided in Fig. 3. The input admittance in this case can be obtained as:

$$Y_{cl,1}(s) = \frac{i_{L1}(s)}{v_{in}(s)} = \frac{G_{i/v}(s) + \frac{I_{L1}}{V_m}\, G_{i/d}(s)\; K_i(s)}{1 + G_{i/d}(s)\; K_i(s)} \tag{13}$$

where V_m is the peak amplitude of input voltage.

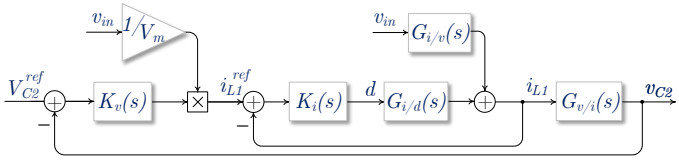


Fig. 4. Block diagram model of the SEPIC PFC converter with a current PR controller and a DC-link PI controller.

C. Closed-Loop Admittance Modeling with PR and PI Controllers

The output voltage of PFC converters should be regulated at a specific voltage. Since it is a DC voltage, a PI controller can be utilized for this purpose. The transfer function of the PI controller can be given as:

$$K_v(s) = k_{pv} + \frac{k_{iv}}{s} \tag{14}$$

where k_{pv} and k_{iv} are the proportional and integral gains, respectively.

The closed-loop PFC SEPIC converter is illustrated in Fig. 2. The system employs two control loops: an outer loop and an inner loop. The outer loop is responsible for regulating the DC link voltage, ensuring that it remains stable and meets the desired operating conditions. The inner loop, on the other hand, is designed to track the reference current generated by the outer loop. To achieve a unity power factor, the reference current is shaped by the phase-locked loop (PLL), which ensures synchronization with the AC voltage phase.

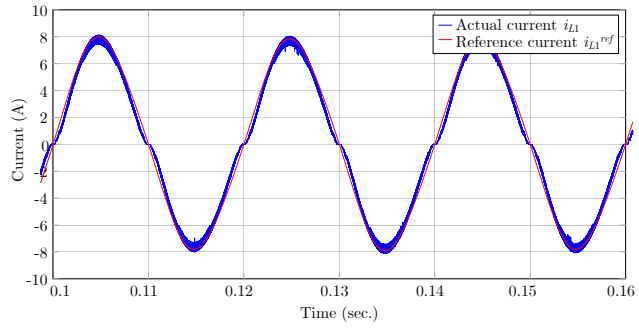
Fig. 4 provides a detailed model of the SEPIC converter, incorporating the proportional-integral (PI) and proportional-resonant (PR) controllers. This model also includes all relevant transfer functions derived from the SEPIC converter. Using this comprehensive model, the relationship between the input voltage and the input current can be calculated as:

$$Y_{cl,2}(s) = \frac{i_{L1}(s)}{v_{in}(s)} = \frac{G_{i/v}(s) - G_{i/d}(s)K_i(s)K_v(s)\frac{V_{C2}}{V_m}}{1 + G_{i/d}(s)K_i(s)\left(K_v(s)G_{v/i}(s) + 1\right)} \tag{15}$$

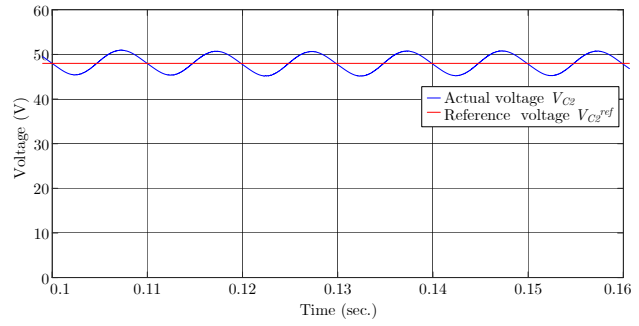
IV. Input Admittance Validation Methodology

In order to validate the input admittance and transfer functions of the SEPIC converter derived from the average model, a detailed analysis is performed on a SEPIC PFC rectifier. The rectifier is configured according to the specifications described in Table I, ensuring that the theoretical results can be compared with the actual performance of the system.

In the switching model of the SEPIC PFC rectifier, the PR and PI controllers that were previously designed are implemented. Fig. 5(a) illustrates both the reference and actual input currents. It is evident that the PR controller performs effectively, ensuring high current quality by making the input current closely follow the reference current with minimal ripple.



(a)



(b)

Fig. 5. Simulation results of SEPIC PFC rectifier (a) input current and (b) output voltage.

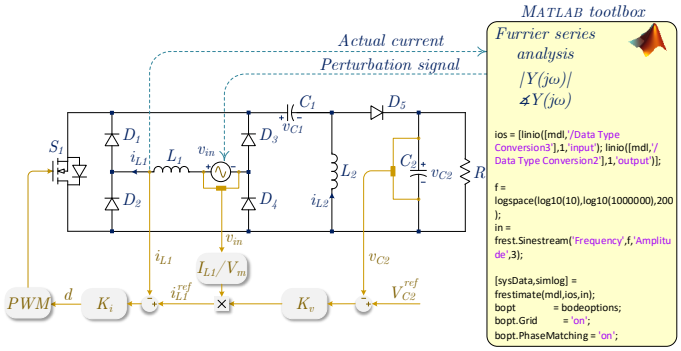


Fig. 6. Frequency response estimation method from the switching mode.

Fig. 5(b) shows the reference output voltage and the actual DC-link voltage. As observed, the output voltage is well-regulated, maintaining a stable value of 48 V.

A frequency response estimation method is employed to analyze the input admittance and transfer function of the system by applying small-signal perturbations over a wide frequency range. In this approach, the MATLAB toolbox is used to estimate the Fourier series of the magnitude and phase of the system response. As shown in Fig. 6, the method involves injecting sinusoidal perturbations into the system and observing its output response, enabling the determination of the system's small-signal characteristics.

A small-magnitude perturbation signal is applied to the duty cycle (input) of the switching model in MATLAB, with the input current, i_{L1}, specified as the output. Following that, as seen in Fig. 7, the transfer function of $G_{i/d}$ is obtained. Excellent agreement is shown between the switching model result and the average model result, which is equivalent to equation (8).

By injecting the perturbation signal into the input voltage and defining the input current as the output, the input admittance based on the switching model can be obtained.

The input admittance of the SEPIC converter in open-loop operation is given by equation (9), and the corresponding Bode plot in addition to the switching model result is shown in Fig. 8. The resonance at 50 Hz is missing because the average model of input admittance is subjected to a dc input voltage. Additionally, three other resonances are observed: one at low frequency (∼124 Hz) and two at higher frequencies (∼3 kHz and ∼4.9 kHz). These resonances arise due to the poles of the input admittance in equation (9). However, due to the complexity of the equation, these resonances cannot be obtained parametrically.

With the presence of a PR controller, the input admittance can be obtained using both the average model (as shown in equation (13)) and the switching model in Fig. 9. In the switching model, the resonance at 50 Hz is sharper, which may be due to the improper adjustment of the perturbation signal's magnitude. At higher frequencies, two resonances appear: one similar to the resonance observed in the open-loop system (∼4.9 kHz) and the other at a slightly higher frequency (∼7 kHz). Furthermore, at higher frequencies, the admittance exhibits inductive behavior with a slope of -20 dB/dec, and in the open-loop system, the slope is -20 dB/dec.

Fig. 10 illustrates the input admittance of the SEPIC rectifier under both PR and PI controllers. The results obtained from the switching model and the average model are in perfect agreement. At higher frequencies, the admittance with the PI controller exhibits inductive behavior, reflected by a magnitude reduction of -20 dB/decade. Despite this change, the magnitude of the admittance with the PI controller is similar to that without it at high frequencies, suggesting that the PI controller has minimal impact on the system's characteristics in the higher frequency range. At lower frequencies, the phase of the input admittance appears to be positive. If the phase exceeds 90 degrees, it can negatively affect the external stability of the system. This is because a phase greater than 90 degrees implies that the system's input admittance could behave in a manner that leads to excessive phase lag, which may cause resonance or instability, especially in grid-connected systems where external conditions (such as grid impedance) can influence the stability. This indicates that the control system primarily influences the system behavior at lower frequencies while maintaining similar performance at higher frequencies.

Since the phase of the input admittance in both open-loop and closed-loop SEPIC PFC converters is typically above -90 degrees, the system appears to be externally stable. However, instability can still occur if the converter parameters are not well-designed or if an improper controller is used.

TABLE I
SEPIC PFC RECTIFIER SPECIFICATIONS

Parameter	Value
Output Power (P_{out})	500 W
Switching Frequency (f_s)	100 kHz
AC Input Voltage (v_g)	110 V, 50 Hz
Output Voltage (V_{out})	48 V
Inductors (L_1, L_2)	1 mH, 150 μH
Capacitors (C_1, C_2)	1 μF, 6800 μF
Integral Gain of PR controller (k_{ii})	10
Proportional Gain of PR controller (k_{pi})	0.7
Integral Gain of PI controller (k_{iv})	100
Proportional Gain of PI controller (k_{pv})	0.1

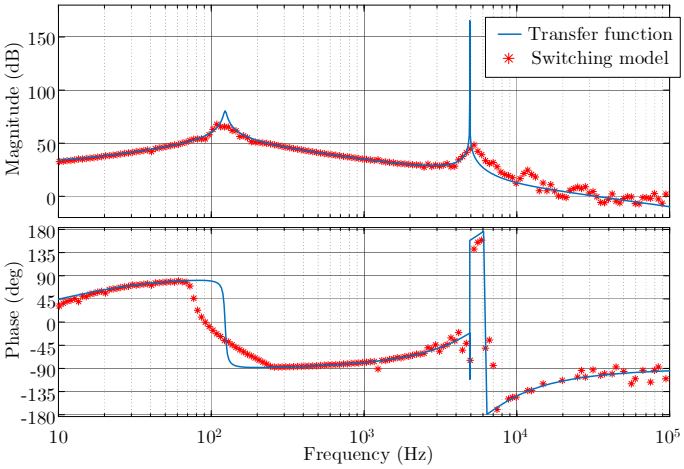


Fig. 7. Frequency response of the input current to the duty cycle in the SEPIC PFC converter, $G_{i/d}(s)$.

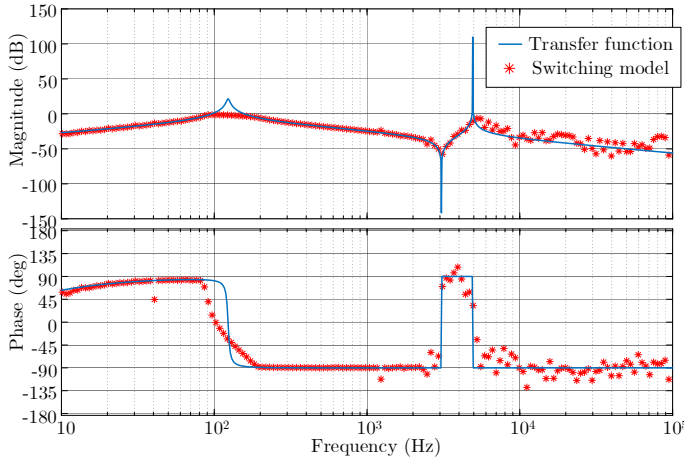


Fig. 8. Frequency response of the open-loop input admittance in the SEPIC PFC converter, $Y_{ol}(s)$.

V. CONCLUSION

In this work, the input admittance models of the SEPIC PFC rectifier were validated through detailed analysis and simulations. The results of the switching model, incorporating both PR and PI controllers, showed excellent agreement with the average model. The input current closely followed the reference current with minimal ripple, ensuring high current quality, and the output voltage remained well-regulated. The frequency response estimation method demonstrated the accuracy of the system's small-signal characteristics, revealing resonance points and the behavior of input admittance at various frequencies. Additionally, the presence of the control system altered the admittance behavior, particularly at lower frequencies, showing the impact of the controller on the system's stability. The results confirmed that both open-loop and closed-loop systems were externally stable, with the input admittance phase remaining below +90 degrees. However, careful design and controller selection are crucial to prevent instability arising from non-passive admittance characteristics. These findings emphasize the importance of input admittance validation to ensure the optimal performance and stability of SEPIC-based PFC converters in practical applications.

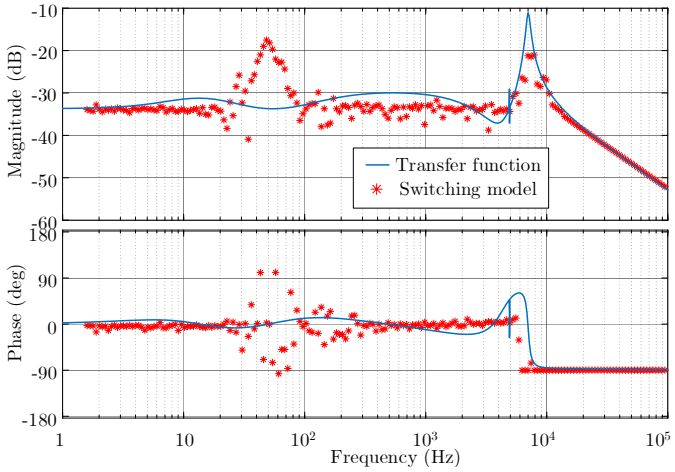


Fig. 9. Frequency response of the closed-loop input admittance in the SEPIC PFC converter with the inner control loop, $Y_{cl,1}(s)$.

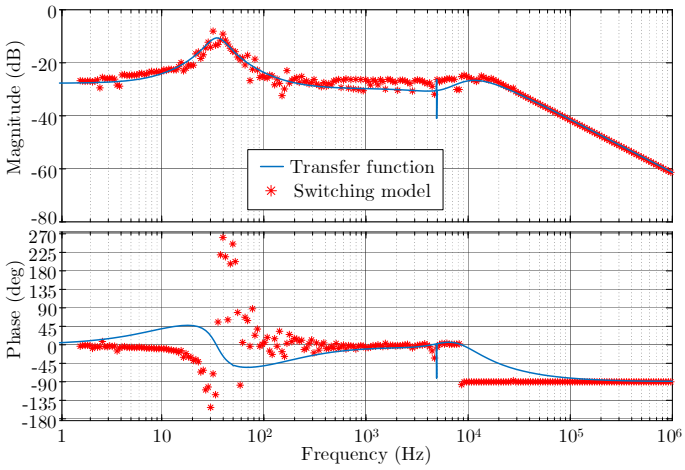


Fig. 10. Frequency response of the closed-loop input admittance in the SEPIC PFC converter with both inner and outer control loops, $Y_{cl,2}(s)$.

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