An Active Capacitor Voltage Balancing Method for a Four-Level Single Flying Capacitor Converter

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Abstract— The four-level single flying capacitor converter (4L-SFC) is an efficient topology for medium-voltage applications, offering a reduced component count over traditional four-level flying capacitor converters. However, maintaining balanced capacitor voltages is a key challenge in this topology, which is critical for stable and reliable operation. In this paper, an active voltage balancing method for 4L-SFC converters is presented, using a straightforward algorithm to adjust voltage levels in response to real-time measurements of capacitor voltages and phase currents. As a result of the proposed method, capacitor voltages remain balanced across a wide range of modulation indexes and operating conditions without significantly increasing switching frequency. Simulation results have demonstrated the effectiveness of the proposed approach, demonstrating that it is capable of maintaining stable capacitor voltages.

Keywords—Capacitor voltage balancing, flying capacitor converter, multilevel converter, space vector modulation.

I. INTRODUCTION

The evolution of medium voltage and current semiconductor devices has prompted the development of multilevel converters, which offer several inherent advantages such as higher DC-link voltages, balanced voltage stress on switching devices, reduced harmonic distortion, lower switching frequencies, and increased power capabilities [1]-[3]. A variety of mature topologies are available for multilevel converters, including modular multilevel converters (MMCs) [4], cascaded H-bridges (CHBs) [5], diode-clamped converters (DCCs) [6], and flying capacitor converters (FCCs) [7]-[8]. Due to their superior power density, efficiency, and lower switching device requirements, DCC and FCC converters outperform CHB and MMC converters for high-density medium-voltage applications [9]-[11].

Despite that, FCC topologies are challenging because of their considerable number of flying capacitors and their difficulty balancing their voltages [12]. It is therefore advantageous to reduce the number of flying capacitors (FCs) in FCC topologies to reduce cost and size. Several researchers have attempted to develop innovative topologies utilizing fewer FCs. However, the reduction in FCs not only eliminates redundant switching states, but also renders capacitor voltage balancing ineffective across the entire operating range [13]. Consequently, it is imperative to develop advanced modulation and control schemes.

A nested converter topology has been developed in [12] as a hybridization of conventional FCC and DCC topologies, called five-level nested diode clamped (5L-NDC) topology. As compared to recently introduced five-level topologies, such as the 5L-ANPC [14], the 5L-NNPP [15], and the 5L-NNPC [16], this topology contains fewer components. However, there are fewer redundant switching states in this topology, resulting in reduced flexibility when balancing capacitor voltages. This limitation is overcome by modifying the modulation scheme with an increased switching frequency.

The four-level single flying capacitor (4L-SFC) topology was first introduced in [17], as a promising alternative among FCCs. The 4L-SFC converter has the advantage of having a simple operation and a significantly reduced number of FCs compared to other four-level topologies, including a four-level FCC [18], a neutral-point clamp (NPC) [19], a nested NPC (NNPC) [20]-[21] and a hybrid clamped converter (HC) [22]-[23]. Although there are four output voltage levels, there are no redundant switching states available as a result of the reduced FCs. Consequently, it is quite challenging to balance the FC voltages and it is necessary to develop enhanced modulation as well as a control scheme to accomplish this. The major challenge with the 4L-SFC is that the FC voltage must be well balanced at one-third of the DC-link voltage.

The conventional modulation schemes, including carrier-based PWM (CB-PWM) and space vector modulation (SVM) methods [24], cannot be effective for the 4L-SFC converter since they result in an FC imbalance problem [25]-[26]. Thus, unbalanced capacitors will cause significant voltage drifts, which will disrupt waveform quality and may damage power devices [27]-[28]. A modulation scheme and a capacitor voltage balancing control method are proposed in [17] to regulate the flying capacitor voltages of the 4L-SFC converter while maintaining other performance indicators. This is accomplished by introducing reconstructed voltage levels [17]. Through this modulation scheme, desired output voltages are generated, and capacitor voltages are naturally balanced. In practice, however, it is necessary to obtain feedback from the FCs and to perform active capacitor voltage balancing due to non-ideal and dynamic conditions.

In this paper, an active FC voltage balancing scheme is implemented by adjusting the duty ratios of voltage levels. In the proposed active voltage balancing scheme, capacitor voltages and phase current signs are measured. Afterward, the duty ratios of the voltage levels are readjusted based on those values in order to reduce the difference between the measured capacitor voltages and the reference values. Using the re-adjusted voltage levels, space vector modulation is implemented. Consequently, the modulation scheme generates the desired output voltage while at the same time regulating the voltages of the flying capacitors. During steady-state

conditions, equal duty ratios are guaranteed for both middle voltage levels that have opposite effects on FC voltages, thus ensuring the FCs are balanced. Whenever there is an unbalanced capacitor voltage, the duty ratios of the middle voltage levels differ, resulting in active control of the capacitor voltage. This proposed modulation has also been demonstrated to comply with the volt-second balance principle. Moreover, switching frequencies are kept low by appropriately arranging switching states and selecting the appropriate switching state space vectors.

Following is an outline of the paper. It is presented in Section II how the 4L-SFC topology operates and how it uses reconstructed voltage levels. Section III describes the implementation of active voltage balancing along with the modulation scheme on the 4L-SFC converter. Section IV presents simulation and experimental results to demonstrate the performance of the proposed scheme for the 4L-SFC converter. Conclusions are provided in section V.

II. The Four-Level Single Flying Capacitor Topology and Its Modulation Scheme

A. Topology and the operation principle of the 4L-SFC

The 4L-SFC topology is shown in Fig 1, which consists of a single flying capacitor per phase, whose voltage rating corresponds to one-third of the DC-link voltage, i.e., $V_{dc}/3$. The circuit consists of four switching devices on each leg. As compared to a conventional 4L-FCC topology, the 4L-SFC topology requires a third as many capacitors, resulting in a significant reduction in component count. There are four phase voltage levels in this converter and there are only four switching states in each leg of the converter, as shown in Table I. As there are no redundant switching states, each voltage level creates its own charging or discharging mode. Therefore, capacitor voltage balancing cannot be achieved using classical modulation schemes.

For each sampling period, the average capacitor current is set to zero to achieve capacitor voltage balancing. This process consists of linearly combining voltage levels of each phase to implement the reconstructed voltage level scheme. Two main objectives must be met through this process:

i. During a sampling period, the average capacitor current must be zero so as to result in a zero change in the capacitor voltage as well.

ii. To synthesize a low distortion output voltage, it is necessary to maintain the volt-second balance.

TABLE I
SWITCHING STATES OF THE 4L-SFC TOPOLOGY AND THE CHARGING STATUS OF THE FLYING CAPACITORS

Switching states (p=a, b, c)				Charging status of the flying capacitor C_p (p=a, b, c)	V_{pn}	Level
S_{p1}	S_{p2}	S_{p3}	S_{p4}			
1	1	0	0	No effect	V_{dc}	3
1	0	1	0	Charging with i_p>0	$2V_{dc}/3$	2
0	1	0	1	Discharging with i_p>0	$V_{dc}/3$	1
0	0	1	1	No effect	0	0

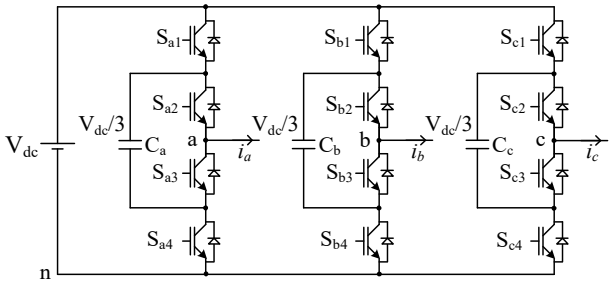


Fig. 1. The four-level single flying capacitor converter topology.

B. Modulation scheme

Each sector of the space vector diagram of the proposed converter consists of nine regions. Three adjacent space vectors are synthesized to form the reference vector in each region. The three vectors are designated as $\mathbf{V_u}$, $\mathbf{V_v}$ and $\mathbf{V_w}$, and are described in terms of corresponding phase voltage levels.

Implementing the concept of reconstructing voltage levels for the 4L-SFC can be expressed after determining the adjacent voltage vectors and calculating their duty ratios. According to the classic SVM method, the adjacent voltage vectors $\{\mathbf{V_v}, \mathbf{V_u}, \mathbf{V_w}\}$ and their duty ratios $\{d_v, d_u, d_w\}$ are derived from $\mathbf{V_{ref}}$.

$$\begin{aligned} &\mathbf{V}_u d_{Vu} + \mathbf{V}_v d_{Vv} + \mathbf{V}_w d_{Vw} = \mathbf{V_{ref}} \\ &d_{Vu} + d_{Vv} + d_{Vw} = 1 \end{aligned} \tag{1}$$

where d_{Vu}, d_{Vv}, and d_{Vw} are the duty ratios of the three adjacent vectors $\mathbf{V_u}$, $\mathbf{V_v}$, and $\mathbf{V_w}$, respectively.

The modulation method for reconstructing phase voltage levels involves maintaining volt-second equilibrium in each phase and ensuring that the sum of duty ratios of the voltage levels applied in each phase equals one. This method uses linear combinations of existing voltage levels to reconstruct the desired levels. For example, to reconstruct voltage level 1 for phase p, a linear combination of levels 0, 1, and 2 is used. Similarly, if phase p of space vector s is set to level 2, it is reconstructed using a linear combination of levels 1, 2, and 3. Throughout the reconstruction process, it is crucial to maintain volt-second balance, meaning the integral of the voltage over time should be consistent for all phases to prevent imbalances. Moreover, the sum of duty ratios of voltage levels applied in each phase must be equal to one. Once the reconstructed voltage levels 1 and 2 are implemented, the method ensures that the average flying capacitor current is zero. This means there is no net current flowing through the flying capacitors over a switching cycle, helping to maintain the voltage levels of the capacitors.The duty ratios of the reconstructed voltage levels are equal to the duty ratio of the corresponding space vector as mentioned by (2).

$$d_{RV_{las}^{as}} = d_{RV_{lbs}^{bs}} = d_{RV_{lcs}^{cs}} = d_{V_s} \quad , \quad s = u, v, w \tag{2}$$

Considering the reconstruction process, the duty ratios of voltage levels 0, 1, 2 and 3 of phase p of space vector s are determined by (3).

$$
\begin{aligned}
d_{V_0^{ps}} &= d_{RV_0^{ps}} + \frac{1}{3} d_{RV_1^{ps}} & d_{V_1^{ps}} &= \frac{1}{3} d_{RV_1^{ps}} + \frac{1}{3} d_{RV_2^{ps}} \\
d_{V_2^{ps}} &= \frac{1}{3} d_{RV_1^{ps}} + \frac{1}{3} d_{RV_2^{ps}} & d_{V_3^{ps}} &= d_{RV_3^{ps}} + \frac{1}{3} d_{RV_2^{ps}}
\end{aligned} \tag{3}
$$

where the duty ratios $d_{V_0^{ps}}$, $d_{V_1^{ps}}$, $d_{V_2^{ps}}$, and $d_{V_3^{ps}}$ respectively correspond to the voltage level 0, 1, 2, and 3 of phase p of space vector s.

In one sampling period, the duty ratio of each phase level is determined as follows:

$$
d_{V_l^p} = d_{V_l^{pu}} + d_{V_l^{pv}} + d_{V_l^{pw}} \qquad l=0, 1, 2, 3 \quad \& \quad p=a, b, c. \tag{4}
$$

where the duty ratios $d_{V_0^p}$, $d_{V_1^p}$, $d_{V_2^p}$, and $d_{V_3^p}$ respectively correspond to voltage level 0, 1, 2, and 3 of phase p during one sampling period.

Having determined the duty ratios associated with each phase level, it is necessary to ensure that the duty ratios are arranged in a manner that minimizes the switching frequency or meets other performance criteria. As a typical level arrangement, voltage levels are applied in the sequence 3-2-1-0 for each phase during one sampling period.

As a next step, it will be necessary to select appropriate space vectors and duty ratios that will, in turn, result in reconstructed levels of interest. This is accomplished by selecting a switching state for each space vector in such a way that switching frequency is minimized. In sector I, the first switching states for space vectors V_u, V_v, and V_w are selected, maintaining phase a at level 3. As a result of applying this algorithm, it can be demonstrated that for all phases, one-third of the half cycle will be at 3 and one-third will be at 0.

The third step modifies the proposed modulation method so that three phase voltage levels are allowed during one sampling period. During a sampling period, the duty ratios of various switching states are rearranged. In this way, phase levels are minimized. As a result of this modification, the output voltage of phase p has three voltage levels, 1, 2, and 3, or three voltage levels, 0, 1, and 2. Considering the new duty ratios of voltage levels as $d'_{V_0^p}$, $d'_{V_1^p}$, $d'_{V_2^p}$, and $d'_{V_3^p}$, the following modifications have been implemented:

When $d_{V_3^p} > d_{V_0^p}$, then the output voltage level 0 is eliminated, and the following new duty ratios are determined.

$$
\begin{aligned}
d'_{V_1^p} &= d_{V_1^p} + d_{V_0^p} & d'_{V_2^p} &= d_{V_2^p} + d_{V_0^p} \\
d'_{V_3^p} &= d_{V_3^p} - d_{V_0^p} & d'_{V_0^p} &= 0
\end{aligned} \tag{5}
$$

When $d_{V_0^p} > d_{V_3^p}$, then the output voltage level 3 is eliminated, and the following new duty ratios are determined.

$$
\begin{aligned}
d'_{V_1^p} &= d_{V_1^p} + d_{V_3^p} & d'_{V_2^p} &= d_{V_2^p} + d_{V_3^p} \\
d'_{V_0^p} &= d_{V_0^p} - d_{V_3^p} & d'_{V_3^p} &= 0
\end{aligned} \tag{6}
$$

The new duty ratios met the necessary conditions, resulting in three voltage levels in the output voltage of phase p at each sampling period.

III. Proposed Active Voltage Balancing Scheme

As a result of the proposed modulation scheme in [6], capacitor voltages should be balanced. It is, however, possible for the open-loop modulation method to gradually degrade its natural capacitor voltage balancing properties under practical operating conditions. Therefore, a closed-loop active capacitor voltage balancing method must be implemented to compensate for voltage drift caused by non-idealities and unfavorable operating conditions.

The duty ratios of the phase voltage levels should be adjusted based on the measured capacitor voltages since these are the only voltage levels that can alleviate unfavorable balancing situations. In the first step, the identical duty ratios of these voltage levels are calculated using the natural voltage balancing modulation method outlined in the previous section. The duty ratios are then readjusted to reduce the difference between the actual capacitor voltages and their reference voltages. To maintain the volt-second balance of the modulation scheme, it is also necessary to change the duty ratios of voltage levels 0 and V_{dc}. During the readjustment process of active voltage balancing of flying capacitors C_p of phase p, the following statuses are taken into account:

Status I: $V_{Cp} > V_{dc}/3$

In this status, the flying capacitor of phase p must be discharged. Table I indicates that, with a positive sign of i_p, the current passing through the capacitor C_p is negative if phase p has a voltage of 1 (i_{Cp}<0) and positive if phase p has a voltage of 2 (i_{Cp}>0). As a result, if the duty ratio of voltage level 1 is increased and/or phase level 1 is applied to the converter for a longer duration than voltage level 2, the balancing behavior of the control scheme will be enhanced. Consequently, the capacitor C_p discharges, resulting in a reduction in its voltage. Alternatively, if i_p is negative, then the duty ratio of voltage level 2 should be greater than the duty ratio of voltage level 1, in order to reduce the positive effect of i_p and improve the effectiveness of the balancing strategy. Therefore, in the case of three voltage levels 1, 2, and 3, the duty ratios are changed as follows,

$$
\begin{aligned}
d''_{V_1^p} &= d'_{V_1^p} + 0.5 \times \min(d'_{V_1^p}, d'_{V_2^p}, d'_{V_3^p}) \times sign(i_p) \\
d''_{V_2^p} &= d'_{V_2^p} - \min(d'_{V_1^p}, d'_{V_2^p}, d'_{V_3^p}) \times sign(i_p) \\
d''_{V_3^p} &= d'_{V_3^p} + 0.5 \times \min(d'_{V_1^p}, d'_{V_2^p}, d'_{V_3^p}) \times sign(i_p) \\
d''_{V_0^p} &= 0
\end{aligned} \tag{7}
$$

where the new duty ratios $d'_{V_0^p}$, $d'_{V_1^p}$, $d'_{V_2^p}$, and $d'_{V_3^p}$ correspond to voltage levels 0, 1, 2 and 3, respectively. These new duty ratios will result in a reduction in the voltage of the flying capacitor C_p and will satisfy the requirements of the modulation. As a result of this modification, phase p output voltage only has three voltage levels, 1, 2 and 3. This allows the switching frequency reduction scheme to be implemented.

In the case of three voltage levels 0, 1, and 2, the duty ratios are changed as follows,

$$\begin{aligned} d^{''}_{V_1^p} &= d^{'}_{V_1^p} + \min(d^{'}_{V_0^p}, d^{'}_{V_1^p}, d^{'}_{V_2^p}) \times sign(i_p) \\ d^{''}_{V_2^p} &= d^{'}_{V_2^p} - 0.5 \times \min(d^{'}_{V_0^p}, d^{'}_{V_1^p}, d^{'}_{V_2^p}) \times sign(i_p) \\ d^{''}_{V_0^p} &= d^{'}_{V_0^p} - 0.5 \times \min(d^{'}_{V_0^p}, d^{'}_{V_1^p}, d^{'}_{V_2^p}) \times sign(i_p) \\ d^{''}_{V_3^p} &= 0 \end{aligned} \tag{8}$$

These new duty ratios will result in a reduction in the voltage of flying capacitor C_p, and the necessary requirements will be met. As a result of this readjustment, the output voltage of phase p consists of just three voltage levels 0, 1 and 2.

Status II: $V_{Cp} < V_{dc}/3$

There should be a positive current flowing through the capacitor if the voltage of the capacitor C_p is lower than the nominal value. By doing so, the difference between the actual voltage and the rated voltage will be reduced. Therefore, for a positive output current, voltage level 1 should comprise a smaller portion of the sampling period than voltage level 2. For negative phase currents, the most favorable approach from the viewpoint of balancing the capacitor voltage is to increase the duty ratios of voltage level 1. Therefore, in the case of three voltage levels 1, 2, and 3, the duty ratios are changed as in (9) to increase the voltage of flying capacitor C_p and the keep the switching frequency minimize.

$$\begin{aligned} d^{''}_{V_1^p} &= d^{'}_{V_1^p} - 0.5 \times \min(d^{'}_{V_1^p}, d^{'}_{V_2^p}, d^{'}_{V_3^p}) \times sign(i_p) \\ d^{''}_{V_2^p} &= d^{'}_{V_2^p} + \min(d^{'}_{V_1^p}, d^{'}_{V_2^p}, d^{'}_{V_3^p}) \times sign(i_p) \\ d^{''}_{V_3^p} &= d^{'}_{V_3^p} - 0.5 \times \min(d^{'}_{V_1^p}, d^{'}_{V_2^p}, d^{'}_{V_3^p}) \times sign(i_p) \\ d^{''}_{V_0^p} &= 0 \end{aligned} \tag{9}$$

In the case of three voltage levels 0, 1, and 2, the duty ratios are changed as follows,

$$\begin{aligned} d^{''}_{V_1^p} &= d^{'}_{V_1^p} - \min(d^{'}_{V_0^p}, d^{'}_{V_1^p}, d^{'}_{V_2^p}) \times sign(i_p) \\ d^{''}_{V_2^p} &= d^{'}_{V_2^p} + 0.5 \times \min(d^{'}_{V_0^p}, d^{'}_{V_1^p}, d^{'}_{V_2^p}) \times sign(i_p) \\ d^{''}_{V_0^p} &= d^{'}_{V_0^p} + 0.5 \times \min(d^{'}_{V_0^p}, d^{'}_{V_1^p}, d^{'}_{V_2^p}) \times sign(i_p) \\ d^{''}_{V_3^p} &= 0 \end{aligned} \tag{10}$$

After a readjustment of the duty ratios, the main requirement is to maintain the volt-second balance of the modulation scheme over the entire sampling period. Considering phase x (x=a, b, c), this condition has been satisfied in (1) and can be written as follows:

$$\begin{aligned} &0 \times d^{''}_{V_0^p} + V_{dc}/3 \times d^{''}_{V_1^p} + 2V_{dc}/3 \times d^{''}_{V_2^p} + V_{dc} \times d^{''}_{V_3^p} = V_{ref-p} \\ &d^{''}_{V_0^p} + d^{''}_{V_1^p} + d^{''}_{V_2^p} + d^{''}_{V_3^p} = 1 \end{aligned} \tag{11}$$

By analyzing statues I and II, duty ratio readjustments can be implemented by considering the sign of the voltage deviation of flying capacitor, which is expressed as follows:

$$sign(\Delta V_{Cp}) = \begin{cases} +1 & if \;\; V_{Cp} > V_{dc}/3 \\ -1 & if \;\; V_{Cp} < V_{dc}/3 \end{cases} \tag{12}$$

The sign of the voltage deviation of the flying capacitor is utilized to combine the relationships (7)-(10). Therefore, in the case of three voltage levels 0, 1, and 2, considering (8) and (10), the duty ratios are readjusted as follows,

$$\begin{aligned} d^{''}_{V_1^p} &= d^{'}_{V_1^p} + \min(d^{'}_{V_0^p}, d^{'}_{V_1^p}, d^{'}_{V_2^p}) \times sign(\Delta V_{Cp}) \times sign(i_p) \\ d^{''}_{V_2^p} &= d^{'}_{V_2^p} - 0.5 \times \min(d^{'}_{V_0^p}, d^{'}_{V_1^p}, d^{'}_{V_2^p}) \times sign(\Delta V_{Cp}) \times sign(i_p) \\ d^{''}_{V_0^p} &= d^{'}_{V_0^p} - 0.5 \times \min(d^{'}_{V_0^p}, d^{'}_{V_1^p}, d^{'}_{V_2^p}) \times sign(\Delta V_{Cp}) \times sign(i_p) \\ d^{''}_{V_3^p} &= 0 \end{aligned} \tag{13}$$

In the case of three voltage levels 1, 2, and 3, considering (7) and (9), the duty ratios are readjusted as follows,

$$\begin{aligned} d^{''}_{V_1^p} &= d^{'}_{V_1^p} + 0.5 \times \min(d^{'}_{V_1^p}, d^{'}_{V_2^p}, d^{'}_{V_3^p}) \times sign(\Delta V_{Cp}) \times sign(i_p) \\ d^{''}_{V_2^p} &= d^{'}_{V_2^p} - \min(d^{'}_{V_1^p}, d^{'}_{V_2^p}, d^{'}_{V_3^p}) \times sign(\Delta V_{Cp}) \times sign(i_p) \\ d^{''}_{V_3^p} &= d^{'}_{V_3^p} + 0.5 \times \min(d^{'}_{V_1^p}, d^{'}_{V_2^p}, d^{'}_{V_3^p}) \times sign(\Delta V_{Cp}) \times sign(i_p) \\ d^{''}_{V_0^p} &= 0 \end{aligned} \tag{14}$$

IV. Simulation Results

Simulations were conducted to verify the proposed active voltage balancing scheme. Detailed parameters of the simulated system are presented in Table II. The flying capacitor voltages are zero at the start of the simulation. In Fig.2, simulation results are shown when modulation index is 0.95. The phase voltage (relative to negative rail), line voltage and output current waveforms are shown in Fig. 2(a) and Fig 2(b). By applying this modulation scheme, the switching frequencies of switches Sa1 and Sa2 (shown in Fig. 1) have been equalized to 2 kHz each. Three-phase flying capacitor voltages are shown in Fig. 2(c), which are regulated at the desired values. Fig. 3 shows the waveforms of the voltage of phase *a* (relative to the negative rail), line voltage, capacitor voltage, and output current. The capacitor voltages are raised to reach the reference value and are well balanced at the desired values, as can be seen from Figure 3(c). In the simulated system, the capacitor voltage balancing of FCs is investigated under various modulation indexes. After t=0.1s, the modulation index changes from 0.95 to 0.6, and after t=0.15s, the modulation index changes from 0.6 to 0.3. As can be seen, the capacitor voltages remain balanced at different modulation indexes. As a result of the impedance nature of the load in the simulated system, the load current is decreased at lower modulation indexes, resulting in a lower capacitor voltage ripple.

The duty ratios of voltage levels 3, 2, 1, and 0 at the beginning of the simulation are shown in Fig. 4. The duty ratios of voltage levels 1 and 2 are not identical, which is due to the active voltage balancing scheme. The switching frequencies of all switches are equal to 2 kHz, which is the same as the natural capacitor voltage balancing scheme presented in [6]. Fig. 5 illustrates the duty ratios of voltage levels when capacitor voltages are balanced at various modulation indexes. The duty

ratios of voltage levels 1 and 2 are the same under these conditions. In addition, voltage levels 0 and 3 have the same duty ratios with a 180-degree phase shift.

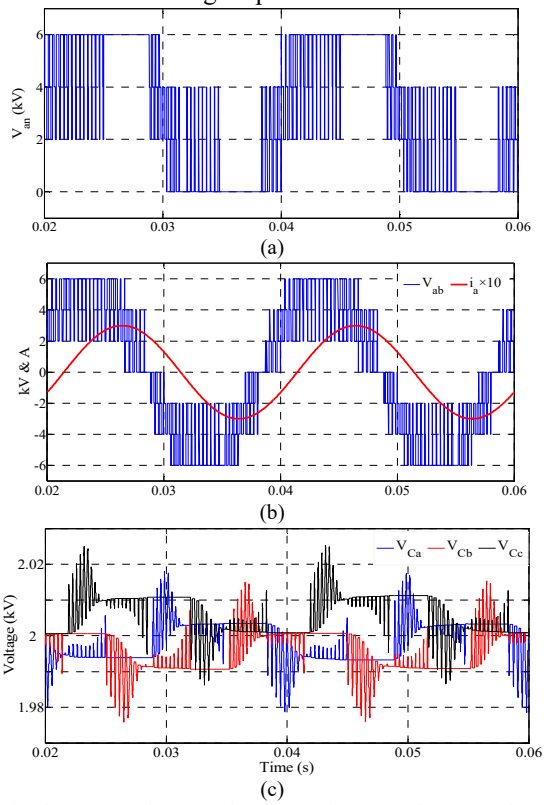
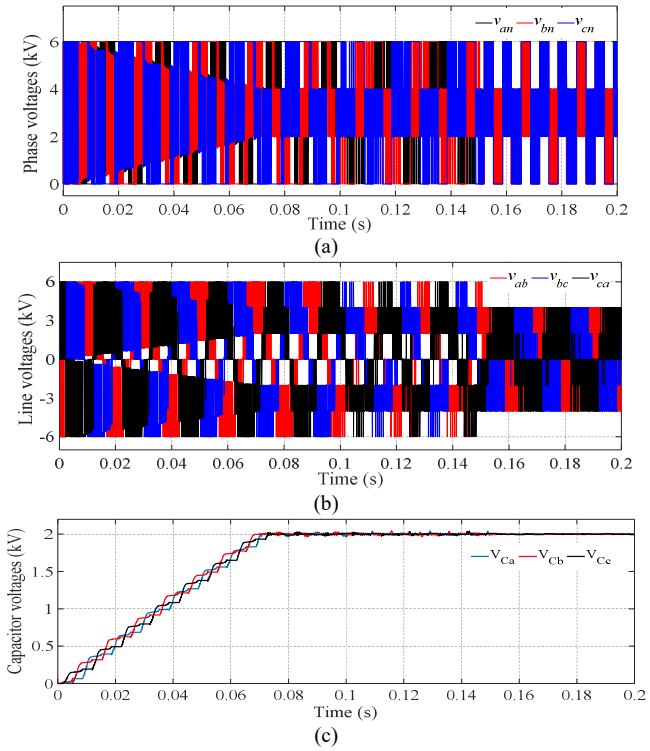


Fig. 2. Simulation waveforms of the proposed SVM technique with switching frequency reduction, (a) phase a voltage (V_{an} in Fig. 2), (b) line voltage and output current, (c) flying capacitor voltage of three phases.



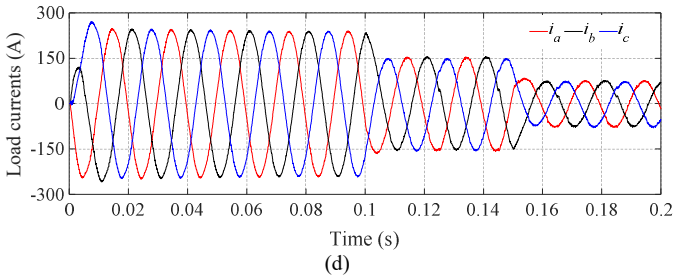


Fig. 3. Simulation waveforms of the proposed active voltage balancing SVM technique, (a) phase voltages, (b) line voltages, (c) flying capacitor voltages, (d) load currents.

TABLE II
SIMULATED SYSTEM PARAMETERS

Parameter	Value
DC source voltage (V_{dc})	6 kV
Capacitance of flying capacitors	1 mF
Line frequency (f_o)	60 Hz
Modulation index (M)	0.95
Sampling frequency (f_s)	3 kHz
Rated load current	220 A
Power factor	0.9

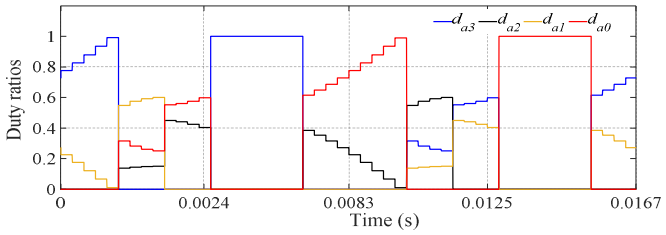


Fig. 4. Duty ratios of voltage levels resulted from the proposed modulation scheme when the capacitor voltages are unbalanced.

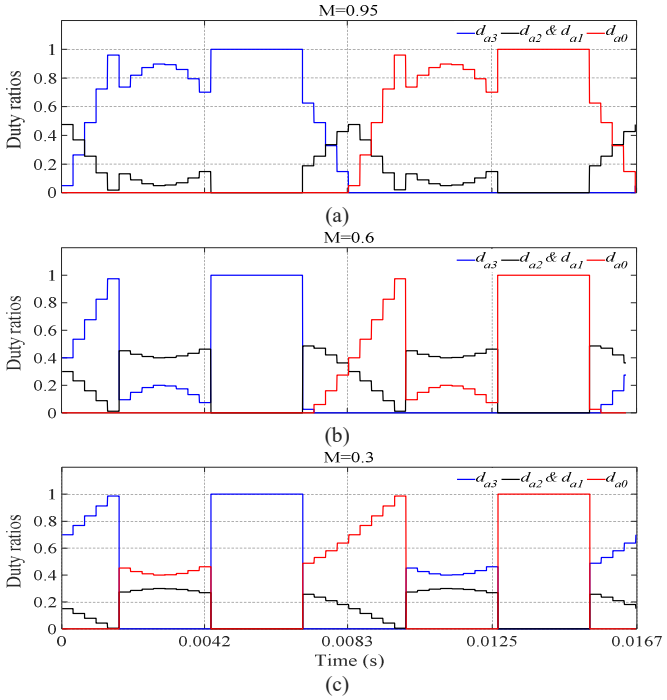


Fig. 5. Duty ratios of voltage levels resulted from the proposed modulation scheme at balancing conditions for various modulation indexes, (a) M=0.95, (b) M=0.6, and (c) M=0.3.

V. Conclusion

This paper proposes an active voltage balancing method for the 4L-SFC converter with a straightforward algorithm. The reconstructed voltage levels were used to implement a space vector modulation scheme. Based on the measurement of the flying capacitor voltages and the output current of each converter phase, the duty ratios of voltage levels are readjusted for active voltage balancing. Using the proposed straightforward method, the FC voltages for the 4L-SFC can be balanced and stabilized at various output frequencies. The active voltage balancing scheme is independent of the output frequency and effectively operated at low frequency applications. As a result of the proposed scheme, all semiconductor switches are operated at the same frequency, thus equalizing switching losses. The experimental results show the effectiveness of the proposed scheme.

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