Inhibiting the current spikes within the channel layer of $LiCoO_2$-based three-terminal synaptic transistors

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Abstract

Synaptic transistors, which emulate the behavior of biological synapses, play a vital role in information processing and storage in neuromorphic systems. However, the occurrence of excessive current spikes during the updating of synaptic weight poses challenges to the stability, accuracy, and power consumption of synaptic transistors. In this work, we experimentally investigate the main factors for the generation of current spikes in the three-terminal synaptic transistors that use $LiCoO_2$ (LCO), a mixed ionic-electronic conductor (MIECs), as the channel layer. Kelvin probe force microscopy (KPFM) and impedance testing results reveal that it is ion migration and adsorption on the drain/source-channel interface that cause the current spikes which compromise the device's performance. By controlling the crystal orientation of the LCO channel layer to impede the in-plane migration of lithium ions, we show that the LCO channel layer with the (104) preferred orientation can effectively suppress both the peak current and power consumption in the synaptic transistors. Our study provides a unique insight into controlling the crystallographic orientation for the design of high-speed, high-robustness and low-power consumption nano-memristor devices.

1. Introduction

The demands of data-intensive machine learning tasks have spurred a quest for novel processing approaches that surpass conventional logic and memory architectures.[1] By leveraging parallel processing, dedicated matrix multiplication units, and efficient memory access patterns, artificial neural networks can significantly improve computational efficiency and accelerate large-scale machine learning tasks.[2,3] To realize these brain-inspired computing systems, multiple research efforts focused on three-terminal ionic-based synaptic transistors, which closely resemble the operation of biological synapses.[4-6] In ionic-based synaptic transistors, the conductive tunable region is primarily controlled by ion migration through a switching layer under an electric field. However, the ion migration exhibits a significant level of randomness that is influenced by grain boundary scattering, vacancies, dopants and nanopores.[7,8] This stochastic ion migration is particularly pronounced in amorphous switching layer materials, which can be further complicated by the repeatedly shuttling of ions during resistive switching cycles, resulting in cycle-to-cycle variability and irreversible damage to devices.[9,10]

To comprehend the dynamic processes of ions and electrons in synaptic transistors, a variety of organic and inorganic mixed ionic-electronic conductors (MIECs) have been utilized to construct synaptic devices.[11,12] However, the incompatibility of lithography technology of organic materials, as well as their unsatisfactory

temperature tolerance capability, limits the applications in large-scale machine learning systems.[13] In contrast, the complementary metal-oxide-semiconductor compatible inorganic MIECs exhibit enhanced resistance to device degradations, ensuring reliable and long-lasting performance in demanding machine learning systems.[13,14] Among them, the lithium-ion conductors (e.g., $LiCoO_2$,[15] Li_3PO_4,[16] and Li_xTiO_2[17]) with moderate diffusion coefficient (10^{-9}-10^{-11} cm^2 s^{-1}) and low activation energy (0.17-0.84 eV) have been extensively studied as channel layer materials.[18,19] The first lithium-ion device has demonstrated predictable ultra-low energy consumption of 250 aJ/μm^2 and high durability of more than 10^5 cycles.[15] Meanwhile, the lithium-based devices exhibit stable resistance retention (10^6 s) and rapid switching speeds of 100 ns due to the small cation size, indicating the great potential of lithium-based devices in the future application of rapid speed and low energy consumption neural network hardware.[20] However, there are still many physical mechanisms of synaptic events involved in lithium-ion diffusion that are far from well understood. The lithium-ion devices possess an exceptional combination of mobile ions (e.g., Li^+), vacancies, and free electrons, enabling reversible accumulation and dissipation of the space charge layer in the channel, which leads to the non-volatile resistive switching (RS) and can be used to mimic synaptic processes.[21-23] During the operation, the application of voltage pulses at the gate is accompanied by current flowing between the source/gate and drain, resulting in the generation of excitatory postsynaptic current-like (EPSC) responses.[24] While the energy consumption per spike event is dominated by the EPSC process, which can be calculated by multiplying the peak EPSC, pulse duration, and voltage between the source and drain (V_{SD}).[11,25] To achieve ultra-low energy consumption, the synaptic transistor needs to be programmed and read using a small value of V_{SD} and should be capable of responding with a small EPSC current.[26] However, there are few effective strategies to solve the problem of excessive current spikes, with deficient intrinsic physical ion diffusion mechanism of EPSC process and corresponding experimental evidence.[27]

Therefore, this study investigates the phenomenon of current spikes in synaptic transistors employing the lithium-ion-based MIECs channel layer and proposes effective strategies to inhibit the probabilistic ion motion within the channel layer. Here we first characterise the ionic-electronic migration behaviour in our LCO synaptic transistors using Kelvin Force Microscopy and Impedance Spectroscopy, and then successfully verify the drain-channel interface diffusion/adsorption model by tuning the lithium-ion diffusion anisotropy in the $LiCoO_2$ channel. The optimized device with an LCO (104) channel shows a near-tenfold decrease in power consumption.

2. Results and discussion

2.1 Structure and EPSC of $LiCoO_2$-based synaptic transistor

We fabricated a three-terminal synaptic transistor as illustrated in Figs. 1(a) and 1(b). The interdigitated electrodes were used as the source/drain electrodes for more efficient measurement of the channel layer conductance state. Specifically, the interdigitated electrode structure can enhance the effective area of source/drain *vs* channel interfaces, enabling efficient charge transfer and amplified interfacial effects. Firstly, the bottom interdigitated electrodes (with a channel distance of about 8 μm) were prepared by the photolithography. Platinum source/drain electrodes (~60 nm) were deposited via sputtering onto the $SrTiO_3$ (STO) substrate. Then, the $LiCoO_2$ (LCO) channel layer (~70 nm) was grown, followed by an ~80-nm-thick SiO_x deposited by radio frequency (RF) sputtering as the insulation layer and lithium-ion reserve layer.[28] At last, the Pt top layer was deposited on top of SiO_x as the gate electrode. In our previous study, we showcased the operational mechanism of the three-terminal LCO-based transistor wherein the application of a negative pulse to the gate electrode triggers the migration of Li^+ ions from the LCO layer towards the SiO_x layer.[29] The trapping effect of the amorphous SiO_x dielectric layer was evaluated by testing the switching behaviour in $LiCoO_2/SiO_x/Si$ stack (see supplementary material Section 1). On the other hand, the positive pulse at the gate results in the ion migration out of the SiO_x layer. This reversible lithium-ion migration causes the reversible insulator-metal transformation (IMT) in the LCO channel layer, modifying the conductance states within the channels.

Our synaptic transistors can mimic the EPSC-like response of a biological synapse as illustrated in Fig. 1(c). In the nervous system, the biological synapse serves as a fundamental unit, facilitating the transmission and communication of information between neighbouring neurons.[30,31] When the pre-synapse is stimulated, neurotransmitters are released from pre-synaptic neurons. These neurotransmitters will bind to receptors on post-synaptic neurons, leading to a transient increase in the post-synaptic current from its base value, I_0, to the peak value, I_p. In our case, the migration of Li^+ is similar to the neurotransmitters released during the EPSC process when the negative gate voltage pulse is applied. However, there is no clear explanation for the physical mechanism of the spike current in the EPSC process of LCO synaptic transistors, which can lead to increased energy dissipation and unstable voltage, resulting in the overheating of the device.

To understand the current spikes in the EPSC process, it is constructive to review the ion migrations, as well as the resulting interfacial phenomenon, including Electric-double-layer (EDL) formation and interfacial

electrochemical reactions,[32] in LCO synaptic transistors. Initially, the lithium ions are uniformly distributed throughout the LCO layer, resulting in the channel exhibiting an insulating state as shown in Fig. 1(d). The positive reading voltage bias (V_{SD}) applied between the source electrode and drain electrode (grounded) results in the charge carriers (Lithium-ion) accumulation on the drain-LCO interface, forming the EDL at the drain/source-channel interface. Once a negative write voltage pulse is applied to the gate electrode, Li^+ ions migrate and accumulate on the LCO-SiO_x electrolyte interface and then partially lithiate the SiO_x layer. It is worth noticing that, when applying the gate voltage, there is also a non-negligible upward migration of locally accumulated lithium ions atop the drain electrode surface [Fig. 1(e)], similar to the instantaneous activation of a "valve". It is this opened current "valve" that facilitates the electron flow through the source during the whole period of the gate voltage pulse, resulting in the current peak, I_p, in the EPSC.

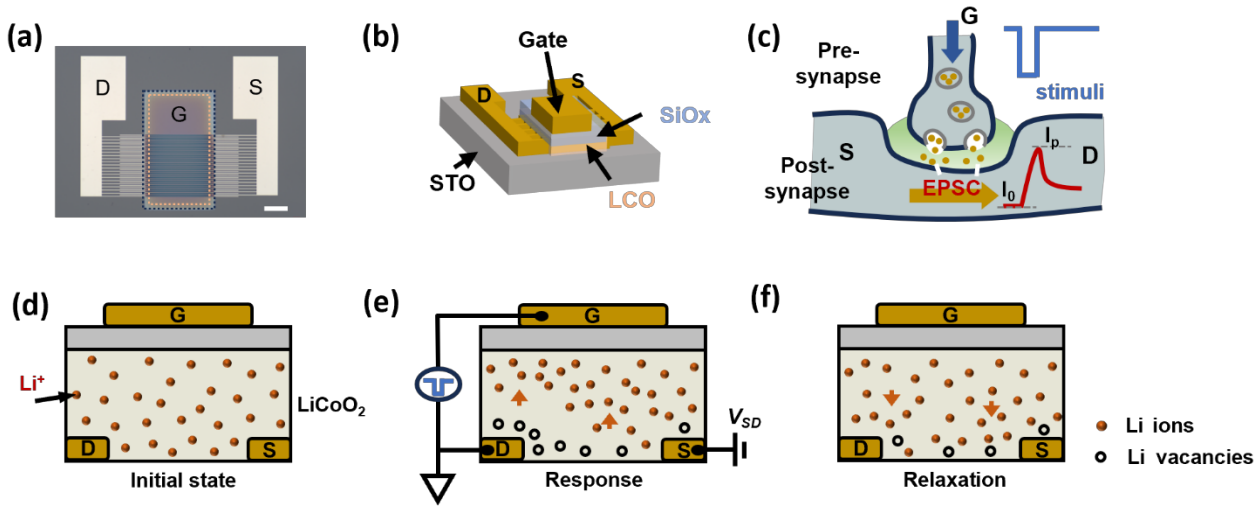

FIG 1. (a) Optical microscope image and (b) schematic diagram of the fabricated synaptic transistor. The length of the scale bar in Figure 1 (a) is 200 μm. (c) A schematic diagram of the EPSC happened in a biological synapse. (d-f) Brief schematic of the EPSC process in LCO-based synaptic transistor.

With the removal of the voltage pulse, the Li^+ ions gradually drift back to their equilibrium positions in the channel. This is accompanied by the relaxation of EPSC. Specifically, when the gate voltage is higher than the lithiation voltage threshold of SiO_x, the Li^+ ions diffuse to the SiO_x insulator layer will not fully return to the LCO channel layer, resulting in an increased electronic conductivity of the LCO channel layer due to the lithiation induced IMT. As a result, EPSC does not return to its initial position (I_0) over a period of relaxation time, and EPSC tends to stabilise at another value when the EDL has formed on the source/drain channel interface again, with the "valve" being switched off.

2.2 Interfacial charge accumulations revealed by Kelvin probe force microscopy (KPFM)

Overall, the concentration of lithium ions at the drain-channel interface determines the magnitude of the peak current I_p. However, previous studies have generally overlooked the impact of interfacial charge accumulation on the EPSC process, with limited experimental evidence has been reported regarding the generation of spiking currents. To understand the interface charge accumulation, we further employed KPFM to probe the surface potential difference between the source and drain under various applied read voltages.

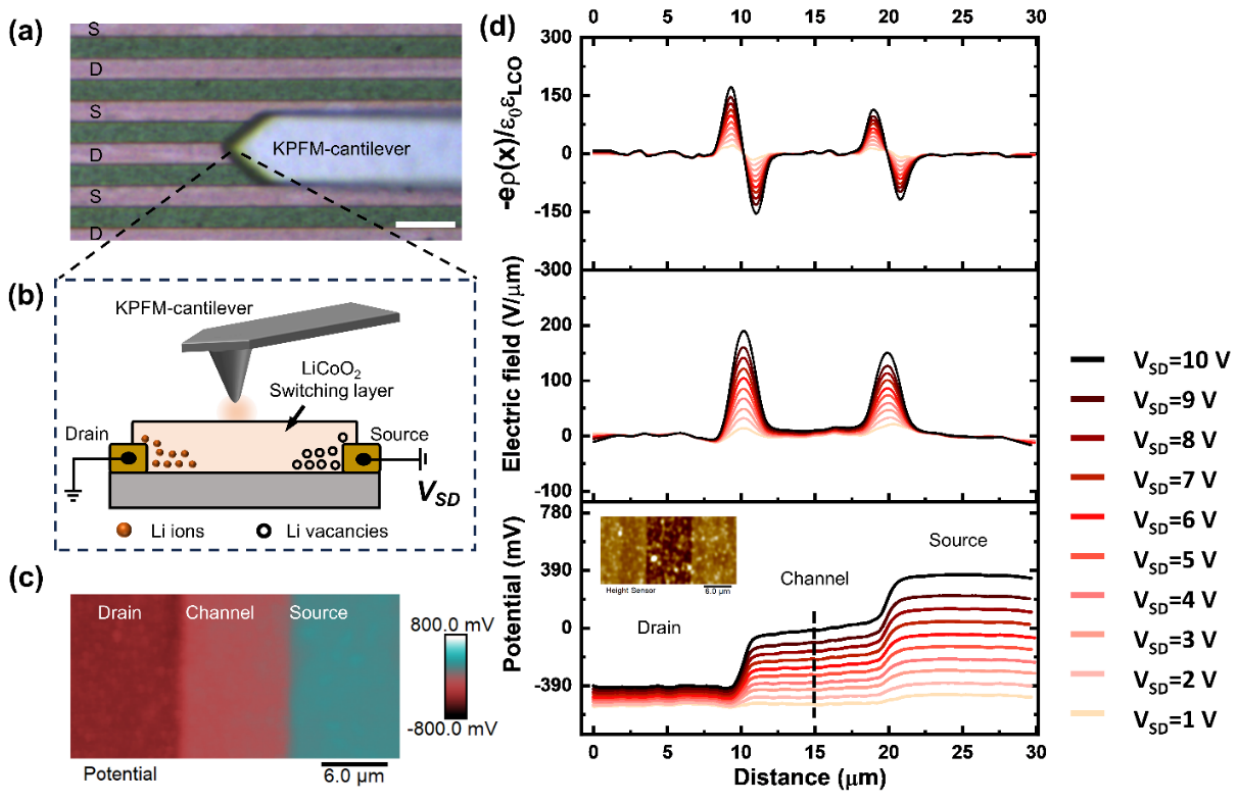

FIG 2. (a) Optical image of KPFM testing. The inset scale bar is 10 μm. (b) Measurement configuration of the KPFM tip on top of a device under varying V_{SD}. (c) 2D surface potential difference distribution map of an LCO (104) channel in a synaptic transistor using the KPFM mode. (d) The surface potential profiles across the channel region at various source voltages when the drain is grounded. The pictures in the middle and above are the corresponding electric field distribution and the charge density distribution in the measured channel region, respectively. The inset picture is the AFM topological height image of the measured LCO (104) channel.

The optical photograph and schematic diagram of the KPFM measurement are shown in Figs. 2(a) and 2(b). The positive voltage biases (1-10 V) were applied to the source electrode, the drain was grounded, and the experiment was conducted at room temperature in an Ar O_2/H_2O-free environment. Fig. 2(c) shows the KPFM surface potential (with respect to the platinum-coated tip) distribution map film from the drain to source contact

along the channel at V_{SD} = 1 V. The sample surface consists of three regions with distinct and well-defined potential distribution. By differentiating the measured potential *vs* distance profile [Fig. 2(d)] along the LCO channel, the surface electric field ($E(x)$) along the *x*-axis (drain-to-source) can be obtained according to the equation $E(x) = \frac{d(Surface\ Potential)}{dx}$.[33,34] As shown in Fig. 2(d), with an increase of V_{SD} from 1 to 10 V, the surface potential at the middle (the black dotted arrows in Fig. 2(d)) of the LCO channel increased from about -520 mV to -10 mV. Moreover, the maximum field strength at source/drain-channel interfaces (the peak value of the Electric Field *vs* Distance plot in Fig. 2(d)) increases gradually with the applied V_{SD}. The sharpest changes in surface potential were observed at the source/drain-channel interfaces. This indicates that there is a considerable Schottky barrier at the Pt/LCO interface.[34,35] We can use Poisson's equation $\left(-\frac{d^2\varphi}{dx^2} = \frac{q\rho(x)}{\varepsilon_0\varepsilon_{LCO}}\right)$, where $\rho(x)$ is the charge density as a function of distance *x*, ε_0 and ε_{LCO} are the dielectric constant of vacuum and LCO, respectively,[35] the distribution of charge density in the channel can be further obtained. The spatial distribution of charge density extending into the channel region can be observed in the $\frac{q\rho(x)}{\varepsilon_0\varepsilon_{LCO}}$ *vs* distance plot in Fig. 2(d). The concentration of ions/vacancies near the drain/source-channel contact is abnormally higher compared to the central region of the channel. The high charge density at the Pt/LCO interface can be attributed to the redistribution of ions following their migration/adsorption under the electric field, indicating an interfacial charge accumulation near the source/drain-channel interfaces. This can be explained as follows: when the source is positively biased, the quasi-fermi level drops at the source, creating an electrical gradient between the source and drain and driving the cations (Li^+) to move and concentrate at the drain electrode surface, and Li^+ vacancies on the source electrode surface.[33,36] Li^+ concentrated on the drain electrode surface forms the EDL on the Pt drain and LCO channel interface, thus resulting in the localized high lithium concentration and high electronic resistance region in the channel, as shown in Fig. 2(b).

The above results unambiguously support our assumptions on the impact of ion migration in LCO synaptic transistors. On the one hand, Li^+ ions accumulate at the drain interface, leading to the creation of a more insulative LCO region. Although a locally conductive region of accumulated Li^+ vacancies is created at the source electrode, the transient conductance (or I_p) of the channel should be determined by an insulating region which functions as a valve. Once the valve opens due to the application of negative gate pulses, the conductance will increase instantaneously, and the spike current of the post-excitation current is therefore generated, resulting in the high I_p in EPSC.

2.3 Effect of crystal orientations on the in-plane Li^+ migrations

Considering that it is the concentration and migration of lithium ions at the interface that determine the magnitude of the current spike, inhibiting the Li^+ ions interface aggregation would be an effective strategy for suppressing spike currents. The epitaxial LCO thin films with different preferred orientations were fabricated to tackle the interfacial charge accumulation/adsorption effect using the anisotropic lithium migration characteristic of LCO.

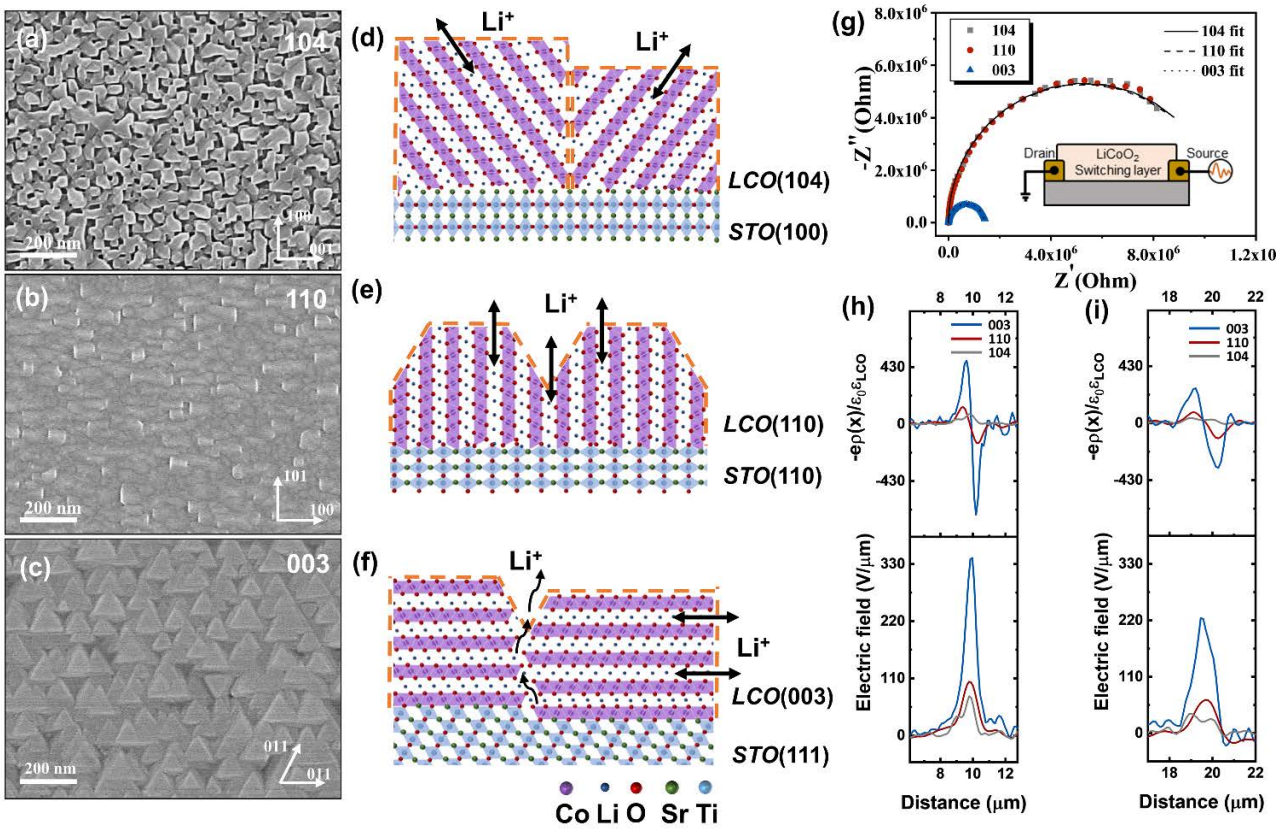

FIG 3. Surface SEM images of (a) LCO (104), (b) LCO (110) and (c) LCO (003) thin films. The in-plane symmetry of the LCO grain is labelled by the arrows. (d-f) The corresponding lattice models and macro characteristics for LCO on STO (100), STO (110) and STO (111). The black arrows denote the Li-ion diffusion pathways in the three structures. (g) Impedance spectroscopy at varying orientations in the range of 0.1-10^6 Hz. The inset diagram is a schematic of the impedance test. Electric field distribution and the charge density distribution of (h) positively polarized drain-channel and (i) negatively polarized source-channel interface region with three different LCO orientations.

$SrTiO_3$ (STO) substrates with (100), (110) and (111) surfaces were used to induce (104), (110) and (003) out-of-plane orientations of the LCO channel layers, respectively. The (003), (110), and (104) orientations were chosen primarily because that, STO (111), (110) and (100) substrates are widely reported and known for their reliable epitaxial growth of the LCO thin films with (003), (110), and (104) orientations.[37] More Importantly,

these three LCO orientations are characteristic crystal orientations for the study of anisotropic diffusion of lithium ions inside the channel layer. For LCO, the Li^+ layers and cobalt-oxygen (Co-O) layers stack layer-by-layer along the c-axis to form a 2D layered crystal structure. It has been established that in bulk LCO, the migration of lithium ions primarily takes place within the two-dimensional plane formed by the Co-O layers.[38] This results in an anisotropic diffusion coefficient of Li^+ ions (10^{-13} to 10^{-10} cm^2 s^{-1}) along the in-plane directions of (104), (110) and (003) facets, rendering them valuable subjects for the in-depth study of ion diffusion kinetics in LCO-based synaptic transistors.[37,39]

The surface morphology captured by SEM confirmed the preferred orientation of the LCO films as shown in Figs. 3(a)-3(c). A square grain with a size of about 36 nm can be observed at the surface of the LCO (104) film, which is in good agreement with previous reports.[37,40] Rooftop-like structures are formed at the surface of the LCO (110) films with a compact structure. Additionally, triangle-like structures are formed at the surface of the LCO (003) films, which have faceted groove structures corresponding to grain boundaries. Figs. 3(d)-(f) gives the corresponding lattice models and macro characteristics for different orientations of LCO thin films. The native Li^+ ions diffusive paths for LCO (003) are parallel to the substrate surface, while those of (110) and (104) planes are almost normal to the substrate surface. Consequently, the LCO (110) and (104) thin films should exhibit a significantly reduced in-plane diffusion coefficient within the channel layer attributed to the limited transport rate of Li^+ ions through grain boundaries.[41,42] In contrast, LCO (003) should exhibit the maximum Li^+ diffusion capacity within the channel layer. Correspondingly, we observe a smaller memory window in the transfer curve of the LCO (003) device (see supplementary material Section 1).

To capture the lithium migration dynamics associated with charge transfer and interface impedance, we measured the drain-source impedance of LCO channels with different preferred orientations. As shown in Fig. 3(g), we employed an AC excitation signal with an amplitude of 50 mV at the source electrode, while the drain was grounded. The frequency range investigated was set between 0.1-10^6 Hz, which allowed us to observe and analyze the impedance behavior at a wide range of time scales. From the impedance spectra, it is evident that LCO (003) exhibits a smaller impedance arc, indicating a lower impedance for Li^+ ions diffusion and charge transfer within the channel layer. The Pt/LCO/Pt interdigitated electrode structure can be characterized as a circuit consisting of a capacitance (C) in parallel with a faradaic impedance (R).[43,44] By fitting the impedance spectra of varying LCO thin films as shown in Fig. S3, the R_{104}, R_{110} and R_{003} are calculated to be about 1.06×10^7 Ω, 1.06×10^7 Ω and 1.40×10^6 Ω, respectively (Table SI). These results are consistent with Xia et

al.'s report that the Li^+ diffusivity in LCO thin film with a (003) orientation is one order of magnitude higher than in the (104) oriented film.[45] Meanwhile, the fitting capacitance C_{003} shows a maximum value of 9.51×10^{-11} F, which means the LCO (003) channel is more likely to accumulate charges at the source/drain-channel interface. This is also directly observed by the KPFM tests conducted on LCO thin film devices with varying preferred orientations as shown in Fig. 3(h) (also see the KPFM measurements in supplementary material Section 2). We do observe the maximum electric field values and charge accumulation at the drain electrode interface in the LCO (003) channel layer, while fewer differences were observed in the other two orientations, which may be due to the vertically-standing Co-O layers blocking the migration of Li ions as shown in Figs. 3(a) and 3(b). A similar interfacial effect can be observed at the source terminal as shown in Fig. 3(i). These KPFM findings agree well with our Li^+ diffusion anisotropy model and impedance results.

2.4 The inhibited current spikes and reduced power consumption

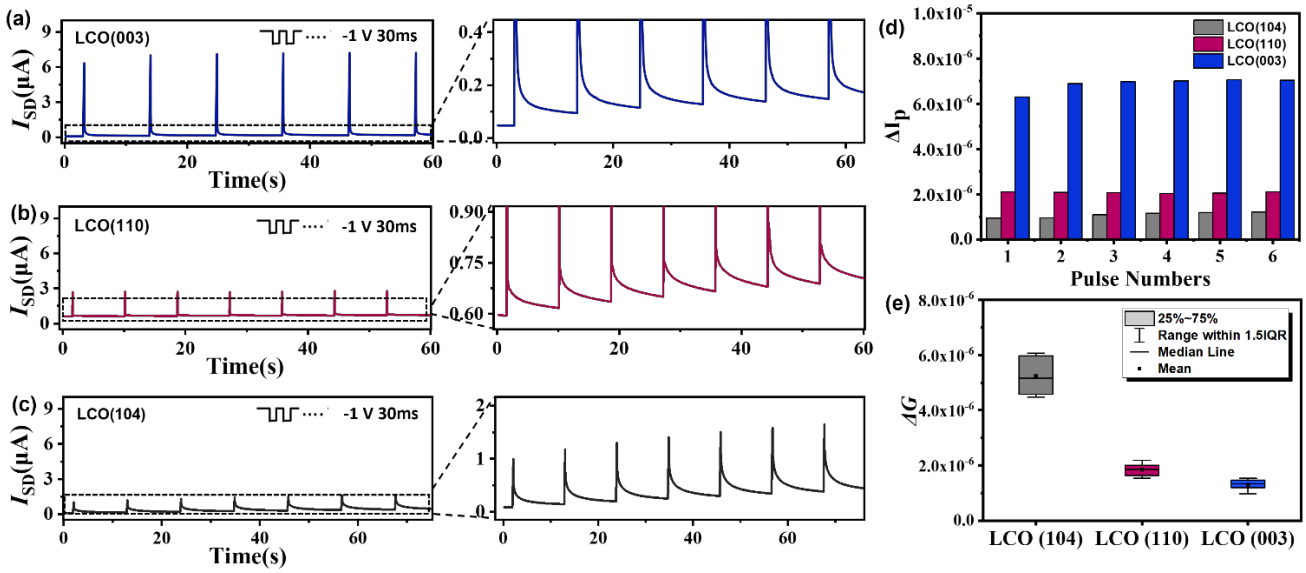

FIG 4. Non-volatile switching of channel conductance states during the LTP. Source-drain current (I_{SD}) as a function of time in (a) LCO (003), (b) LCO (110) and (c) LCO (104) synaptic transistor triggered by gate current pulse (-1 V for 30 ms), with the source-drain bias of 10 mV. (d) Post-synaptic currents peak value ΔI_p of six pulsed excitation processes in three different devices. (e) The statistical distribution of the conductance change ΔG versus the initial conductance induced by one gate current pulse.

Artificial synaptic transistors were fabricated on the high-quality epitaxial LCO thin film deposited at different STO substrates. To showcase the necessary multi-level states for analog computation, the LCO devices were operated by applying voltage pulse trains to the gate electrode. These pulse trains comprised a "write" operation,

characterized by a finite gate voltage pulse. During the operation, the I_{SD} current was measured with a constant source-drain bias of 10 mV. As shown in Figs. 4(a)-4(c), by alternatively applying a series of identical pulses, potentiation consisting of six EPSC-like processes was observed in devices of all orientations. The EPSC attained a peak value and decayed back to a new and higher conductance state, indicating the nonvolatility characteristic of LCO synaptic transistors. It is worth noting that the LCO (003) exhibits a high current spike, whereas this current spike is effectively suppressed in LCO (104) and LCO (110). The energy efficiency of devices calculated by $\Delta I_p = I_p - I_0$ in each EPSC event are shown in Fig. 4(d). The average peak value for LCO (003) is 6.87×10^{-6} A, whereas LCO (104) has a minimum value of 1.09×10^{-6} A. Since the "write" operation is decoupled from the "read" process, by which means the gate terminal is used for channel conductance modulation through driving ion into the electrolyte, and source/drain terminals for readout.[20,46] And the "write" current (gate current) is lower than the "read" current, the energy efficiency of the synaptic transistor is dominated by the "read" process.[47] Therefore, the energy consumption for a single pulse event can be calculated by $\Delta I_p \times V_{SD} \times t$, where t is the pulse duration.[48,49] As a result, the power consumption of LCO (104) is the lowest (approximately six times lower than that of LCO (003)) with a power consumption of 0.327 nJ per single pulse event. Since the energy consumption is proportional to the effective device area,[49] the areal energy consumption in this work is as low as 1.46 fJ μm^{-2}, demonstrating a superior performance compared to most reported devices utilizing lithium-ion and hydrogen-ion migration (see supplementary material Table SII). Moreover, the change of conductance ΔG after one pulse are shown in Fig. 4(e). LCO (104) exhibits a larger variation in the conductance change, indicating its increased susceptibility to external gate voltage. This can be attributed to the presence of a vertical diffusion channel [Fig. 3(d)], which allows for more efficient interaction between lithium ions and the electric field generated by the gate voltage. We also noticed that the performance of the LCO (110) devices is slightly inferior, which may be attributed to the presence of more grain boundaries in LCO (104) [Fig. 3(a)] that facilitate the longitudinal diffusion of lithium ions. The current reliability issues caused by defects, such as grain boundaries and vacancies, are a key focus in the pursuit of memristive devices for chip hardware applications. It has been reported that grain boundaries and dislocations can be used to confine conductive filaments into the one-dimensional channels, effectively enhancing the uniformity and durability of device switching, which in turn improves the accuracy of neural network recognition.[50] Furthermore, by introducing the large voids (0.542 nm), the spontaneous diffusion of Li^+ can be suppressed, and the synaptic device's resistance state exhibits fluctuations of less than 1% over more than 2000 cycles.[51] However, compared

to previous efforts in grain lattice defect[50] and micro-nanopore regulation[51], controlling ion diffusion in oriented channels within an intact crystal lattice offers better controllability and stability than the unorganized random diffusion across defects and along grain boundaries.[52] For layered $LiTMO_2$ (TM = Co, Mn…) channel materials, the two-dimensional diffusion channels of Li^+ result in anisotropic diffusion rates along different crystal orientations.[53,54] Regulating the crystal orientation and grain boundaries of channel layers will be the most direct way to reduce write energy consumption and enhance device performance.

2.5 Synaptic plasticity of LCO devices in ambient condition

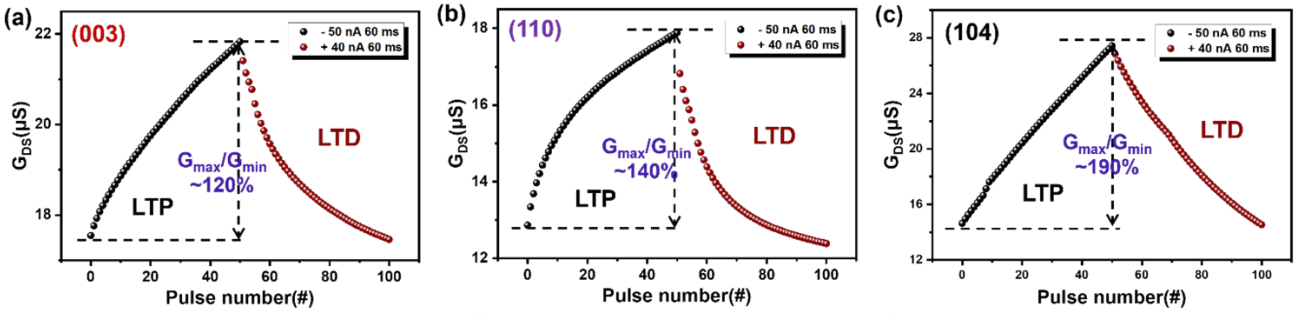

FIG. 5 Analog channel conductance modulation of LTP and LTD process in LCO (a) (003), (b) (110), and (c) (104) synaptic devices. The 50 repeated negative (-50 nA, 60 ms) and positive (40 nA, 60 ms) gate current pulses are applied.

LTP is widely recognized as a fundamental process underlying learning and memory operations in biological systems. In contrast, LTD is utilized to selectively weaken synapses and inhibit the further encoding of new information after LTP has occurred.[55] To demonstrate the multilevel analog conductance states as required to mimic the synaptic functionalities, the LTP and LTD in all three devices were studied. The devices were programmed by applying 50 negative gate current pulses (-50 nA, 60 ms) and positive gate current pulses (40 nA, 60 ms). The non-volatile change in channel conductance induced by each gate pulse was measured by applying a voltage pulse between the source and drain (0.1 V, 60 ms) as shown in Fig. 5. During LTP operation, Li^+ ions diffuse towards the gate and are partially captured by the SiO_x layer, increasing channel conductance. Similarly, when a positive current pulse is applied to the gate terminal (LTD), the returning Li^+ ions intercalate into the LCO, leading to a higher resistance. The conductance range (G_{max}/G_{min}) in LCO (003), LCO (110), and LCO (104) is about 120%, 140% and 190%, respectively, indicating lithium ions can be modulated easily along the out-of-plane direction in LCO (104) channel. The obtained results further prove the migration anisotropy of Li^+ ions in different grain orientations, which is consistent with the findings illustrated in the transfer characteristic curves (refer to supplementary material Section 1). Additionally, the LCO (104) samples exhibit

a conductance modulation process that is more linear and symmetrical. Furthermore, the high-temperature operation stability and environmental stability are important key factors affecting practical applications of synaptic transistors. To estimate the high-temperature resilience of LCO (104) synaptic device in the ambient environment, memory retention was also measured at elevated temperatures (see supplementary material Section 4). The charge retention time is more than 10^3 s for our device at 90 ℃, which demonstrates the improvement in terms of high-temperature retention and air stability compared to earlier reported synaptic devices.[28] This observation holds crucial significance for applications in neural network hardware identification, as it ensures more reliable and predictable behavior in the synaptic transistors.[51] These results highlight the potential of LCO-based devices for next-generation low-power electronic devices beyond the von Neumann architecture.

3. Conclusion

In summary, the synaptic transistors containing LCO channel layers with (104), (110) and (003) orientations were successfully prepared. The different orientation of the LCO channel layer leads to different in-plane Li^+ diffusion coefficients, with Li^+ migrating most rapidly in the in-plane direction in the LCO (003) channel layer. KPFM tests validated the model of lithium-ion accumulation at the drain interface, which significantly impacts the maximum peak current of the device. Impedance measurements and the corresponding charge distribution analysis confirmed that the LCO (003) film exhibited greater charge accumulation at the source/drain-channel interfaces compared to LCO (110) and LCO (104) films. This observation highlights the influence of film orientation on interfacial charge accumulation behavior. Through the fabrication of synaptic transistors incorporating LCO channel layers with different orientations, we achieved non-volatile switching of the devices, and the smallest EPSC current spike was achieved in the synaptic transistor with the LCO (104) channel. Significantly, our findings revealed that the LCO (104) devices exhibited the lowest power consumption, measuring at an impressively low value of 0.327 nJ. This result provides valuable insights into the underlying mechanisms governing the operation of MIECs devices, which in turn facilitates further improvements in their efficiency and functionality.

4. Experimental section

Polycrystalline LCO was deposited on silicon wafer substrates by using RF magnetron sputtering. The substrates used were highly doped p-type Si (100) with and without the amorphous silicon oxide layer (see supplementary material Section 1). The epitaxial LCO films with (003), (110) and (104) preferred orientations were grown on

the (111), (110) and (100) crystal planes of $SrTiO_3$ (STO) single crystal substrates, respectively. All LCO samples used in this study were deposited by using magnetron sputtering (Flow rate: 25 sccm O_2 + 25 sccm Argon; Areal power density: 30 W cm^{-2}; Deposition pressure: 0.5 Pa). The three-terminal LCO synaptic transistors were fabricated using the bottom-up synthesis method. Firstly, two parallel Pt electrodes were patterned on the substrate before the LCO channel layer was deposited, serving as source and drain electrodes. After the epitaxial LCO films were deposited on STO substrates, a ~80 nm amorphous SiO_x was deposited by reactive sputtering to cover the whole LCO channel area. Lastly, a Pt top electrode was patterned on top of the SiO_x dielectric layer as the gate electrode.

Supplementary Material

See the supplementary material for additional information about switching *I-V* curves of two-terminal Au/$LiCoO_2$/Si(p+) and Au/$LiCoO_2$/SiO_x/Si(p+) memristors, KPFM testing schematic, 2D surface potential difference distribution maps and surface potential profiles of different oriented LCO channels, transfer characteristic curves of synaptic transistors with different LCO preferred orientations, impedance fitting results of LCO films with different preferred orientations, ambient stability measurements of the LCO (104) synaptic devices.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Supplementary Material

Inhibiting the current spikes within the channel layer of $LiCoO_2$-based three-terminal synaptic transistors

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1. Contribution of Li^+ diffusion to the channel conductance

The trapping effect of Li^+ ions diffusion towards the gate on the channel conductivity variation was evaluated by studying the *I-V* hysteresis and transfer characteristic curves. Firstly, we fabricated the two-terminal memristor to evaluate the influence of Li^+ ions transportation and the trapping effect of the SiO_x layer on the device's memristive behaviours. As shown in Figs. S1(a)-(b), the Au/LCO/Si(p+) stack and Au/LCO/SiO_x/Si(p+) stack were prepared by magnetron sputtering. Interestingly, the Au/LCO/SiO_x/Si(p+) stack shows a bipolar memristive behaviour and obvious resistance switching. However, the Au/LCO/Si(p+) presents neglectable current hysteresis. These results confirm that SiO_x can work as a solid-state electrolyte allowing the transportation and trapping of Li^+ ions when external voltage is removed, and thus modulating the channel conductance.[S1, S2] Meanwhile, the conductance modulating capacity of the device is determined by the amount of Li^+ ions diffusion and captured by SiO_x.[S3]

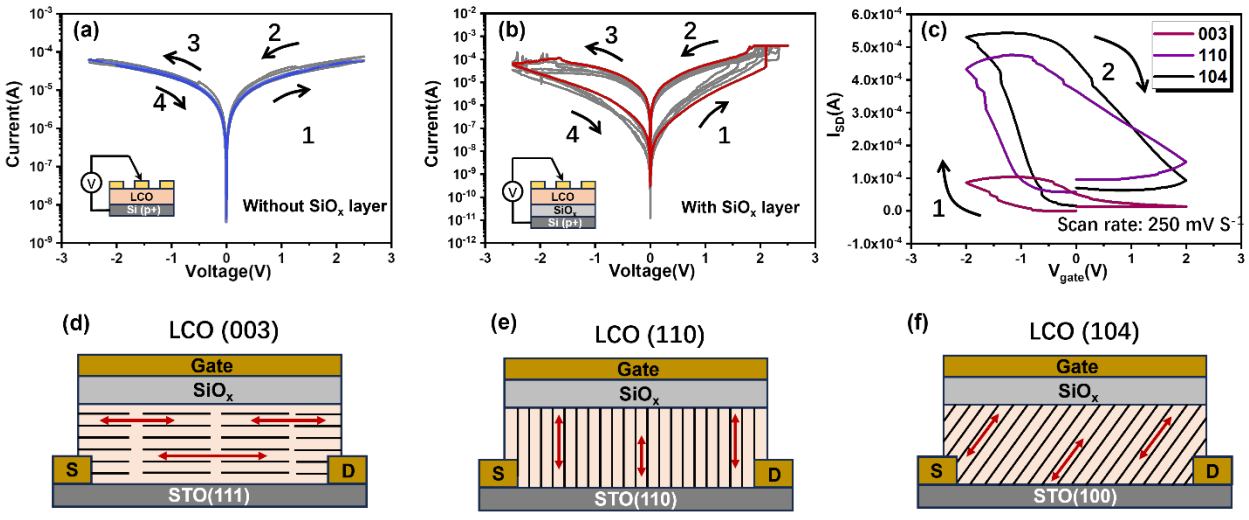

Figure S1 (a) *I-V* curves of the two-terminal Au/$LiCoO_2$/Si(p+) stack. (b) Switching *I-V* curves of the two-terminal Au/$LiCoO_2$/SiO_x/Si(p+) memristor. (c) Hysteretic transfer characteristic curves of synaptic transistors with various LCO orientations. The source-drain bias is 0.1 V and the voltage sweep rate is 250 mV s^{-1}.

The transfer characteristic curves of synaptic transistors with various LCO orientations are depicted in Figure S1(c). In all three devices, the channel current increased when the voltage sweep reached negative values, while decreased when the gate voltage swept to positive values, indicating a reversible switching of the channel from a high resistance state (HRS) to a low resistance state (LRS).

Interestingly, the LCO (003) device shows a small memory window (I_{max}/I_{min}) of about 4 and a high operating voltage of about -1.4 V. In contrast, the LCO (110) and LCO (104) show larger hysteresis loops and smaller switching threshold voltage (about -0.8 V and -0.6 V, respectively). This larger hysteresis can be attributed to the nonvolatile conductance change in the LCO channel. The magnitude of ion-induced hysteresis in LCO devices is directly related to the net ionic diffusion through the SiO_x layer which can be further explained by intrinsic different ion diffusion channels. As shown in the Li^+ ions migration model in Figs. S1(d)-(f). The LCO (104) and LCO (110) have the Li^+ ions diffusion channels (Co-O octahedra interlayers) almost perpendicular to the film surface, and the low lithium/electron diffusion energy barrier within the two-dimensional Co-O layers results in the low switching voltages and large memory windows.[S4] In contrast, the LCO (003) film surface is parallel to the Li^+ ions channels, the local redistribution of Li^+ ions must diffuse along the grain boundaries. At these grain boundaries, the high diffusion energy barrier of lithium-ions and low conductivity of electrons both contribute to the smaller memory window and higher threshold voltage.[S5]

2. Kelvin probe force microscopy (KPFM) measurements within oriented LCO channels.

To further investigate the interfacial charge accumulation between the source and drain electrodes, the KPFM testing was performed within different oriented LCO channels. As shown in Fig. S2(a), the platinum source and drain electrodes (with a thickness of about ~60 nm) were fabricated by photolithography on the $SrTiO_3$ (STO) substrates with <100>, <110>, and <111> orientations, followed by the deposition of ~70 nm thick $LiCoO_2$ (LCO) layers with (003), (110) and (104) orientations in the channel area, respectively.

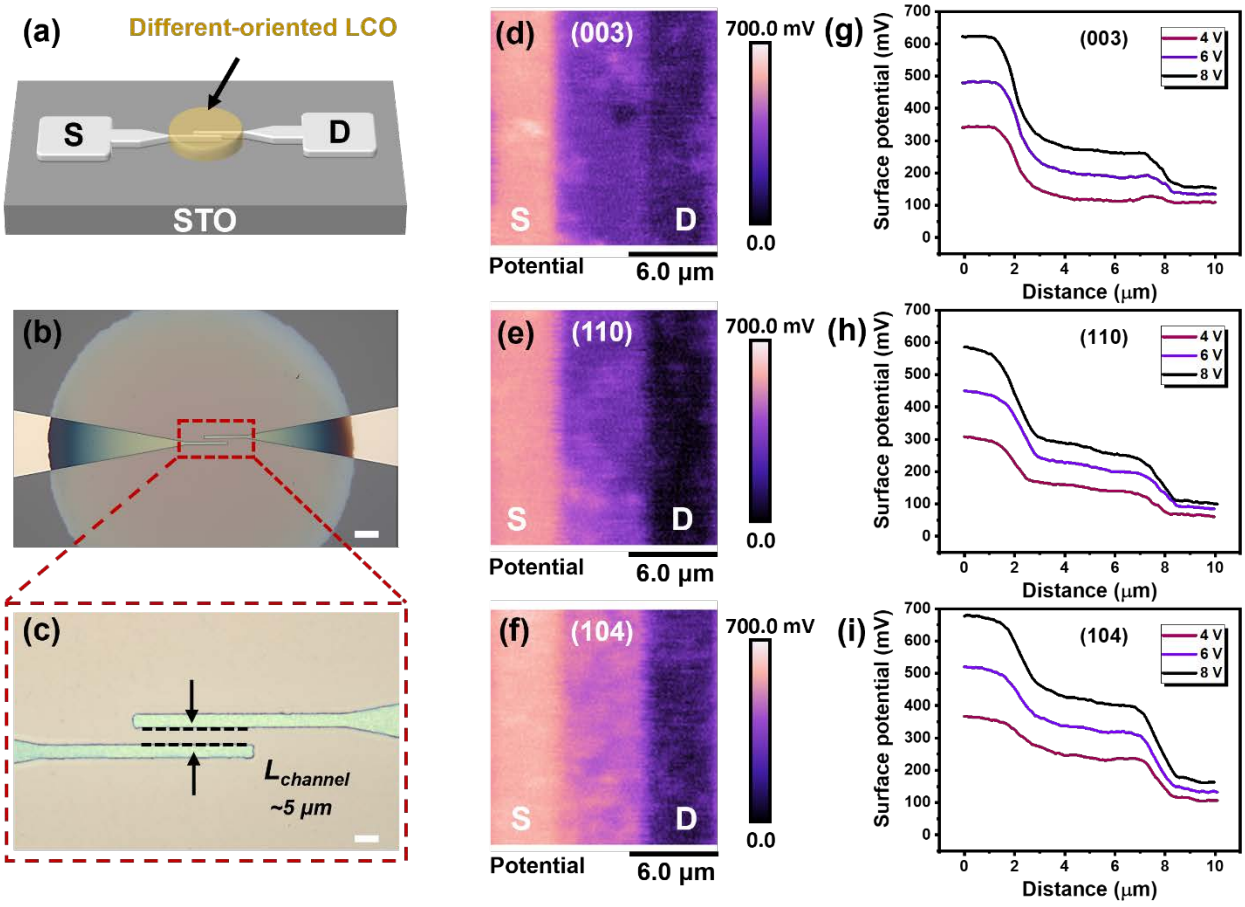

Figure S2 (a) Schematic diagram of the KPFM testing devices. (b) Optical micrograph of KPFM testing device with a channel length of 5 μm and (c) the corresponding enlarged view of the channel area. The scale bars are set at 40 μm and 5 μm, respectively. (d)-(f) 2D surface potential difference distribution map of a channel with the LCO orientations (003), (110) and (104). The drain is grounded and source with a constant bias of 6 V. (g)-(i) The surface potential profiles across the LCO (003), (110) and (104) channels at various source voltages (4V, 6 V, 8 V) when the drain is grounded.

Figs. S2(b)-(c) display the optical image of KPFM testing device with a channel length of 5 μm. KPFM measurements were carried out under a source-drain bias (V_{SD}) of 4 V, 6 V and 8 V with the drain electrode grounded. In Figs. S2(d)-(f), we demonstrate the corresponding surface potential mapping at V_{SD} = 6 V. A visible spatial gradient of the surface potential from source (brighter region) to drain (darker region) indicates a flow of channel current between source and drain.[S6] Moreover, as can be seen in the profiles of average surface potential (Figs. S2(g)-(i)) along the source to drain electrode under varying positive voltage polarizations at the source electrode, the LCO channel with (003) preferred orientation shows the highest surface potential drop at the source-channel junction among three orientations, indicating the existence of shielding effect of the lithium-ions at the source-channel junction that greatly reduced the potential applied at the Source electrode.

3. Impedance spectroscopies of LCO channels with different crystal orientations.

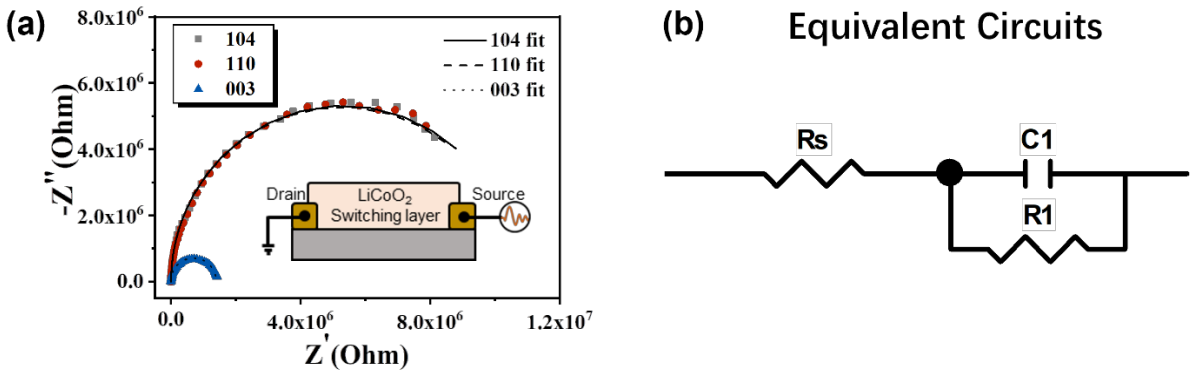

Figure S3 (a) Impedance spectroscopy at varying orientations in the range of 0.1-106 Hz. The inset diagram is a schematic of the impedance test. (b) Equivalent circuit for fitting impedance profile.

Table SI Impedance fitting results of LCO films with different preferred orientations

	LCO (003)	LCO (110)	LCO (104)
$R_s(\Omega)$	1198.0	992.4	748.1
$R_1(\Omega)$	1.4002e-6	1.0599e-7	1.0632e-7
$C_1(F)$	9.5162e-11	8.3452e-11	7.686e-11

4. Ambient stability of the LCO (104) synaptic devices.

High-temperature operation and environmental stability are important key factors affecting practical applications of synaptic transistors. To estimate the high-temperature resilience of LCO (104) synaptic device in the ambient environment, memory retention was measured at elevated temperatures without packaging protections, as shown in Fig. S4a. The charge retention time is more than 10^3 s for our device at 90 ℃, which demonstrates great improvement in terms of high-temperature stability and memory retention compared to earlier reports on relative synaptic devices.[S3, S7] Moreover, we also estimate the ambient stability by long-term synaptic plasticity of via testing the same device after one week. As shown in Fig.S4b, the LCO-based synaptic transistor almost retains the initial LTP-LTD conductance modulation characteristics, such as memory window and linearity. Meanwhile, $LiCoO_2$ is relatively stable in air and moisture sensitivity compared with other lithium transition metal oxides ($LiTMO_2$, TM = Fe, Co, Ni, Mn, etc.), and has been successfully commercialized.[S8, S9] It is worth mentioning that our tests were conducted in atmospheric environments (Fig. S4c), and it is expected that the packaged device will further enhance the environmental stability.

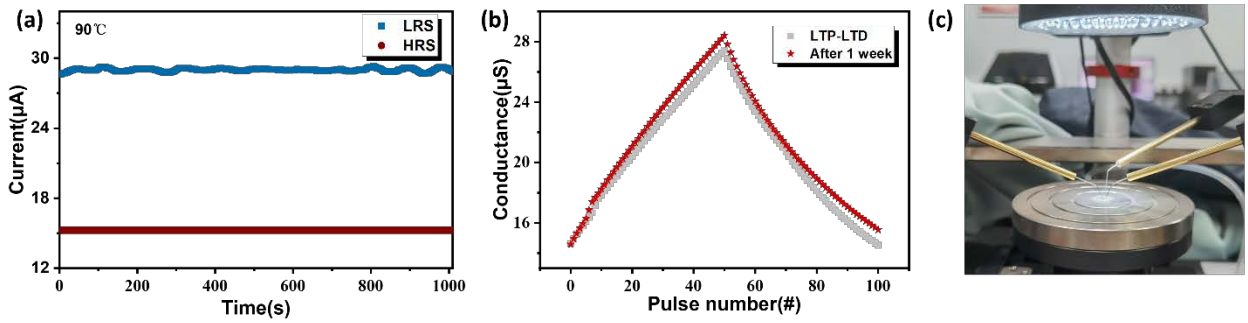

Figure S4 (a) State retention of LCO (104) devices at 90 ℃ under atmospheric environment. (b) LTP-LTD conductance modulation reproducibility test for synaptic devices after exposure to atmospheric environment for one week. (c) Photograph of the LCO synaptic transistor tested under atmospheric environment.

Table SII Comparison of the energy consumption for Li^+/H^+ based synaptic devices.

Active layer	Electrolyte	Active ions	Pulse amplitude	Pulse width	Energy consumption	Ref.
Carbon nanotube	PEG	H^+	5 V	1 ms	31.2 fJ/um^2	[S10]
WO_3	Nafion	H^+	500 nA	5 ms	0.39 fJ/um^2	[S11]
WO_3	LiPON	Li^+	10 μA	10 ns	100 fJ/um^2	[S12]
NDI-gTVT	$LiClO_4$/PEO	Li^+	1 V	0.04 s	7.42 pJ/um^2	[S13]
VO_2	DEME-TFSI	H^+	1.5 V	200 ms	0.21 fJ/um^2	[S14]
WSe_2	$LiClO_4$/ PEO	Li^+	5 V	50 ms	10 fJ/um^2	[S15]
Graphene	$LiClO_4$/ PEO	Li^+	50 pA	10 ms	13.9 fJ/um^2	[S16]
α-MoO_3 nanosheets	$LiClO_4$/ PEO	Li^+	2.5 V	1 ms	~ 4 fJ/um^2	[S17]
HfO_2/Si	$LiClO_4$/ PEO	Li^+	0.05 V	50 ms	~4.68 pJ/um^2	[S18]
α-MoO_3	EMIM-TFSIf	H^+/OH^-	2.5 V	1 ms	~480 fJ/um^2	[S19]
IZO	SiO_2	H^+	0.3 V	10 ms	45 pJ/um^2	[S20]
In_2O_3	$Li_xAl_2O_3$	Li^+	2.5 V	50 ms	63 fJ/um^2	[S21]
α-Nb_2O_5	Li_xSiO_2	Li^+	3.6 V	10 ms	20 fJ/um^2	[S22]
$LiCoO_2$	SiO_x	Li^+	4 V	5 μs	~ 8 fJ/um^2	[S23]
$LiCoO_2$	SiO_x	Li^+	50 nA	60 ms	1.46 fJ/um^2	**This work**

Supplementary references

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