

ROTA-I/O: Hardware/Algorithm Co-design for Real-Time I/O Control with Improved Timing Accuracy and Robustness

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Abstract—In safety-critical systems, timing accuracy is the key to achieving precise I/O control. To meet such strict timing requirements, dedicated hardware assistance has recently been investigated and developed. However, these solutions are often fragile, due to unforeseen timing defects. In this paper, we propose a robust and timing-accurate I/O co-processor, which manages I/O tasks using Execution Time Servers (ETSs) and a two-level scheduler. The ETSs limit the impact of timing defects between tasks, and the scheduler prioritises ETSs based on their importance, offering a robust and configurable scheduling infrastructure. Based on the hardware design, we present an ETS-based timing-accurate I/O schedule, with the ETS parameters configured to further enhance robustness against timing defects. Experiments show the proposed I/O control method outperforms the state-of-the-art method in terms of timing accuracy and robustness without introducing significant overhead.

I. INTRODUCTION

Input/Outputs (I/Os) are a vital part of safety-critical systems [1], [2], [3], as these systems rely on I/Os to interface with sensors and actuators that need to either perceive a hazard in time or make manoeuvres to avoid a hazardous situation [4]. For instance, spacecraft attitude control systems rely on precise and time-sensitive I/O operations to obtain and adjust the attitude of the spacecraft [5], while autonomous vehicle engines depend on accurate I/O tasks for optimal fuel injection [6]. A lack of I/O accuracy often leads to imprecise control of devices and less effective environmental readings being collected [7]. Hence, it is necessary to ensure that I/O operations behave correctly: (i) with *timing accuracy* – being executed at exact time instants (or at least within a small margin) to achieve precise control [8], [7]; and (ii) with *robustness* – having the capability to deal with unexpected timing defects to maximise control accuracy [9], [10], [11].

In industry, timing-accurate and robust I/O control is mandated by many globally recognised safety standards, including ISO 26262 [1] and DO-178C [12]. As explicitly stated in clause 4 of ISO 26262, “I/Os (e.g., sensors and actuators) must exhibit correct timing, accuracy, and robustness” [1]. Additionally, clause 6 of the standard elaborates on the system-level failures that can arise from timing defects in I/O control, underscoring the importance of such requirements.

However, achieving timing accurate I/O control is ever-challenging due to unexpected timing defects, including ill-defined I/O-centric calculations [13], underestimated WCET, and transient failures triggered by harsh environments, as

recognised by Davids and Burns [9] in typical safety-critical systems. These unforeseen timing defects [14] can fundamentally compromise I/O’s timing accuracy by disrupting the well-arranged precise execution sequences of I/O tasks (e.g., produced by methods in [15], [16], [17], [18], [8], [7]), and subsequently, cascading disruptions throughout the I/O, leading to system failures and even catastrophic consequences [1].

Software approaches that consider timing accuracy (e.g., [16], [17], [18]) often provide carefully-planned I/O schedules on easily analysable platforms, e.g., uniprocessors and partitioned systems using isolation. However, these methods have proven to be extremely difficult to achieve for both timing accuracy and robustness on modern platforms, due to ever-increasing hardware and architectural complexities. On such platforms, the significant uncertainty about I/O transmissions, e.g., communication delays and resource contentions [19], [20], [21] occurring from software applications (instigation) to hardware devices (execution) [8], can directly disable any pre-planned schedule with an expected task arrival time.

Hardware approaches [22], [23], [8], [7] usually employ dedicated assistants to manage I/O operations in proximity to the devices. By bringing stringent scheduling close to the devices, these approaches mitigate transmission uncertainty, ensuring timing accuracy under some use cases. However, to realise such management, these solutions rely on an idealistic assumption that “*the timing behaviours of the I/O operations must be well-defined*” [8], [7]. For systems with timing defects, the scheduling produced by the above approaches would be entirely violated (as explained above). Thus, in more realistic application scenarios, it is important, but also challenging, to achieve timing-accurate and robust I/O management.

Contributions. In this paper, (i) we propose a device-coupled co-processor (*ROTA-I/O*) that manages I/O operations directly at the hardware level, featuring configurable Execution Time Servers (ETSs) and a scalable two-level scheduler. The ETSs provide temporal isolation between I/O tasks, prohibiting defect propagation. The scheduler dispatches I/O operations hierarchically using the ETSs, establishing a scheduling infrastructure. (ii) With the new hardware, we present an ETS-based scheduling method (namely *ROTA-Sched*) that schedules I/O tasks and configures the ETSs, achieving real-time I/O control with accuracy and robustness. (iii) We built a systematic full-stack framework from the System-on-Chip (SoC) to the Instruction Set Architecture (ISA) and programming model, forming a complete solution for real-time I/O control.

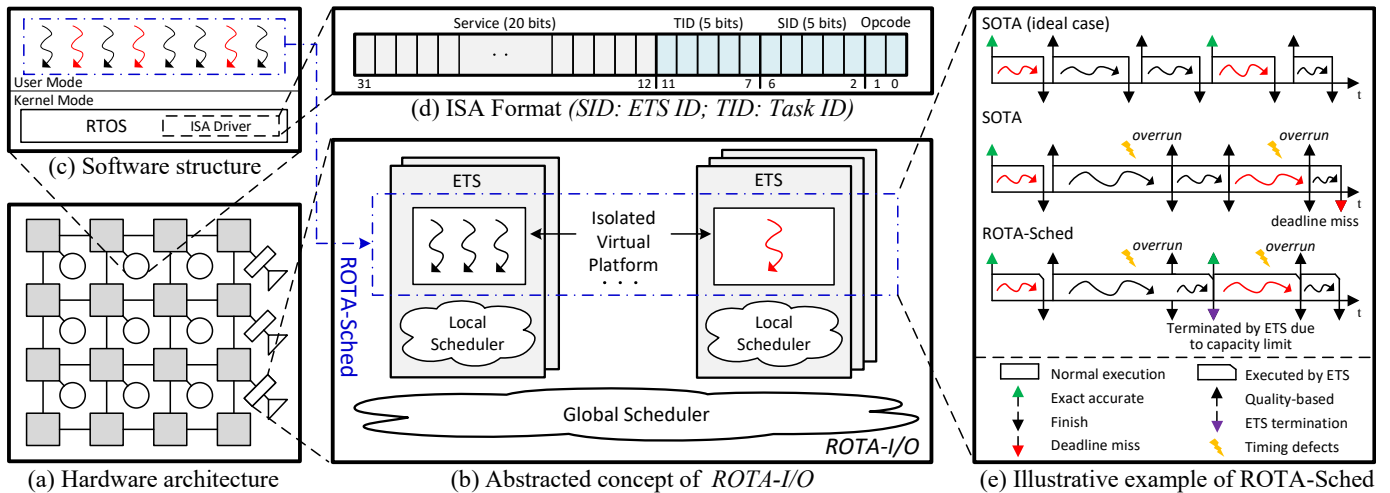


Fig. 1: A conceptual overview of *ROTA-I/O* (square: router; circle: core; rectangle: *ROTA-I/O*; triangle: device; curved arrows: tasks with different timing guarantees; ETS: Execution Timer Server): (a) *ROTA-I/O* serves as a co-processor, enabling I/O management at hardware; (b) *ROTA-I/O* features sets of ETSs and a two-level scheduler, limiting the impact of timing defects while offering a configurable scheduling infrastructure; (c) *ROTA-Sched* schedules tasks and configures *ROTA-I/O* using (d) the dedicated ISA; (e) an illustrative mechanism of *ROTA-Sched*, improving I/O robustness and accuracy.

We deployed our proposed solution on the Xilinx VC709 FPGA and examined it using various metrics. Experimental results show that compared to State-of-the-Art (SOTA) real-time controllers, *ROTA-I/O* improves acceptance ratio and control quality by 22.61% and 42.32% respectively, on average (maximum: 2.18x and 3.06x). Synthesising a *ROTA-I/O* yields less than 3% hardware overhead of a full-featured processor. **Organisation.** Sec. II describes the overview of *ROTA-I/O*. Sec. III presents the architectural design of *ROTA-I/O*. Based on the hardware, the *ROTA-Sched* is proposed in Sec. IV. Sec. V presents the experimental results. Finally, Sec. VI provides the related work, and Sec. VII concludes the paper.

II. *ROTA-I/O*: OVERVIEW

A. Top-level Concepts

To achieve timing-accurate and robust control for the I/Os, we adopted a hardware/algorithm co-designed approach (Fig. 1) that tightly couples I/O management to the devices and enables hierarchical scheduling with temporal isolation. Below, we detail the design and scheduling concepts.

Design concepts. We designed the I/O co-processor (*ROTA-I/O*) with groups of Execution Time Servers (ETSs) and a two-level scheduler (Fig. 1(b)). The ETSs manage the I/O tasks and establish an isolated environment for their execution, effectively realising dedicated Virtual Platforms (VP) for task execution [24], [25]. With the two-level scheduler, I/O tasks are prioritised in a hierarchical manner: a *global scheduler* distributes the time budget from the physical platform to the VPs and determines the *scheduling parameters* (see scheduling concepts) of the VP in each ETS; each ETS then has a *local scheduler* to prioritise the tasks allocated to that VP using the distributed budget. The design concepts have the following properties to ensure timing-accurate and robust I/O control:

TABLE I: Examples of the ISA for *ROTA-I/O* control (*Priv: 1 and 0 indicate the kernel and user modes, respectively*).

Instruction	Priv	Description
c.set , rs1, rs2	1	Set rs1 budget to ETS rs2.
c.enr , rs1, rs2	1	Enroll ETS rs2 with a start time of rs1.
p.ld , rs1, rs2	0	Pre-load the task addressed in rs1 to ETS rs2.
i.ld , rs1, rs2	0	Imm-load the task addressed in rs1 to ETS rs2.
i.run , rs1	0	Run the pre-loaded task addressed in rs1.

- *ROTA-I/O* facilitates the I/O management being tightly coupled with the devices. This effectively bypasses most of the uncertainty associated with I/O transmissions.
- The ETSs handle I/O tasks independently, which provides temporal isolation, hence the propagation of unexpected timing defects on the system is prevented.
- The two-level scheduler is responsive to the system and environmental changes: for changes to one I/O task, the corresponding ETS can be configured and updated locally, without affecting the remaining systems; for changes to the taskset, the ETS-based allocation and schedule of I/O tasks can be updated globally.

Scheduling concepts. With the new hardware design, an ETS-based scheduling algorithm (*ROTA-Sched*) was developed to configure the ETSs and coordinate the executions of I/O tasks on the ETSs. For a given I/O taskset, the algorithm determines the parameters for the ETSs, including the start time, budget, etc. This information is used by the global scheduler to manage the executions of the ETSs. The task execution order in each ETS is then produced by *ROTA-I/O*. If the budget of an ETS has been exhausted due to timing defects, the scheduler will terminate its tasks to mitigate the impact of timing defects on the following ETSs, so that both robustness and timing accuracy can be guaranteed.

B. ISA Support

In coping with the reconfigurable characteristics of *ROTA-I/O*, we developed a dedicated ISA to abstract control interfaces for the software, where the instructions are classified into three categories (see Tab. I): *c*-type instructions ($c.x()$) for ETSs' configurations, *i*-type instructions ($i.x()$) for tasks requiring immediate-loading, and *p*-type instructions ($p.x()$) for tasks requiring pre-loading. For instance, $c.set()$ and $c.enr()$ respectively assign the time budget and the start offset of an ETS, whereas both $p.ld()$ and $i.ld()$ are used for loading I/O tasks. The main distinction between these loading instructions lies in their operational scope: $i.ld()$ includes both the I/O operations and their scheduling parameters, facilitating immediate task execution. By contrast, $p.ld()$ loads only the I/O operations, with task execution delayed until the scheduling parameters are defined by $i.run()$ (see Sec. IV-C for details). Given that the $c.set()$ can cause device contention and bus congestion, it is designed as a privileged instruction, executable only by an operating system (OS) or a hypervisor with a global view of the system.

To ensure ISA coding and decoding efficiency, we standardised a uniform format for these instructions. Fig.1(d) demonstrates the ISA format in four sections: the bottom 2 bits serve as the opcode, indicating the instruction type; the subsequent 10 bits represent the operated ETS and tasks; and finally, the top 20 bits convey specific service information.

C. Programming Model

With the new ISA introduced above, *ROTA-I/O* can be programmed through three phases, *i.e.*, initialisation, execution, and adaptation. In the initialisation phase, *ROTA-Sched* first determines the ETS parameters, *ROTA-I/O* then configures the ETSs using $c.set()$ and $c.enr()$, with I/O tasks being pre-loaded via $p.ld()$. In the execution phase, processors send run-time I/O tasks to *ROTA-I/O* using $i.ld()$ or trigger the pre-loaded tasks using $i.run()$, *ROTA-I/O* then manages these tasks according to the given configurations. Moreover, when a change occurs in the environment or the system, *e.g.*, the increased arrival rate of a task, an adaptation will be triggered, where *ROTA-Sched* is invoked to identify the affected ETSs and reconfigure their scheduling parameters using $c.set()$.

D. Integrating *ROTA-I/O* into a SoC

Deploying *ROTA-I/O* shifts I/O management from the OS kernel (as in conventional embedded/computer architectures) to the hardware, resulting in architectural changes. Fig.1(a) depicts the integration of *ROTA-I/O* in a multi-/many-core SoC. Specifically, the *ROTA-I/O* is physically connected to the device, establishing a scheduling infrastructure for accurate and robust control. We also connect *ROTA-I/O* to the home port of a router via physical links to construct communication channels and timing synchronisation with processors. Through these connections, tasks running on the processors can inter-communicate with *ROTA-I/O* utilising the ISA in Section II-B.

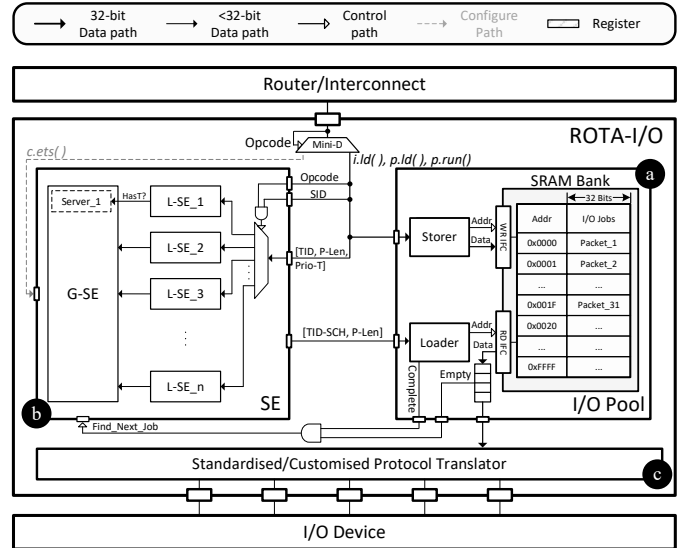


Fig. 2: Top-level micro-architecture of *ROTA-I/O* (*Mini-D*: mini decoder; *Prio-S/T*: priority of server/task; *TID*: task ID; *TID-SCH*: scheduled *TID*): **a** tasks are maintained in an SRAM-based I/O pool, allowing prioritisation; **b** nested schedulers prioritise the I/O tasks hierarchically; **c** scheduled tasks are translated into physical signals for the device control.

At the software level, we deploy a Real-Time Operating System (RTOS) in the kernel space, offering a real-time environment for applications that require timing guarantees (see Fig. 1(c)). Given *ROTA-I/O*'s comprehensive I/O management, we replace the default I/O manager within the RTOS using a new ISA-compatible driver, providing abstract access interfaces for the applications. The implementation of the driver is straightforward. This forwards tasks and the scheduling parameters of ETSs (*e.g.*, the period and the budget of an ETS) to *ROTA-I/O* by interpreting the ISA. Evidently, *ROTA-I/O* provides the key to guaranteeing I/O timing accuracy and robustness against unexpected timing defects. We now detail the micro-architecture of *ROTA-I/O*.

III. *ROTA-I/O*: MICRO-ARCHITECTURE

The *ROTA-I/O* design introduces a set of ETSs and a two-level scheduler, limiting the propagation of timing defects and constructing a configurable scheduling infrastructure. The top-level micro-architecture of *ROTA-I/O* is depicted in Fig. 2, consisting of three key components: an I/O pool, a Scheduling Engine (SE), and a protocol translator. The I/O pool (Fig. 2. **a**) buffers I/O tasks loaded by the processors and supports random access to them, allowing task prioritisation. The SE (Fig. 2. **b**) creates two nested priority queues to schedule I/O tasks in a hierarchical manner. The translator (Fig. 2. **c**) interprets I/O tasks into specific control signals in the physical layer. As the *ROTA-I/O* micro-architecture is designed to be compatible with various underlying protocol translators, either standardised or customised translators can be directly instantiated. Next, we introduce the design details of the I/O pool and the SE.

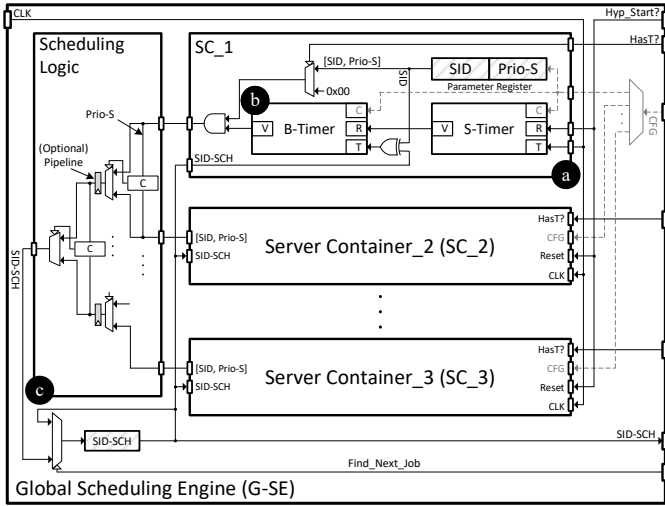


Fig. 3: G-SE micro-architecture (refer to Fig. 2 for legends; *SID-SCH*: scheduled ETS ID; *C*: comparator): **a** SCs are one-to-one associated to an ETS, featuring a parameter register to maintain the ETS’s priority, and **b** a pair of count-down timers to manage the budget; **c** the ETSs’s status is collected and prioritised, and the results are broadcasted to L-SEs.

A. I/O Pool

The micro-architecture of the I/O pool (Fig. 2. **a**) contains a dual-port SRAM, a pair of SRAM controllers and a FIFO queue. The SRAM stores the I/O tasks, decomposed as specific I/O operations. We use the memory address (12 bits) to index these I/O operations – the upper 7 bits represent the Task ID (TID), and the lower 5 bits give the release order of I/O operations with the same TID. We connect the SRAM controllers to each of the SRAM ports, behaving as a storer and a loader. During execution, when the I/O pool receives a `p.ld()` or an `i.run()` instruction, the payload will be written into the corresponding addresses of the SRAM using the storer. In addition, when the I/O pool receives the task ID scheduled by the SE, the I/O operations will be read from the SRAM using the loader and are then pushed into the FIFO queue for subsequent execution by the protocol translator.

B. Scheduling Engine (SE)

The micro-architecture of the SE (Fig. 2. **b**) constructs two nested priority queues: an upper-level one, *i.e.*, Global SE (G-SE), prioritises ETSs, deciding which ETS can execute the I/O task at a specific time point, while a lower-level one, *i.e.*, Local SE (L-SE), prioritises the I/O tasks within an ETS, executing them according to their priority.

Global SE (G-SE). We designed the G-SE (Fig. 3) using a collection of Server Containers (SCs) and scheduling logic. The SCs are *logically one-to-one* linked to with an ETS, maintaining the priority and time budget of the ETS. In each SC (Fig. 3. **a**), a dedicated parameter register is employed to store the Server ID (SID) and priority of the ETS. In addition, a pair of count-down timers are deployed to manage the time

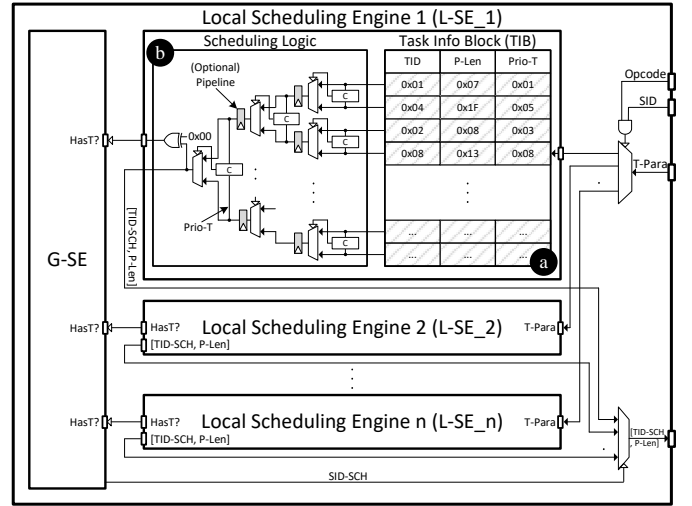


Fig. 4: L-SE micro-architecture (refer to Fig. 2 for legends; *T-Para*: task parameters; *TID-SCH*: scheduled task ID): **a** task parameters in the same ETS are stored in a TIB, implemented using a register chain; **b** all entries of the TIB are compared, identifying the task with the highest priority and returning the TID to G-SE, forming the final scheduling decision.

budget assigned to the ETS — a Budget-Timer (B-Timer) holds the ETS’s time budget, and a Start-Timer (S-Timer) maintains the refresh time point within each hyper-period (Fig. 3. **b**). Inside each timer, two registers are deployed to store the reset and current values. At the interfaces, three input ports and one output port are introduced. The input ports are used to program, reset and trigger the timer, and the output port reveals the status of the timer, *i.e.*, whether the current value is greater than ‘0’. With that, the timer’s reset value can be updated using the `c.cfg()` instruction through its program port; the timer’s current value is reset when its reset port equals ‘0’, and reduced by one when its trigger port meets a *rising edge*. To refresh an ETS with a preserved budget, the reset values in S-Timer and B-Timer are set as the refresh time point and the time budget (by *ROTA-Sched* in Sec. IV). We link the B-Timer’s reset port to the S-Timer’s status port, and the S-Timer’s reset port to the global clock. This resets the S-Timer at the start of every hyper-period and resets the B-Timer when the S-Timer counts to ‘0’.

The scheduling logic collects the status of the ETSs and prioritises them. To achieve this, the SC register is aggregated with the B-Timer output using an AND gate, which checks whether the SC is supplying enough time budget for its associated ETS. If the ETS has enough time budget, the SID and priority of the ETS are returned; otherwise, 0 is returned. The scheduling logic utilises pure combinational circuits to compare filtered results (Fig. 3. **c**), selecting the SC and routing its SID to the L-SEs in a fixed cycle.

Local SE (L-SE). We designed the L-SE (Fig. 4) using a Task Info Block (TIB) and scheduling logic. The TIB records the parameters of the tasks buffered in the ETS, decomposed

from the header of the `p.ld()` and `i.run()` instructions, including TID, P-Len and priority (Fig. 4. **a**). We implement the TIB using a register chain to allow parallel accesses. The scheduling logic deploys combinational circuits to collect the task parameters from the TIB and prioritises them (Fig. 4. **b**), returning the TID of the task with the highest priority. Lastly, a multiplexer is employed to gather scheduling results from both the G-SE and L-SE. The outputs of the L-SEs and the G-SE are connected to the multiplexer’s data ports and control port, respectively, forming the final scheduling decision.

C. Design Trade-Offs

Using a two-level micro-architecture to design the scheduler ensures scalability, providing the opportunity to extend its capacity for handling more ETSs, so that the developer only needs to deploy additional L-SEs and SCs (in the G-SE) to manage the introduced contentions. As the L-SE and SC are encapsulated in dedicated hardware modules and initialised independently, their integration will not introduce significant critical paths. However, as increasingly more modules are integrated, critical paths may emerge due to the heightened complexity of prioritisation. A practical solution to address this issue is to incorporate pipeline stages in the scheduling logic, as demonstrated in Fig.3. **c** and Fig. 4. **b**.

To further improve resource efficiency, it is possible to develop a *monolithic* scheduler to manage all tasks collectively. However, this approach would result in a substantial increase in combinational logic, potentially causing critical paths. This becomes particularly pronounced when scaling the scheduler to support more ETSs, ultimately compromising system-wide scalability. In Sec. V-E, we provide a quantitative analysis demonstrating that the proposed micro-architecture can be scaled without leading to any critical paths.

In Sec. V-E, we provide a quantitative analysis demonstrating that the proposed micro-architecture can be scaled to support over 32 cores, without bringing any critical path.

IV. *ROTA-Sched*: AN ETS-BASED SCHEDULE

This section presents the ETS-based schedule (*ROTA-Sched*) constructed based on the *ROTA-I/O*. By utilising the ETSs provided by *ROTA-I/O*, the *ROTA-Sched* allocates and schedules the *I/O* jobs in a hyperperiod on ETSs to mitigate the impact of interference caused by timing defects [26], [9], [27], improving both timing accuracy and robustness of *ROTA-I/O*. The *ROTA-Sched* is constructed based on the system model in Sec. IV-A with two major steps: (i) allocation and scheduling of jobs in ETSs, and (ii) configuration of scheduling parameters of ETSs. The first step (Sec. IV-B) produces a job-level schedule for *I/O* tasks which provides timing predictability and improved accuracy. The second step (Sec. IV-C) determines the scheduling parameters for ETSs to further mitigate the impact of timing defects on *I/O* jobs, enhancing the robustness of *ROTA-I/O*. With the two steps, we provide a complete ETS-based scheduling solution that achieves robust and timing-accurate *I/O* control. Notations introduced in this section are summarised in Tab. II.

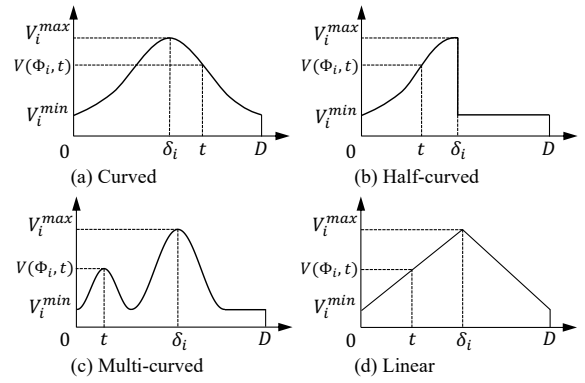


Fig. 5: Example timing-accurate models of *I/O* tasks (*x*-axis: time relative to the release of a task; *y*-axis: the resulting *I/O* control quality given a time instant *t*).

A. System Model

The system has n periodic *I/O* tasks, denoted $\Gamma = \{\tau_1, \tau_2, \dots, \tau_n\}$, where each task contains a series of sequential *I/O* operations on *ROTA-I/O*. An *I/O* task is defined by $\tau_i = (C_i, T_i, D_i, \delta_i, \Phi_i)$, in which C_i is the worst-case execution time; T_i is the period; D_i is the deadline with $D_i = T_i$; δ_i denotes the ideal start offset of τ_i that achieves the maximum *I/O* operation quality, *i.e.*, the exact timing accuracy; and Φ_i is the timing-accurate model associated with τ_i .

In a hyper-period T^H of the system, a task τ_i can raise up to $N_i = T^H \setminus T_i$ jobs, denoted as $\{\tau_i^1, \tau_i^2, \dots, \tau_i^{N_i}\}$. Notation τ_i^j is the j^{th} job of τ_i , which has a release time of $r_i^j = T_i \times (j - 1)$, a deadline of $d_i^j = r_i^j + D_i$, an ideal start offset of $\delta_i^j = T_i \times (j - 1) + \delta_i$, and an actual offset θ_i^j determined by *ROTA-Sched*. Jobs on *ROTA-I/O* are executed under a list schedule non-preemptively.

Timing-accurate Model. Different from [7], which uses a global timing-accurate model for all tasks to quantify the operation quality, tasks in this work can have different models. Fig. 5 presents four example timing-accurate models. For instance, Fig. 5(a) shows a typical timing-accurate model [28], [29] that can be found in fuel injection in control systems [6] and the data sampling in automotive systems [30]. Fig. 5(b) depicts a model for systems with more strict timing requirements, *e.g.*, the radar scanning in a supersonic fighter [31]. To reflect this generality, we let function $V(\Phi_i, t)$ denote the quality of τ_i (and its jobs) based on Φ_i and a start time t . Task τ_i yields the maximum *I/O* control quality if it starts at the ideal time, *i.e.*, $V_i^{\max} = V(\Phi_i, \delta_i)$. We assume that Φ_i has a single time instant that leads to the exact timing accuracy, and all jobs of τ_i share the same Φ_i . In addition, a predictable *I/O* task can obtain a minimal quality of V_i^{\min} (*e.g.*, $V_i^{\min} = V(\Phi_i, D_i)$), and a deadline miss leads to zero quality or a negative penalty value.

ETS Model. As described in Sec. II, the tasks in the *ROTA-I/O* are executed using the ETSs to prevent the propagation of timing defects between tasks in two ETSs. An ETS in *ROTA-I/O* is defined by $S_k = \{T_k, \lambda_k, \alpha_k\}$, in which T_k gives the

Algorithm 1: ETS-based I/O allocation and schedule.

```

1 ▷ Decomposing confliction graphs
2 while  $\|E\| > 0$  do
3    $\tau_i^j = \operatorname{argmax}_{i,j} \{\zeta_i^j \mid \forall \tau_i^j \in \mathcal{G}\};$ 
4    $\mathcal{G}_x = \mathcal{G} \setminus \tau_i^j;$ 
5 end
6 ▷ Schedule exact-accurate jobs on  $S^*$ 
7 for each  $\tau_i^j \in \mathcal{G}$ , earliest  $\delta_i^j$  first do
8    $S_k = \{\alpha_k = \delta_i^j, \lambda_k = C_i\};$ 
9    $S^* = S^* \cup S_k; \quad G(S_k) = \{\tau_i^j\};$ 
10   $\theta_i^j = \delta_i^j; \quad \Gamma^H = \Gamma^H \setminus \tau_i^j;$ 
11 end
12 ▷ Schedule quality-based jobs on  $S^\neg$ 
13 generate each  $S_k$  for  $S^\neg$  using the free time spaces
    between the ETSs in  $S^*$ ;
14 for each  $S_k \in S^\neg$ , the earliest  $\alpha_k$  first do
15    $\Gamma_k = \{\tau_i^j \mid r_i^j < \alpha_k + \lambda_k \wedge d_i^j > \alpha_k, \forall \tau_i^j \in \Gamma^H\};$ 
16   for each  $\tau_i^j \in \Gamma_k$ , the earliest  $d_i^j$  first do
17     if  $\tau_i^j$  is feasible with  $G(S_k)$  on  $S_k$  then
18        $G(S_k) = G(S_k) \cup \tau_i^j;$ 
19        $\Gamma^H = \Gamma^H \setminus \tau_i^j;$ 
20     end
21   end
22 end
23 if  $\Gamma^H \neq \emptyset$ , return infeasible;
24 Optimise  $\theta_i^j$  of all  $\tau_i^j$  of each  $S_k \in S^\neg$  based on  $\Phi_i$ 
    using a linear search;
25 return  $\{S^*, S^\neg\};$ 

```

period, λ_k denotes the budget, and α_k is the start time. Once S_k is started, its budget is consumed with the passage of time. When the budget is exhausted, S_k is terminated along with all its unfinished tasks. Each time when S_k is released, the budget of S_k is replenished to λ_k . To describe the relationship between ETSs and I/O jobs, we let function $G(S_k)$ denote a set of jobs that are allocated to S_k .

B. Allocation and Scheduling of Jobs in ETSs

For a given set of I/O jobs in a hyper-period (denoted Γ^H), *ROTA-Sched* produces a feasible ETS-based list schedule with guaranteed timing predictability and improved accuracy. To achieve this, *ROTA-Sched* identifies the set of exact timing-accurate jobs that can yield the highest total quality (*i.e.*, with exact timing accuracy), and assigns a dedicated ETS to guard the execution of each *exact-accurate* job. The remaining jobs are then scheduled to improve their quality based on Φ_i , where several (*quality-based*) jobs can share one ETS. This protects jobs in one ETS from the timing defects in other ETSs and limits the propagation of timing defects within this ETS. Below, we first detail the identification of the timing-accurate jobs and then present the allocation and scheduling of jobs in the ETSs. The constructed ETS-based allocation and scheduling process of I/O jobs is presented in Alg. 1. Notations

 TABLE II: Notations introduced for constructing *ROTA-Sched*.

Notation	Description
Γ, Γ^H	The sets of I/O tasks and their jobs in a hyperperiod.
S^*, S^\neg	The sets of ETSs that manage the execution of exact-accurate and quality-based jobs.
τ_i	A periodic I/O task with an index of i .
C_i, T_i, D_i	The worst-case execution time, period, and deadline τ_i .
Φ_i, δ_i	The timing-accurate model and the exact-accurate start offset of τ_i .
$V(\Phi_i, t)$	The quality given Φ_i and a start offset t of τ_i .
$V_x^{max/min}$	The maximum/minimum quality of τ_i .
τ_i^j	The j^{th} job of τ_i in a hyperperiod.
r_i^j, d_i^j, δ_i^j	The release time, deadline, and the exact-accurate (best-case) start offset of τ_i^j .
ζ_i^j	Total quality from jobs affected by τ_i^j if it starts at δ_i^j .
θ_i^j	The actual start offset of τ_i^j decided by <i>ROTA-Sched</i> .
S_k	An ETS with an index k .
α_k, T_k, λ_k	The start time, releasing period, and capacity of S_k .
$G(S_k)$	The set of I/O jobs being assigned to S_k .
$\ \cdot\ $	The size of a given set or list.

S^* and S^\neg denote the ETSs that manage the execution of the exact-accurate and quality-based jobs, respectively.

Exact-accurate Jobs. To identify the exact-accurate jobs, a conflict graph \mathcal{G} is formulated assuming each job $\tau_i^j \in \Gamma^H$ is executed at the ideal offset δ_i^j . Then, for two jobs with an execution conflict, an edge is added to indicate they cannot start at their δ_i^j simultaneously. Let $E(\tau_i^j)$ denote the jobs connected to τ_i^j , the total quality of jobs that τ_i^j can affect if it starts at δ_i^j (represented by ζ_i^j) is computed by Equation 1.

$$\zeta_i^j = \sum_{\tau_x^l \in E(\tau_i^j)} V_x^{max} \quad (1)$$

With \mathcal{G} and $\zeta_i^j, \forall \tau_i^j \in \Gamma^H$ obtained, the algorithm starts by decomposing \mathcal{G} iteratively to identify the exact-accurate jobs based on ζ_i^j (lines 2-5). In each iteration, the τ_i^j with the maximum ζ_i^j is removed from \mathcal{G} , indicating it cannot be executed with exact timing accuracy, with the condition that τ_i^j can be fitted between the exact-accurate jobs (if possible). Otherwise, no feasible solution would be found during the allocation phase for the quality-based jobs. This process repeats until jobs left in \mathcal{G} are not connected with each other, *i.e.*, $\|E\| = 0$, which are identified as exact-accurate (*i.e.*, $\theta_i^j = \delta_i^j$). This in general increases the number of exact timing-accurate jobs. For each exact-accurate job τ_i^j , a dedicated ETS S_k is assigned to manage its execution with a start time $\alpha_k = \delta_i^j$ and an initial budget $\lambda_k = C_k$ (lines 7-11).

Quality-based Jobs. With S^* constructed, a set of ETSs for the quality-based jobs (*i.e.*, S^\neg) are generated using the free time space between the ETSs in S^* . The α_k and λ_k of each $S_k \in S^\neg$ are initialised based on the start time and length of the corresponding space (line 13). For each $S_k \in S^\neg$, the algorithm takes the unallocated jobs that are active during S_k (*i.e.*, Γ_k in line 15) and always tries to allocate the job with the earliest d_i^j to S_k (lines 16-21). A simple feasibility test is used to decide the acceptance or rejection of this allocation based on the remaining capacity of S_k , the allocated jobs $G(S_k)$, and d_i^j (line 17). If feasible,

τ_i^j is added to S_k with the earliest possible start offset (lines 18-19). This in general increases the success ratio of the allocation. With the mapping of jobs decided, for each job in S^\neg with the latest θ_i^j first, the algorithm postpones θ_i^j if a higher quality can be achieved based on Φ_i to further improve the operation quality of the system (where possible, without affecting other jobs using a linear search, line 24). The algorithm finishes and returns both the S^* and S^\neg with the allocation and scheduling of the I/O jobs embedded. Finally, the I/O jobs are registered to the associated ETS on *ROTA-I/O* using the instruction `p.l.d, \tau_i^j, S_k` introduced in Tab. I, in which $\tau_i^j \in G(S_k), \forall S_k \in S^* \cup S^\neg$.

Verification. The proposed *ROTA-Sched* is conducted on each I/O job in a hyper-period and returns a list schedule of the jobs, in which the schedule verifies whether a job can meet its deadline along with the scheduling process. Thus, similar to the job-level schedule in [32], [7], the scheduling algorithm also serves as the timing verification method of the system, in which the system is schedulable if a feasible solution can be obtained by Alg. 1, assuming there exist no timing defects.

Discussion. The time complexity of Alg. 1 is $\mathcal{O}(n^2)$, as at most $(\|\Gamma^H\| \times \|\Gamma^H\|)$ iterations are required to deconstruct \mathcal{G} (i.e., generation of S^*) and to allocate as well as schedule jobs in S^\neg . The algorithm returns a feasible ETS-based I/O scheduling solution that improves timing accuracy. If an unexpected timing defect occurs, its impact on I/O jobs is effectively restricted to one ETS, preventing the cascading disruptions on other ETSs in the system. However, jobs within the ETS could miss their deadlines or be terminated (if the ETS capacity is exhausted), due to the timing defect. Below, we present the configuration of ETS parameters that further enhance the robustness by mitigating the impact of timing defects on the produced schedule.

C. Configuration of ETS Parameters

Initial Configuration. Based on the allocation and schedule of I/O jobs determined by Alg. 1, the second step of *ROTA-Sched* produces the scheduling parameters of the ETSs, i.e., the start time α_k , the capacity λ_k , and the period T_k for each $S_k \in S^* \cup S^\neg$. The α_k is given by the earliest start offset of jobs in $G(S_k)$, i.e., $\alpha_k = \min\{\theta_i^j \mid \forall \tau_i^j \in G(S_k)\}$. An initial capacity of S_k can be obtained by Equation 2, which is calculated based on (i) α_k and (ii) the latest finish time of jobs in $G(S_k)$. As the ETSs are generated for a complete hyper-period, all ETSs in the system have the same period of $T_k = T^H$. In addition, as requested by the scheduler in *ROTA-I/O*, an earlier ETS (or job) is assigned with a higher priority.

$$\lambda_k = \max\{\theta_i^j + C_i \mid \forall \tau_i^j \in G(S_k)\} - \alpha_k \quad (2)$$

Additional Capacity of S_k . With the above parameters, the ETSs can be scheduled using a list scheduler (as described in Sec. III-B), in which S_k is always dispatched at α_k and finishes at $\alpha_k + \lambda_k$ in each hyperperiod. This provides a necessary time budget for the execution of the jobs in S_k , and eliminates the propagation of timing defects that occur in S_k to the following ETSs, as the execution of S_k cannot exceed λ_k regardless of

the impact from timing defects. However, for jobs in S_k , this capacity is insufficient to cope with unexpected timing defects within S_k , leading to unfinished job executions.

To mitigate the impact of timing defects within an ETS, an additional budget is provided to cope with the execution delay, allowing jobs in the ETS an extra chance to finish executions within their deadlines. However, this could result in a delay to the following ETSs (and the I/O jobs). Thus, to enable this additional budget while not jeopardising the real-time guarantee of the system, the following two bounds are computed first, for each $S_k \in S^* \cup S^\neg$:

- the highest delay that S_k can incur, denoted as Υ_k ; and
- the largest slack between S_k and the next ETS (say S_{k+1}), denoted as Ψ_k .

The first bound implies that a certain amount of additional capacity can be provided to the previous ETS (if required), without causing immediate deadline misses in S_k (see Lemma 1). The second provides a limitation on such capacity that prevents potential deadline misses in the following ETS (i.e., S_{k+1}) due to the transitive delay effect from S_k .

Lemma 1. For a given $S_k \in S^* \cup S^\neg$, the highest delay that S_k can incur is $\Upsilon_k = \min\{d_i^j - \theta_i^j - C_i \mid \forall \tau_i^j \in G(S_k)\}$.

Proof. Given a list schedule of I/O jobs in S_k (see Alg. 1, where each job is executed based on an explicit start offset), the worst-case delay effect occurs if all jobs are tightly executed, i.e., without any timing gap between the execution of two jobs. In this case, a delay of Υ_k on α_k can directly impose the same amount of latency on θ_i^j of each job in S_k , leading to deadline misses for jobs with $\theta_i^j + C_i + \Upsilon_k > d_i^j$. Therefore, to provide timing guarantee, $\Upsilon_k \leq \min\{d_i^j - \theta_i^j - C_i\}, \forall \tau_i^j \in G(S_k)$ must hold, hence, the lemma follows. \square

Lemma 2. For S_k and S_{k+1} , the largest slack between S_k and S_{k+1} is $\Psi_k = (\alpha_{k+1} + \min\{\Upsilon_{k+1}, \Psi_{k+1}\}) - \alpha_k - \lambda_k$. For the last S_k , $\Psi_k = T^H - \alpha_k - \lambda_k$.

Proof. First, given two consecutive ETSs S_k and S_{k+1} , the largest lack between them appears when S_k has the earliest finish (i.e., $\alpha_k + \lambda_k$), whereas S_{k+1} has the latest start. Then, for S_{k+1} , its latest start offset is bounded by both Υ_{k+1} and Ψ_{k+1} , because (i) the bound of Υ_{k+1} prevents deadline misses in S_{k+1} (proved in Lemma 1), and (ii) Ψ_{k+1} imposes a bound on the transitive delay of the following ETSs (if they exist) that avoids further deadline misses. \square

Based on Lemmas 1 and 2, Theorem 1 describes the additional capacity of S_k (denoted as ω_k) without affecting the timing of I/O jobs in the system.

Theorem 1. For a given S_k , it can execute using an additional capacity of $\omega_k = \min\{\Upsilon_{k+1}, \Psi_{k+1}\}$ without jeopardising the timing guarantee of the system.

Proof. Following Lemmas 1 and 2, this theorem can be proved using straightforward counterexamples. If $\omega_k = \Psi_{k+1} > \Upsilon_{k+1}$, the delay imposed on S_{k+1} from S_k would cause direct deadline misses of I/O jobs in S_{k+1} . This is proved

in Lemma 1. Otherwise, *i.e.*, $\omega_k = \Upsilon_{k+1} > \Psi_{k+1}$, the delay incurred by S_{k+1} can transitively affect the execution of the following ETSS, leading to further deadline misses. This is proved in Lemma 2. Therefore, the theorem holds. \square

As with Ψ_k , the computation of ω_k starts from the last $S_k \in S^* \cup S^-$ with $\omega_k = \min\{\Upsilon_{k+1}, (T^H - \alpha_k - \lambda_k)\}$, and calculates ω_k for each S_k backwards to provide the maximum additional capacity possible when being required. With the support of this additional capacity, jobs in S_k can execute until the time instant $\alpha_{k+1} + \omega_k$ with an additional budget up to Ψ_k , *i.e.*, the slack between the finish of S_k and the latest start of S_{k+1} . In addition, by taking Υ_{k+1} and Ψ_{k+1} into account when computing ω_k , we prevent potential deadline misses due to the transitive delay effect on the following ETSS, *i.e.*, the start of S_{k+1} is delayed with a bound of ω_k .

With ω_k obtained, the final capacity of S_k is determined as $\lambda_k = \max\{\theta_i^j + C_i \mid \forall \tau_i^j \in G(S_k)\} - \alpha_k + \omega_k$ based on Equation 2. This provides an extra execution budget for S_k to cope with unforeseen timing defects, while not endangering the timing requirements of I/O jobs. Based on the ISA constructed in Sec. II-B, the computed α_k , λ , and T_k of $S_k \in S^* \cup S^-$ can be configured in *ROTA-I/O* using instructions `c.enr`, α_k , S_k and `c.set`, λ_k , S_k , respectively (see Tab. I).

To this end, we constructed *ROTA-Sched* that schedules the I/O jobs on ETSS provided by the *ROTA-I/O*. The proposed *ROTA-Sched* provides the promised timing-accurate I/O control without timing defects. More importantly, using ETSS with the additional capacity, *ROTA-Sched* enhances robustness against unforeseen timing defects, as described in Theorem 2.

Theorem 2. *ROTA-Sched can tolerate an interference of $\omega = \min\{\omega_k \mid \forall S_k \in S^* \cup S^-\}$.*

Proof. For a given $S_k \in S^* \cup S^-$, it can cope with an additional interference of at most ω_k without causing a deadline miss in S_{k+1} (if it exists). This is proved in Theorem 1. Hence, the system can at least cope with a minimum interference of ω due to timing defects, while not affecting the timing of I/O jobs of other ETSS with $\omega \leq \min\{\omega_k \mid \forall S_k \in S^* \cup S^-\}$. Therefore, the theorem follows. \square

Following directly from this theorem, *ROTA-Sched* can tolerate an interference of ω while guaranteeing the timing of each I/O job (including those in the ETS with timing defects) if $\omega < \min\{\min\{\omega_k, \Upsilon_k\} \mid \forall S_k \in S^* \cup S^-\}$. Under this case, the interference caused by timing defects in S_k is not higher than the maximum delay that S_k can incur (*i.e.*, Υ_k). Hence, jobs in S_k can meet their deadlines, as proved in Lemma 1.

Finally, it is worth noting that an early ETS that consumes the extra budget (incurs timing defects) can result in less additional budget for later ones, *i.e.*, dynamic use of the additional capacity. However, this will not jeopardise the temporal isolation provided by the ETSS, which is effectively bounded by Ω_k for S_k so that the predictability of jobs in later ETSS is not affected. That is, the extended execution of an ETS will not cause any additional deadline misses in later ETSS. For instance, if S_k executes until $\alpha_{k+1} + \omega_k$, S_{k+1}

will have a reduced additional capacity as it must be finished at $\alpha_{k+1} + \lambda_{k+1}$ regardless of the delay. By contrast, if S_k finishes execution before α_{k+1} , S_{k+1} can still start at α_{k+1} with improved timing accuracy. This increases the success ratio of the system, where a job can execute and deliver using the additional budget when timing defects occur. This is further justified in Sec. V-C by experimental results.

V. EVALUATION

Experimental platform. We built the *ROTA-I/O* on a Xilinx VC709 evaluation board. The I/O controller was implemented using Chisel (v.3.4) and connected to a 5×5 mesh type NoC (Fig. 1 (a)). As well as the *ROTA-I/O*, the NoC also contained 8/16 open-source RISC-V processors [33], shared L2 cache (512 KB), external memory (4 GB), and I/O devices. We instantiated the processors with a 5-staged pipeline and single-width dispatch. All the hardware elements were synthesised, placed, and routed using Xilinx Vivado (v.2022.2). The software executing on the processors (OS, drivers, and applications) was compiled using a RISC-V GNU tool-chain (v.2022.11). We selected FreeRTOS (v.10.4) as the OS kernel, with the modifications that were introduced in Sec. II-D. To enable comparisons, we introduced 3 Baseline Systems (**BSs**) on similar hardware, replacing *ROTA-I/O* with different I/O controllers: BS|RTOS [34] is a legacy BS with the standard I/O controller, leaving I/O scheduling and management to the RTOS at software level; BS|GPIOCP [8] and BS|RTIOC [7] were built upon the SOTA real-time I/O controllers with different methodologies (see Sec. VI). All systems ran at 100 MHz due to the use of an FPGA as a prototyping platform.

A. Hardware Overhead

Experimental setup. We configured *ROTA-I/O* to support 8 ETSS and compared its overhead with a standard Ethernet controller and the real-time controllers used in the BS|RTOS, BS|GPIOCP and BS|RTIOC, respectively. The Ethernet controller was chosen from the Xilinx IP library with default settings, and the GPIOCP and RT-I/O were instantiated to ensure the same capacity with *ROTA-I/O*. In addition, to examine the overhead from a system perspective, we compared *ROTA-I/O* against two general-purpose RISC-V processors (Rocket [33] and Boom [35]). Rocket was configured using the settings described in the experimental platform. Boom had all the features of the Rocket processor, with the extra support of 3-width instruction-level parallelism. All components were compared using LUTs, registers, and BRAMs. All components were synthesised and implemented by Xilinx Vivado (v.2022.2) and compared using Look-Up-Tables (LUTs), registers, and BRAMs. Since these metrics were evaluated using various units, we the results using the Ethernet controller: 4,393 LUTs, 5,113 registers, 2 DSPs and 16KB BRAMs.

Obs 1. *ROTA-I/O* used less hardware than other controllers. From the SoC's perspective, the overhead was trivial.

This observation is given in Fig. 6(a), the implementation of *ROTA-I/O* consumed similar hardware compared to the standard Ethernet controller: 108.2% LUTs, 83.9% registers,

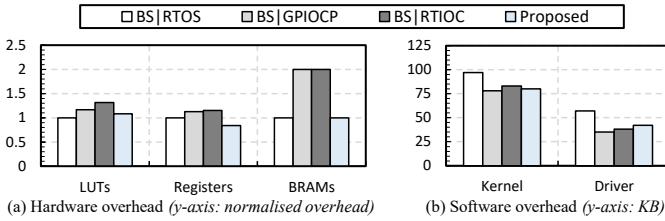


Fig. 6: Analysis of hardware and software overheads.

TABLE III: System schedulability under varied U .

$U =$	0.2	0.3	0.4	0.5	0.6	0.7	0.8
$P_r = 0, P_e = 0$							
BS GPIOCP	0.69	0.42	0.23	0.09	0.02	0.01	0.00
BS GA	0.99	0.95	0.84	0.69	0.53	0.38	0.20
BS RT-IOC	0.87	0.73	0.59	0.41	0.28	0.19	0.10
Proposed	0.86	0.70	0.55	0.38	0.21	0.11	0.05
$P_r = 0.3, P_e = 0.5$							
BS GPIOCP	0.59	0.3	0.1	0.03	0.00	0.00	0.00
BS GA	0.74	0.45	0.22	0.08	0.01	0.00	0.00
BS RT-IOC	0.72	0.45	0.24	0.09	0.02	0.00	0.00
Proposed	0.77	0.53	0.33	0.17	0.06	0.02	0.00

100.0% BRAMs. When compared to the other SOTA real-time controllers, *ROTA-I/O* demonstrated lower overhead across all metrics: GPICOP (92.6% LUTs, 74.4% registers, 50% BRAMs) and RT-IOC (82.3% LUTs, 72.9% registers, 50% BS-RAMs). The improvement is attributed to the resource-efficient micro-architecture introduced in Sec. III. From the SoC’s view, *ROTA-I/O*’s overhead is negligible: when compared with the general-purpose Rocket and Boom cores, *ROTA-I/O* only required 20% and 3% overhead, respectively.

B. Software Overhead

Deploying *ROTA-I/O* requires kernel changes and a new driver (Sec. II-D), hence we examined the software overhead. **Experimental setup.** We examined the software overhead via run-time memory footprint, with consideration of the OS kernel and the I/O drivers (unit: KB). The vanilla kernel used in the examined systems was fully featured with the software I/O manager and essential I/O drivers [34]. The memory size tool was RISC-V GNU tool-chain.

Obs 2. *ROTA-I/O* consumed less software than BS|RTOS. Its overhead was similar to BS|GPIOCP and BS|RTIOCP.

In Fig. 6(b), the OS kernel and drivers required by *ROTA-I/O* consumed 32 KB (20.8%) less memory than the software solution due to its hardware-implemented I/O management. Compared to other solutions, the memory usage of *ROTA-I/O* was similar: 107.9% (BS|GPIOCP) and 98.7% (BS|RTIOCP).

C. I/O-level Timing Performance

This section evaluates the timing performance of the proposed I/O control method against the BSs and the Genetic Algorithm described in [7] (BS|GA) that optimises the timing performance of I/O tasks. As with [7], the timing accuracy was measured as the *percentage of exact-accurate jobs* and *operation quality* based on Φ_i normalised by the maximum quality achievable (i.e., $\sum_{\tau_i^j \in \Gamma^H} V_{max}$).

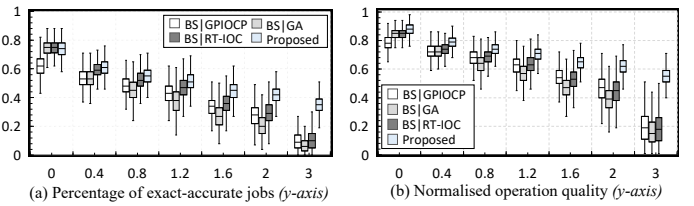


Fig. 7: Timing accuracy with $U = 0.6, P_r = 0.3$ (x -axis: P_e).

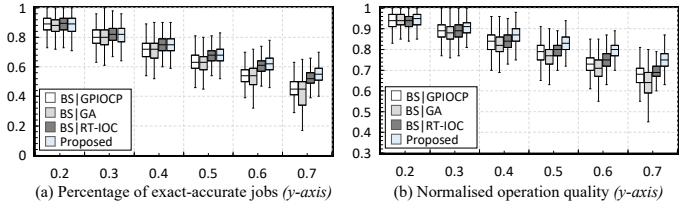


Fig. 8: Timing accuracy with $P_r = 0.3, P_e = 0.5$ (x -axis: U).

Experimental setup. The number of I/O tasks was set to $n = [4, 16]$, and the utilisation of tasks was generated by the UUniFast algorithm [36] with a total system utilisation given by $U = 0.05 \times n$. For each τ_i , T_i was generated randomly with a uniform distribution with a hyper-period of 1440ms, and $D_i = T_i$. The Φ_i of a task was randomly chosen from examples in Fig. 5, with V_{max} and V_{min} randomly decided from $[1, 100]$ and $[0, V_{max}]$, respectively. In addition, two control variables were defined for timing defects: P_r controlled the percentage of jobs that incurred timing defects and P_e gave the interference incurred by such a job, quantified as $C_i \times (1 + P_e)$. For each system configuration, 1,000 systems were randomly generated and evaluated.

Obs 3. *ROTA-I/O* showed higher schedulability and timing accuracy compared to SOTA methods with timing defects.

This observation is seen in Table III and Fig. 8, showing the resulting system schedulability and timing accuracy under varied U , respectively. Table III shows that the BS|GPIOCP was constantly outperformed by other methods due to its simple FIFO-based scheduling strategy [7]. In addition, we noticed that although *ROTA-I/O* shows a slightly lower schedulability than BS|RTIOCP without timing defects, it outperforms all SOTA methods when timing defects occur. This is because the BS|RTIOCP produces the schedule by a bin-packing approach, without considering the tightness of deadlines of I/O jobs, hence, is more fragile to timing defects. BS|GA tends to produce a tight schedule where jobs are executed close to each other. Thus, although BS|GA has the highest schedulability when $P_r = P_e = 0$, it showed the most pronounced fall with timing defects. By contrast, the ETS-based schedule (i.e., *ROTA-Sched*) that explicitly executes the job with the earliest d_i^j first (line 16 in Alg. 1), hence, is less likely to be affected by timing defects compared to SOTA methods.

In addition, as shown in Fig. 8, *ROTA-I/O* demonstrated both a higher percentage of exact-accurate jobs and the strongest overall quality in the general case, especially when the system

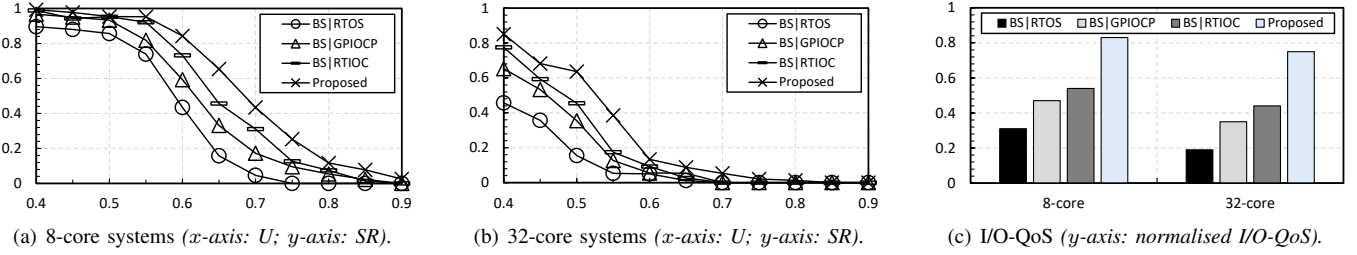


Fig. 9: Case study, evaluating system-level real-time performance (in (a) and (b)) and I/O quality (in (c)).

TABLE IV: Acceptance ratio with $U = 0.6$ and $P_r = 0.3$.

$P_e =$	0	0.4	0.8	1.2	1.6	2.0	3.0
BS GPIOCP	1.00	0.99	0.97	0.94	0.88	0.8	0.43
BS GA	1.00	0.99	0.95	0.91	0.82	0.72	0.38
BS RT-IOCP	1.00	0.98	0.96	0.92	0.84	0.75	0.40
Proposed	1.00	0.99	0.98	0.96	0.93	0.92	0.87

was heavy-loaded ($U \geq 0.6$). This is because, with the ETSS applied, *ROTA-I/O* effectively mitigates the impact of timing defects on the start offset of the I/O jobs, leading to higher timing accuracy compared to the SOTA methods. By contrast, the timing accuracy of the SOTA methods was significantly undermined by timing defects. For instance, BS|GA (the method with the highest quality in [7]) was outperformed by both BS|RTIOCP and BS|GPIOCP as shown in Fig. 8 in the general case. This observation revealed the impact of timing defects on existing timing-accurate I/O schedules, and justified the necessity for developing robust I/O control methods.

Obs 4. *ROTA-I/O* improves robustness compared to SOTA methods when impact of timing defects becomes significant.

This observation is seen in both Table IV and Fig. 7, which report the acceptance ratio (the percentage of jobs that meet their deadlines) and the timing accuracy of systems that are deemed schedulable by the competing methods, with an increasing impact (*i.e.*, P_e) of timing defects. From the results, *ROTA-I/O* showed both a higher acceptance ratio and timing accuracy compared to SOTA methods. For instance, *ROTA-I/O* outperformed BS|RTIOCP by 22.61% and 42.32% on average (2.18x and 3.06x when $P_e = 3$), in terms of acceptance ratio and operation quality, respectively. One notable reason is that, with the additional budget assigned for the ETSSs, *ROTA-I/O* allows more jobs to finish while providing the necessary temporal isolation for jobs in the following ETSSs. This justified the dynamic use of the additional budget (see Sec. IV-C). By contrast, the SOTA methods do not take unexpected interference from timing defects into account. Thus, these methods are highly sensitive to timing defects, which significantly affect their pre-planned schedule and resulting timing performance, especially when $P_e \geq 1.2$ as shown in Fig. 7.

D. System-level Real-time Performance

We evaluated the system-level real-time performance of the systems using an automotive case study. Specifically, we configured all systems with either 8 or 32 cores and executed

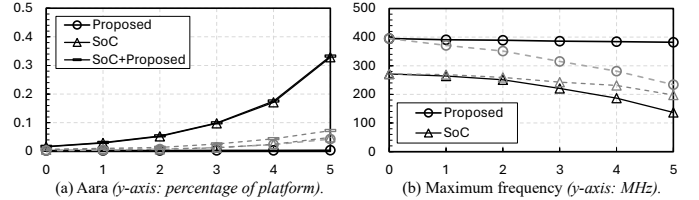


Fig. 10: Scalability (x -axis: η^{core} for black lines, η^{io} for grey lines).

two distinct sets of tasks: (i) 10 automotive safety tasks selected from the Renesas automotive use case database, such as CRC and RSA32; and (ii) 10 function tasks from the EEMBC benchmark, including FFT and speed calculation. We slightly modified these tasks to generate raw data externally, which was then transmitted to the system under test via an Ethernet connection (1 Gbps). The results were subsequently transmitted back using two FlexRay channels (10 Mbps). The value of Φ_i for each I/O task was randomly chosen from the examples provided in Fig. 5, with V_{max} and V_{min} set within the ranges of $[1, 100]$ and $[0, V_{max}]$, respectively. Each task was associated with a predefined period and an implicit deadline. Additionally, we introduced synthetic workloads to potentially adjust the overall system utilisation. These workloads, akin to the function tasks, were derived from the EEMBC benchmark. However, since the execution time of a task can be influenced by various factors, the addition of synthetic workloads provided only a *target utilisation* (U) for the system.

Experimental setup. We executed the systems 200 times under varying target utilisation $[50\%, 100\%]$, at intervals of 5%. Each experimental trial lasted 200 seconds, with $[10, 20]$ hardware faults randomly injected to the I/O controllers, delaying the I/Os' execution. For a fair comparison, we ensured that both the input data and the injected faults were identical across all tested systems. We evaluated the systems using Success Ratio (SR) and Quality of I/O Services (QoS-I/O). The SR recorded the percentage of trials that were executed successfully (*i.e.*, without deadline miss of any safety and function task), under a specified target utilisation. The QoS-I/O reports the average quality among all I/O tasks.

Obs. 5. Deploying *ROTA-I/O* increased overall real-time performance than baseline systems with improved I/O quality.

As shown in Fig. 9(a), (b), and (c), when the examined systems were configured using the same settings, our proposed

system consistently outperformed the BSs in terms of SR and I/O-QoS. The reasons for these improvements are two-fold: (i) the approach of hardware/algorithm co-design enhances the efficiency of I/O management (see Sec.III); (ii) the micro-architecture of *ROTA-I/O* isolates ETSS and prevents the propagation of timing defects – aligned to Obs. 3.

Obs. 6. With the increased complexity of the SoCs (*i.e.*, the core numbers), all systems exhibited a decline in SR.

This pattern is given by the comparison between Fig. 9(a) and Fig. 9(b). The reduction in SR stems from the additional on-chip interference and resource contention introduced by the growing number of processors and tasks - characteristic challenges in all multi/many-core systems, particularly when multiple tasks rely on the I/Os. Even so, in 32-core systems, *ROTA-I/O* consistently achieved the highest SRs, highlighting the effectiveness and applicability of *ROTA-I/O* in complicated many-core SoCs. To further mitigate such decline, it is necessary to consider the NoC contentions and interference to facilitate an end-to-end optimisation [37], [38], [39].

E. System-level Scalability

We acknowledge that the design scalability impacts its feasibility; hence, we performed a scalability analysis.

Experimental setup. The same method described in Sec.V-A was adopted to implement an SoC with a scaling number of processor cores and I/Os. In addition, we introduced scaling factors: η^{core} and η^{io} to control the number (2^n) of cores and I/Os in the system. As the number of cores increases, the associated I/O pool and L-SEs in a *ROTA-I/O* also expand to buffer and schedule more tasks. Conversely, an increase in the number of I/Os requires a corresponding increase in the number of *ROTA-I/O*s for additional device management.

First, we compared the scalability of area consumption between the legacy SoC (built upon standard ETH controllers) and the *ROTA-I/O*-based SoCs. The area consumption was normalised by the overall area of the platform. We then examined the maximum frequency of the *ROTA-I/O* and the SoC using varying η^{core} and η^{io} .

Obs. 7. *ROTA-I/O*'s area was almost unaffected by η^{core} and linearly scaled by η^{io} . Also, implementing *ROTA-I/O* in multi-/many-core SoCs did not impact the maximum performance.

As seen in Fig.10(a), when systems were scaled with η^{core} , the area consumption of *ROTA-I/O* was nearly constant. When scaled with η^{io} , the area of *ROTA-I/O* increased linearly, demonstrating the micro-architecture's hardware scalability. Furthermore, as illustrated in Fig. 10(b), in all examined cases, *ROTA-I/O*'s maximum frequency was always higher than the baseline SoCs. This indicates that *ROTA-I/O* did not become a critical path of the entire SoC design, and therefore did not limit the maximum performance of the system.

F. Summary

Based on the observations given in all experiments, *ROTA-I/O* showed robustness by coping with timing defects under both synthesised systems and a real-world case study, improving timing predictability and accuracy compared to SOTA

methods, without consuming significantly more resources than SOTA I/O controllers. In addition, the scalability of *ROTA-I/O* is demonstrated using real-world implementations, validating both the applicability and the effectiveness of the proposed solution on large-scale industrial applications.

VI. RELATED WORK

Research into real-time I/O design and verification methods in multi-/many-core systems has been investigated from the perspective of both the software and hardware.

Software-based I/O scheduling. Conventional safety-critical systems rely on an OS or a hypervisor to manage the I/Os [10]. Hence, software approaches aimed at satisfying I/O timing demands have typically modified the OS kernel [16], [17], [18] or the hypervisor [40], [41] to integrate I/O-aware task scheduling and mapping strategies [42], avoiding unnecessary contentions and trying to execute I/O operations as accurately as possible. A considerable amount of work has contributed to this research domain by developing different task mapping and scheduling methods, *e.g.*, reserving I/O bandwidths for software tasks according to their workload [15], [18], and applying a time utility function to schedule tasks at or close to their ideal offsets [43], [44]. However, as explained in Sec. I, software solutions are becoming difficult to apply to modern systems, due to the never-ending increase in hardware and architectural complexity, *e.g.*, many-core systems with mesh Network-on-Chips (NoCs). Such complexity introduces significant uncertainty to I/O transmissions, *e.g.*, communication delays and resource contentions through the system, making accurate control extremely tough to achieve from the software.

I/O-aware NoCs. At the NoC level, a commonly used method to improve real-time performance of I/O transactions is the duplication of communication channels. For instance, such duplicated channels were particularly deployed for different types of I/O devices, *e.g.*, cameras [45] and display devices [46]. Similarly, Jiang *et al.* [37], [47] introduced a bypass channel, termed “I/O ring”, facilitating more efficient data routing (one cycle level) between processors and all types of device. Distinct from merely duplicating communication channels, bandwidth reservation has also been studied to ensure service for particular tasks or transactions. This involves the interconnect assigning priorities to each hardware element and allocating bandwidth accordingly. For example, dedicated AXI controllers reserve bandwidth for high-priority devices [38], [48], [39], [49]. However, these methods solely focused on schedulability and average throughput of I/Os, without any attention paid to the key factors of timing accuracy and robustness.

Hardware-assisted I/O management. At the I/O level, dedicated assists have been developed and manufactured by different semiconductor vendors. For example, a programmable real-time unit has been developed by TI [23] and a time processor unit by NXP [22]. These controllers are physically connected to I/O devices and handle I/O operations directly at the hardware level. Since I/O management is deployed close to I/O devices, it effectively avoids I/O transmission uncertainty,

and hence, provides the potential for achieving I/O timing predictability and accuracy. Leveraging the hardware support, Jiang *et al.* [8] and Zhao *et al.* [7] presented different configuration methods that ordered the execution of I/O operations, specifying the start time of each I/O task (*i.e.* a series of I/O operations). Similarly, Guerra and Fohler [28] introduced a gravitational pendulum model that assigned higher “gravity” to I/O tasks with higher importance to improve their unity. These methods achieved a certain amount of timing predictability and accuracy for I/O control in their system models [28] and in work using their assumptions [8], [7]. However, as discussed in Sec. I, these approaches are fragile and would be entirely undermined by the interference of many timing defects.

VII. CONCLUSION

This paper presents a real-time I/O controller named *ROTA-I/O* using a hardware/software co-design approach. *ROTA-I/O* supports configurable ETSs and a two-level scheduler to establish the scheduling infrastructure that can prevent the propagation of timing defects between ETSs. Based on *ROTA-I/O*, an ETS-based I/O scheduling method named *ROTA-Sched* was constructed to mitigate the impact of timing defects, hence, improving both robustness and timing accuracy. Experimental results demonstrated that *ROTA-I/O* outperforms SOTA methods without consuming significantly more hardware resources. In future work, we plan to tape out the *ROTA-I/O* with safety-critical micro-controllers in a real chip to examine its energy efficiency under different application scenarios.

Lessons learned. Different from the conventional solutions that attempted to manage I/O timing defects solely through hardware design (e.g., physical isolation [50]) or software techniques (e.g., virtualisation [50]), this work shows that using a hardware/algorithm co-designed approach, timing accuracy and robustness can be effectively improved with light overhead. The constructed *ROTA-I/O* and *ROTA-Sched* provide key insights and effective means that foster a collaborative environment between the hardware and the schedule for real-time systems that neither discipline could achieve independently.

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REFERENCES

- [1] I. ISO, “26262: Road vehicles-functional safety,” 2018.
- [2] J. L. Hennessy, *Computer architecture: a quantitative approach*, 2011.
- [3] Z. Jiang, N. C. Audsley, and P. Dong, “Bluevisor: A scalable real-time hardware hypervisor for many-core embedded systems,” in *2018 IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS)*. IEEE, 2018, pp. 75–84.
- [4] N. Borgioli, M. Zini, D. Casini, G. Cicero, A. Biondi, and G. Buttazzo, “An I/O virtualization framework with i/o-related memory contention control for real-time systems,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 41, no. 11, pp. 4469–4480, 2022.
- [5] R. Chai, A. Tsourdos, A. Savvaris, S. Chai, Y. Xia, and C. P. Chen, “Six-DOF spacecraft optimal trajectory planning and real-time attitude control: a deep neural network-based approach,” *IEEE transactions on neural networks and learning systems*, vol. 31, no. 11, pp. 5005–5013, 2019.
- [6] J. Mossinger, “Software in automotive systems,” *IEEE software*, vol. 27, no. 2, p. 92, 2010.
- [7] S. Zhao, Z. Jiang, X. Dai, I. Bate, I. Habli, and W. Chang, “Timing-accurate general-purpose I/O for multi- and many-core systems: Scheduling and hardware support,” in *2020 57th ACM/IEEE Design Automation Conference (DAC)*. IEEE, 2020, pp. 1–6.
- [8] Z. Jiang and N. C. Audsley, “GPIOCP: Timing-accurate general purpose I/O controller for many-core real-time systems,” in *Design, Automation & Test in Europe Conference & Exhibition (DATE), 2017*. IEEE, 2017, pp. 806–811.
- [9] R. I. Davis and A. Burns, “Robust priority assignment for fixed priority real-time systems,” in *Proc. of RTSS*, 2007.
- [10] A. Burns and A. J. Wellings, *Real-time systems and programming languages: Ada 95, real-time Java, and real-time POSIX*, 2001.
- [11] R. I. Davis and A. Burns, “A survey of hard real-time scheduling for multiprocessor systems,” *ACM computing surveys (CSUR)*, vol. 43, no. 4, pp. 1–44, 2011.
- [12] L. Rierson, *Developing safety-critical software: a practical guide for aviation software and DO-178C compliance*. CRC Press, 2017.
- [13] Z. Ballard, C. Brown, A. M. Madni, and A. Ozcan, “Machine learning and computation-enabled intelligent sensor design,” *Nature Machine Intelligence*, vol. 3, no. 7, pp. 556–565, 2021.
- [14] A. Burns, R. I. Davis, S. Baruah, and I. Bate, “Robust mixed-criticality systems,” *IEEE Transactions on Computers*, vol. 67, no. 10, pp. 1478–1491, 2018.
- [15] L. Abdallah, M. Jan, J. Ermont, and C. Fraboul, “I/O contention aware mapping of multi-criticalities real-time applications over many-core architectures,” in *22nd IEEE Real-Time and embedded Technology and Applications symposium (RTAS 2016)*, 2016, pp. pp–25.
- [16] J.-E. Kim, M.-K. Yoon, R. Bradford, and L. Sha, “Integrated modular avionics (IMA) partition scheduling with conflict-free i/o for multicore avionics systems,” in *2014 IEEE 38th Annual Computer Software and Applications Conference*. IEEE, 2014, pp. 321–331.
- [17] E. Betti, S. Bak, R. Pellizzoni, M. Caccamo, and L. Sha, “Real-time I/O management system with cots peripherals,” *IEEE Transactions on Computers*, vol. 62, no. 1, pp. 45–58, 2011.
- [18] N. Kim, S. Tang, N. Otterness, J. H. Anderson, F. D. Smith, and D. E. Porter, “Supporting I/O and IPC via fine-grained os isolation for mixed-criticality real-time tasks,” in *Proceedings of the 26th international conference on real-time networks and systems*, 2018, pp. 191–201.
- [19] B. B. Brandenburg, “Multiprocessor real-time locking protocols,” in *Handbook of Real-Time Computing*. Springer, 2022, pp. 347–446.
- [20] S. Zhao, “A FIFO Spin-based Resource Control Framework for Symmetric Multiprocessing,” Ph.D. dissertation, The University of York, 2018, <http://etheses.whiterose.ac.uk/21014/>.
- [21] N. Audsley, A. Burns, M. Richardson, K. Tindell, and A. J. Wellings, “Applying new scheduling theory to static priority pre-emptive scheduling,” *Software engineering journal*, vol. 8, no. 5, pp. 284–292, 1993.
- [22] <https://www.nxp.com/eTPU>, TPU, accessed Nov. 17, 2022.
- [23] <http://www.ti.com/tool/pru-swpkg>, PRU, accessed Nov. 17, 2022.
- [24] J. Lee, S. Xi, S. Chen, L. T. Phan, C. Gill, I. Lee, C. Lu, and O. Sokolsky, “Realizing compositional scheduling through virtualization,” in *2012 IEEE 18th Real Time and Embedded Technology and Applications Symposium*. IEEE, 2012, pp. 13–22.

- [25] I. Shin and I. Lee, "Periodic resource model for compositional real-time guarantees," in *RTSS 2003. 24th IEEE Real-Time Systems Symposium, 2003*. IEEE, 2003, pp. 2–13.
- [26] —, "Compositional real-time scheduling framework," in *25th IEEE International Real-Time Systems Symposium*. IEEE, 2004, pp. 57–67.
- [27] R. I. Davis and A. Burns, "Robust priority assignment for messages on controller area network (CAN)," *Real-Time Systems*, vol. 41, pp. 152–180, 2009.
- [28] R. Guerra and G. Fohler, "A gravitational task model for target sensitive real-time applications," in *2008 Euromicro Conference on Real-Time Systems*. IEEE, 2008, pp. 309–317.
- [29] R. Guerra and G. Fohler, "A gravitational task model with arbitrary anchor points for target sensitive real-time applications," *Real-Time Systems*, vol. 43, pp. 93–115, 2009.
- [30] S. Liu, B. Yu, N. Guan, Z. Dong, and B. Akesson, "Real-time scheduling and analysis of an autonomous driving system," in *Proceedings of RTSS 2021 Industrial Challenge Problem*, pp. 1–47, 2021.
- [31] H. Mei, "Real-time stream processing in embedded systems," Ph.D. dissertation, University of York, 2017.
- [32] P. Chen, W. Liu, X. Jiang, Q. He, and N. Guan, "Timing-anomaly free dynamic scheduling of conditional DAG tasks on multi-core systems," *ACM Transactions on Embedded Computing Systems (TECS)*, vol. 18, no. 5s, pp. 1–19, 2019.
- [33] K. Asanovic, R. Avizienis, J. Bachrach, S. Beamer, D. Biancolin, C. Celio, H. Cook, D. Dabbelt, J. Hauser, A. Izraelevitz *et al.*, "The rocket chip generator," *EECS Department, University of California, Berkeley, Tech. Rep. UCB/EECS-2016-17*, vol. 4, pp. 6–2, 2016.
- [34] <https://www.freertos.org>, FreeRTOS, accessed July. 15, 2023.
- [35] J. Zhao, B. Korpan, A. Gonzalez, and K. Asanovic, "Sonicboom: The 3rd generation berkeley out-of-order machine," in *Fourth Workshop on Computer Architecture Research with RISC-V*, vol. 5, 2020, pp. 1–7.
- [36] E. Bini and G. C. Buttazzo, "Measuring the performance of schedulability tests," *Real-time systems*, vol. 30, no. 1, pp. 129–154, 2005.
- [37] Z. Jiang, X. Dai, R. Wei, I. Gray, Z. Gu, Q. Zhao, and S. Zhao, "NPRC-I/O: A NoC-based real-time I/O system with reduced contention and enhanced predictability," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 2023.
- [38] F. Restuccia, M. Pagani, A. Biondi, M. Marinoni, and G. Buttazzo, "Is your bus arbiter really fair? restoring fairness in axi interconnects for fpga socs," *ACM Transactions on Embedded Computing Systems (TECS)*, vol. 18, no. 5s, pp. 1–22, 2019.
- [39] M. Pagani, E. Rossi, A. Biondi, M. Marinoni, G. Lipari, and G. Buttazzo, "A bandwidth reservation mechanism for AXI-based hardware accelerators on FPGAs," in *31st Euromicro Conference on Real-Time Systems (ECRTS 2019)*, 2019.
- [40] E. Missimer, K. Missimer, and R. West, "Mixed-criticality scheduling with I/O," in *2016 28th Euromicro Conference on Real-Time Systems (ECRTS)*. IEEE, 2016, pp. 120–130.
- [41] R. West, Y. Li, E. Missimer, and M. Danish, "A virtualized separation kernel for mixed-criticality systems," *ACM Transactions on Computer Systems (TOCS)*, vol. 34, no. 3, pp. 1–41, 2016.
- [42] D. Casini, A. Biondi, G. Cicero, and G. Buttazzo, "Latency analysis of I/O virtualization techniques in hypervisor-based real-time systems," in *2021 IEEE 27th Real-Time and Embedded Technology and Applications Symposium (RTAS)*. IEEE, 2021, pp. 306–319.
- [43] J. Wang and B. Ravindran, "Time-utility function-driven switched ethernet: Packet scheduling algorithm, implementation, and feasibility analysis," *IEEE Transactions on Parallel and Distributed Systems*, vol. 15, no. 2, pp. 119–133, 2004.
- [44] P. Li, B. Ravindran, and E. D. Jensen, "Adaptive time-critical resource management using time/utility functions: Past, present, and future," in *Proceedings of the 28th Annual International Computer Software and Applications Conference*, vol. 2. IEEE, 2004, pp. 12–13.
- [45] B. Parten, Y. Lee, B. Quach, L. Myers, W. Ray, and W. Maung, "Multi-channel peripheral interconnect supporting simultaneous video and bus protocols," 2017, US Patent.
- [46] P. R. Chandra, K. C. Kahn, E. Galil, E. Kugman, N. Zolotov, V. Yudovich, Y. Dishon, and E. Bagelman, "Multi-protocol tunneling over an I/O interconnect," 2014, US Patent.
- [47] Z. Jiang, X. Dai, S. Zhao, R. Wei, and I. Gray, "Many-core real-time network-on-chip I/O systems for reducing contention and enhancing predictability," in *Proceedings of Cyber-Physical Systems and Internet of Things Week 2023*, 2023, pp. 227–233.
- [48] F. Hebbache, M. Jan, F. Brandner, and L. Pautet, "Shedding the shackles of time-division multiplexing," in *2018 IEEE Real-Time Systems Symposium (RTSS)*. IEEE, 2018, pp. 456–468.
- [49] Z. Jiang, K. Yang, N. Fisher, I. Gray, N. C. Audsley, and Z. Dong, "Axi-ic^{RT}: Towards a real-time axi-interconnect for highly integrated socs," *IEEE Transactions on Computers*, vol. 72, no. 3, pp. 786–799, 2022.
- [50] C. Herber, A. Richter, H. Rauchfuss, and A. Herkersdorf, "Spatial and temporal isolation of virtual can controllers," *ACM SIGBED Review*, vol. 11, no. 2, pp. 19–26, 2014.