smaller cavity efficiency and a stronger influence of third order dispersion due to the internal grating compressor.

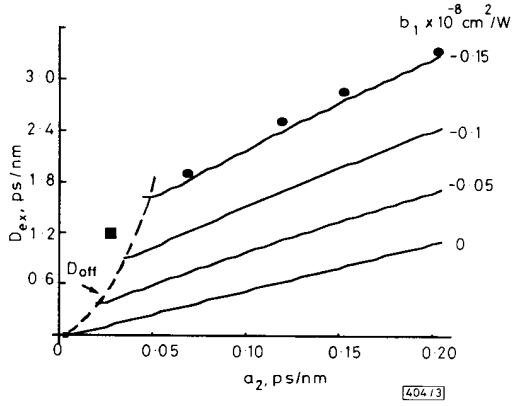

Fig. 3 *External compressor dispersion at optimum as function of intracavity group velocity dispersion*

● experiment
——— numerical simulations for different b_1 values
– – – – analytical calculation of minimum dispersion

Modelling: Laser-diode modelocking was analysed using the master equation approach developed by Haus [6]. Intracavity dispersion as well as instantaneous net-gain saturation and self-phase modulation effects were included as in the work of Martinez *et al.* [7]. Closed-form analytical solutions of pulse parameters could then be obtained. Numerical simulations were performed in parallel to test the stability of the solutions. The details of our analysis are given elsewhere [8].

Two well-known peculiarities of semiconductor laser media as compared to other systems are: large refractive index (phase) variations associated with gain/absorption variations, and strong gain/absorption saturation detected in short time scales [9]. Considering that quadratic variations of phase with energy ($-\Psi''$ terms in Reference 7) occur with a sign opposite to those of net gain (g'' term), we theoretically verified that modelocking could be only achieved for normal intracavity GVD. As a second result, we found that instantaneous net-gain saturation (b_1 term in Reference 7) was responsible for the dispersion offset measured at minimum intracavity GVD.

For strong chirp, the minimum intracavity GVD and dispersion offset were found to be correctly described by the following formulas:

$$a_{2m} = a_{20}\left\{1 - \frac{b_1}{2} \cdot \frac{k_1}{k_2[-a_{20}\Psi'']^{1/2}}\right\} \quad (1)$$

$$D_{off} = (-b_1)^{3/2}\left\{\frac{k_1^{1/2}a_1^{1/4}g'^2}{2\sqrt{(2)}k_2^{7/4}(-\Psi'')^{1/2}(-g_0)^{3/4}}\right\} \quad (2)$$

where $a_{20} = -2a_1\Psi''g_0/k_2$ is the minimum GVD in the absence of fast gain saturation, a_1 is the available bandwidth and k_1, k_2 are related to the g_0, g', g'' coefficients appearing in the series expansion of net gain with energy ($k_1 = g'^2 - 4g_0 \cdot g''$ and $k_2 = g'^2 - 6g_0 \cdot g''$). The theoretical evolution of D_{off} predicted by eqns. 1 and 2 is reported in Fig. 3 for $a_1 = 7 \times 10^{-4}\,ps^2$, $g_0 = -0{\cdot}6$, $g' = 0{\cdot}3\,pJ^{-1}$, $g'' = -0{\cdot}02\,pJ^{-2}$ and $-\Psi'' = -2{\cdot}5g''$ (dashed curve). Full curves are numerical calculations of the external compressor dispersion at optimum. As seen, there is an excellent agreement between calculations and experiments for $b_1 = -0{\cdot}15 \times 10^{-8}\,cm^2/W$, which is close to what can be deduced from previous experiments [9]. Note the absence of dispersion offset when only energetic (slow) variations of laser net gain and phase are considered ($b_1 = 0$). The weak dependence of the curve slope with b_1 is also remarkable; this can be reasonably approximated by $2(g'^2 - 3g_0 \cdot g'')/(g_0 \cdot g'')$.

Conclusion: Passive (hybrid) modelocking of laser diodes in an extended cavity with high tunable group velocity dispersion has been demonstrated. The evolution of pulse compressibility with intracavity dispersion has revealed the important role of instantaneous laser net gain saturation even for modelocked pulses in the picosecond time scale. The requirement of positive dispersion seems to be related to the self-phase modulation of the laser medium.

15th June 1993

A. Azouz, N. Stelmakh and J.-M. Lourtioz (*Institut d'Electronique Fondamentale URA 22 du CNRS, Université Paris XI, Bât. 220, 91405 Orsay Cedex, France*)

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DESIGN-FOR-TEST STRUCTURE TO FACILITATE TEST VECTOR APPLICATION WITH LOW PERFORMANCE LOSS IN NON-TEST MODE

A. H. Bratt, R. J. Harvey, A. P. Dorey and A. M. D. Richardson

Indexing term: Design for testability

A switching based circuit is described which allows application of voltage test vectors to internal nodes of a chip without the problem of backdriving. The new circuit has low impact on the performance of an analogue circuit in terms of loss of bandwidth and allows simple application of analogue test voltages into internal nodes. The circuit described facilitates implementation of the forthcoming IEEE 1149.4 DfT philosophy [1].

Introduction: A DfT philosophy must simultaneously satisfy several criteria of which three major elements are [2]:

(i) Control and observation of deeply embedded nodes must be possible to verify circuit functionality and detect fabrication defects by the application and observation of test vectors.

(ii) Performance loss must be minimal in normal (non-test) operating mode. In particular, loss of bandwidth must be avoided and area overhead must not be excessive.

(iii) Migration of the testing problem from device level to chip level should be possible and this process should be amenable to automation.

It is assumed that a design may be divided into a number of blocks which perform identifiable functions and may be tested in isolation. The process of testing then becomes one of application of test voltages between blocks and observation of the subsequent output of the block on the proceeding signal path. A major problem with this methodology is that blocks often have low output impedance which frustrates attempts at directly controlling voltage levels between them due to the low impedance of the node, a phenomenon known as backdriving.

It has been proposed that a pass transistor structure may be used to isolate an inter-block node from the output stage of the previous block [3], but the presence of switching transistors in the signal path during non-test mode may have serious performance repercussions in limiting the bandwidth. Fig. 1 shows a circuit designed to prevent backdriving based on that proposed in Reference 3 and traces (i) and (ii) of Fig. 3

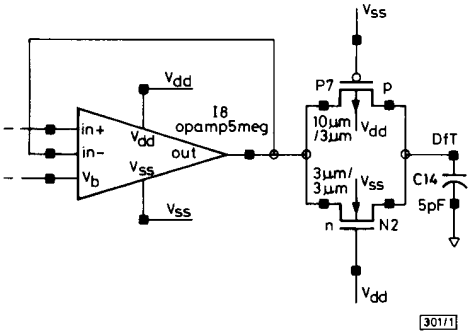

Fig. 1 *Complementary pass transistors used to prevent backdriving*

represent the bandwidth loss of an operational amplifier without and with, respectively, the complementary switch added as in Fig. 1. Clearly the performance impact is significant and the effect may easily be demonstrated to be much more severe for a circuit which as a sensitive output (sensitive in the sense of having low drive power, high loading or a low impedance path to ground).

A circuit is presented in this Letter which overcomes the backdriving problems associated with attempts to directly drive inter-block nodes and has much less impact on the bandwidth of the circuit in non-test mode.

DfT switching circuit operational amplifier: Fig. 2 shows a schematic diagram of an operational amplifier with two standard input stages of the type shown in Reference 4 and a common output stage. The digital input signal 'test' and its complement 'testbar' may be used to connect either of the input stages to the output stage. Note that the field effect transistors (FET) which perform the switching action (M1 and M2) are inserted in small-signal paths rather than large signal paths. The source and drain terminals of M1 and M2 are maintained at a common voltage of approximately $V_{dd} - 0{\cdot}8$ V so the need for a complementary switch as in Fig. 1, is obviated. Note also that M1 and M2 need only have an aspect ratio of 10/3 because they carry a typical current of only 8 μA with a 1 MHz sinusoid input signal of 1 V peak to peak.

If input stage B is selected (test = '0') then the operational amplifier performs its normal function with minimal loss of bandwidth. Trace (iii) of Fig. 3 represents the Bode plot of this amplifier in non-test mode. Clearly the bandwidth change

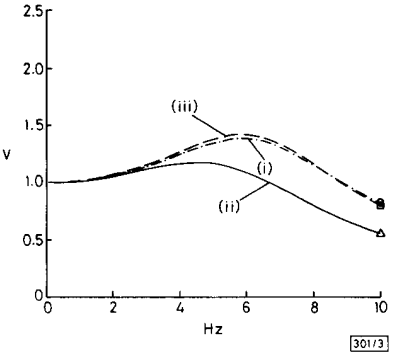

Fig. 3 *Bode plot of operational amplifier with no DfT structures added, proposed IEEE 1149.4 DfT structures added, and new DfT structures added*

(i) no added DfT structures
(ii) proposed IEEE 1149.4 DfT structures added
(iii) new DfT structures added

with respect to the unloaded case (trace (i)) is greatly reduced from that seen in trace (ii). Increasing the aspect ratio of the switching FETs M1 and M2 will further reduce the bandwidth degradation if necessary.

If input stage A is selected then voltages that are applied to terminal 'vector' will re-appear at the output of the amplifier subject to the usual limitations of an operational amplifier such as offset voltage, slew rate limitation etc. The FETs in stage A may be made very much smaller than those of input stage B because, in general, the performance of this input stage for testing purposes is not usually required to be as high as for stage B.

The problem of backdriving in the test mode is no longer present with this circuit configuration; the inter-block test vector voltage is produced by the output stage of the operational amplifier rather than in opposition to it.

Conclusion: A switching based circuit has been described which allows a DfT scheme to be implemented with little loss of bandwidth and a minimal area overhead. The problem of backdriving is effectively obviated because the output stage for both test and non-test modes is the same. A cell-by-cell testing strategy is possible with the proposed circuit under the limitation that it has been assumed that the majority of blocks

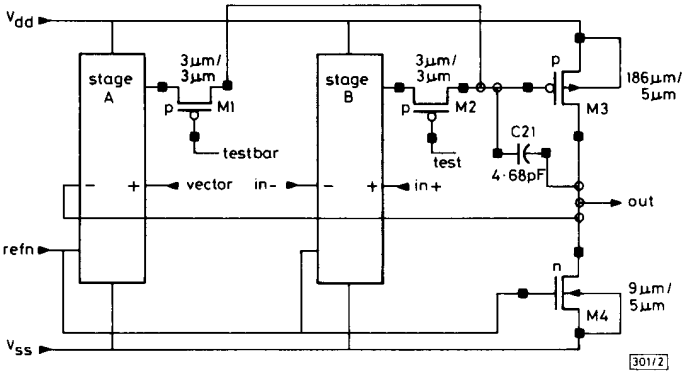

Fig. 2 *Proposed operational amplifier circuit with switchable input stages for application of voltage test vectors*

have an operational amplifier driving the output node. Injection of test vectors into interblock nodes is performed easily and with little loading of the test vector voltage.

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A. H. Bratt, R. J. Harvey, A. P. Dorey and A. M. D. Richardson (*Engineering School, SECAMS, Lancaster University LA1 4YR, United Kingdom*)

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ANALYSIS OF SKELETON JUNCTIONS IN 3 × 3 WINDOWS

E. R. Davies and D. Celano

Indexing terms: Image processing, Pattern recognition

The Letter studies the formation and analysis of skeletons in binary images. Particular emphasis is placed on the concept of crossing number which is found to be subtly different when testing a point *known* to be on a skeleton and testing *whether* a point is on a skeleton: these ideas are applied to the elimination of noise spurs from skeletons.

Introduction: The skeleton of a binary figure can be defined as a connected graph that runs along the medial lines of the limbs of the figure [1]. It is a useful concept in that its form reflects the general shape of a figure (including all its holes and limbs), and in particular its connectedness parallels that of the figure. Analysis of skeletons involves particularly location and classification of 'nodes' (including junctions and line ends) and measurement of limb lengths and orientations.

Although skeletons are important for the analysis of shapes in binary images, a number of intricacies arise in the formation and analysis of skeletons. This Letter considers skeleton junction analysis and studies the elimination of noise spurs from skeletons: the immediate motivation for this arose from our own work on structure in textures.

Crossing number and skeleton formation: Both the formation and the analysis of skeletons are aided by the concept of a crossing number χ, the basic idea of which is to count the number of changes from white to black and black to white on proceeding once around a given pixel [1, 2]. However, the concept is complicated in its implementation because the definition of connectedness on a binary lattice involves a fundamental difficulty. In particular, diagonally adjacent 1s have to be regard as joined, but diagonally adjacent 0s must not be; this '8-connectedness' definition overcomes the problem that the background 0s are simultaneously adjacent to each other and separated from each other by the foreground 1s in the configuration

0	1
1	0

Hence [1, 2], χ has to be redefined as the number of effective changes from white to black and black to white on going around a given pixel, and implemented in a 3 × 3 window as

$$\chi = U(A1 \neq A3) + U(A3 \neq A5) + U(A5 \neq A7) + U(A7 \neq A1) + 2[U(\neg A1 \,\&\, A2 \,\&\, \neg A3) + U(\neg A3 \,\&\, A4 \,\&\, \neg A5) + U(\neg A5 \,\&\, A6 \,\&\, \neg A7) + U(\neg A7 \,\&\, A8 \,\&\, \neg A1)] \quad (1)$$

where the 3 × 3 window notation is:

$A4$	$A3$	$A2$
$A5$	$A0$	$A1$
$A6$	$A7$	$A8$

the window values $A0$ to $A8$ are all Boolean 0s and 1s, '&' is the logical AND function, '¬' is the logical NOT function, and the 'unity' function $U(.)$ converts Boolean values 0 and 1 to numerical values 0 and 1, respectively.

Also of relevance for skeleton formation and analysis is the σ-function:

$$\sigma = U(A1) + U(A2) + U(A3) + U(A4) + U(A5) + U(A6) + U(A7) + U(A8) \quad (2)$$

A simple parallel thinning algorithm is now [2]: successively remove boundary North, South, East and West points until no further change occurs, but only at points for which $\chi = 2$ and $\sigma \neq 1$. The first of these two conditions prevents points from being removed when this would affect connectedness, and the second condition prevents limbs from being shortened. Although many more complex thinning algorithms exist [1, 3, 4], this simple one shows the role played by crossing number in skeleton formation.

Skeleton analysis potentially involves examination of local crossing number values, e.g. $\chi = 4$, $\chi = 6$ or 8, $\chi = 2$, $\chi = 0$ might indicate respectively a 'normal' skeleton point, a junction, a line end, and a point skeleton. We amend this view of the situation below.

Analysis of skeleton junctions: We have found that although crossing number is a useful concept for skeleton formation, it has restricted value when analysing skeletons. Consider the following instance:

1	1	0
0	1	1
1	0	0

This apparently corresponds to a T-junction, but its crossing number value of 4 indicates that it is a 'normal' skeleton point. In fact both interpretations are wrong, assuming this is known to be a point on a skeleton; thus the A3 value of 1 can only arise if there is a point North-East of it. Similarly the A1 value of 1 can only arise if there is a point East, NE or SE of it. In fact all window border points that are 1s must correspond to different lines joining the centre pixel; this clearly includes lone diagonal points (e.g. the A6 point in the above example). Thus the number of lines arriving at a given point must be σ, and we can consistently (see the Introduction) define the effective crossing number on a skeleton as being twice this, i.e. $\chi_{skel} = 2\sigma$. We amplify this statement by giving two examples of 5 × 5 windows for which the inner 3 × 3 windows have σ-values of 4 and 8, respectively:

1	0	0	1	0
0	1	1	0	0
0	0	1	1	1
0	1	0	0	0
1	0	0	0	0

1	0	1	0	1
0	1	1	1	0
1	1	1	1	1
0	1	1	1	0
1	0	1	0	1