A Design-For-Test Structure for Optimising Analogue and Mixed Signal IC Test

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Abstract

A new Design-for-Test (DfT) structure based on a configurable operational amplifier, referred to as a "swap amp" is presented that allows access to embedded analogue blocks. The structure has minimal impact on circuit performance and has been evaluated on a custom designed Phase Locked Loop (PLL) structure. A test chip containing faulty and fault free versions of this PLL structure, with and without DfT modifications, has been fabricated and an evaluation of this DfT scheme based on the swap-amp structure carried out. It is shown that for embedded analogue blocks, the DfT strategy can not only improve and simplify analogue & mixed signal IC test, but can also be used for diagnostics.

1. Introduction

Developments in processing technology and circuit design have drastically reduced the problems associated with manufacturing complex mixed-signal and analogue IC's. These problems have however not all been solved and as with digital VLSI in the 80's, testing is once again becoming the major obstacle to advances in integration complexity. Testability is mainly an issue of control and observation of deeply embedded internal nodes [1] which in the digital domain, has been addressed by numerous DfT and Built-in-self-test (BIST) techniques to ensure that a design can be adequately tested. In the analogue world, the introduction of control voltages within a design is not a trivial matter since the effects of capacitive and resistive loading due to the switch can seriously compromise the performance of a finely tuned analogue design. This paper reports on the implementation of a Design-for-Test (DfT) philosophy which allows injection of control voltages using an operational amplifier with a configurable internal architecture. Bandwidth performance loss is shown to be greatly reduced compared with more traditional approaches with an area overhead of approximately 5% for each modified operational amplifier. The DfT scheme is simple to implement and the problem of backdriving is totally eliminated. Application of the DfT scheme to a phase-locked-loop circuit is presented. The scheme is shown to greatly improve both detection and diagnostic capabilities associated with a number of hard and soft faults. The format of the paper will be as follows; Section 2 will identify related work, sections 3 and 4 will then discuss critical issues in the design of an analogue DfT architecture and identifies the optimal placement of switches. Section 5 will describe the design of the swap-amp and present an analysis of its performance. In section 6, a DfT scheme exploiting the "swap-amp" design is discussed and in section 7 the test chip fabricated to access the fault detection and diagnostic capabilities of the scheme is described. Section 8 will present results from the silicon and section 9 will conclude and discuss future work.

2. Background

The problems related to testing mixed signal and analogue IC's are numerous and include fault modelling and simulation, test generation, test time and complexity as well as the difficulties associated with obtaining access to embedded analogue blocks. The push towards high reliability and low ppm defect levels has generated interest in realistic layout dependent defect models [2-4] and novel test methodologies. These can improve the fault coverage over that achieved using standard functional production tests at minimal cost and implementation complexity [4-11].

Test access and analogue DfT has been discussed by a number of authors [12-16] but has been limited to ensuring that the correct internal nodes are routed to dedicated test pins and that the problem of test is considered early in the design process. A DfT methodology for active analogue filters was proposed in [12] and an extension to enable fault isolation and diagnostics carried out in [17]. A novel technique for switched capacitor implementations based on a programmable biquad filter has been developed [13]. This

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technique is probably better referred to as an analogue Built-in Self Test (BIST) methodology as the DfT circuitry provides a facility for on-line test of the biquad filters. Commercial implementation of analogue DfT strategies has not been widely published, however an interesting methodology based on extending a digital SCAN architecture to provide an Analogue BIST capability has been investigated [18].

3. Design Partitioning

Designers deliberately introduce hierarchy into designs and fragment each hierarchic level into a number of blocks to make designs more manageable. In order to simplify the testing of an analogue or mixed signal circuit, it is necessary to partition the circuit at either the schematic level of the design hierarchy or preferably at the layout

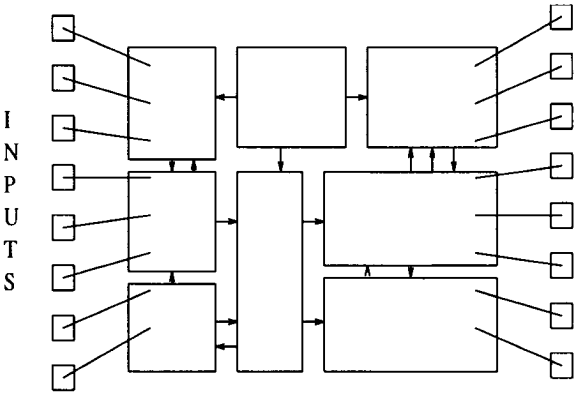

Fig. 1. Basic circuit partitioning or "fragmentation"

level. At the schematic level it is usually convenient to exploit the hierarchial partitioning introduced during the design process, but for optimal test generation, partitioning at the layout level to minimise interconnect between circuit partitions may well be desirable, especially if defect oriented test strategies are to be used [4]. One problematic issue relating to partitioning is that of feedback paths. This inherent feature of many analogue designs tends to resist attempts to treat a design on a block by block basis. In a complex design these paths must usually be broken to allow the testing procedure to begin.

4. DfT Strategies

4.1 Invasive Access Strategies

Fig. 2. shows a method which could be used to break connections between two analogue blocks and insert a control voltage. The switches in this diagram are controlled by a number of D-type flip-flops which are loaded serially. Both control and observation of internal analogue voltage levels is achieved by an appropriate configuration of the test bus. In the domain of analogue

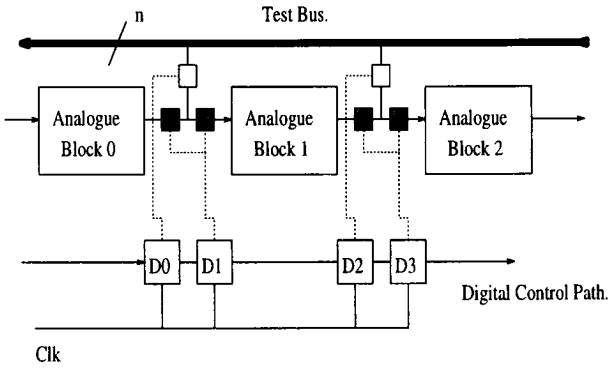

Fig. 2. DfT Strategy using switches between circuit blocks

circuit design it is not a trivial matter to break feedback loops by inserting switches in metalised track connections, shown shaded in Fig. 2. The series resistance of even a very wide (e.g. aspect ratio 100:1) CMOS transistor is several orders of magnitude greater than the resistance of the metal track. Capacitance of the switch is also usually many times higher than that of the metal track.

The effective resistance of a MOSFET operating in the linear region, with only a few mV of voltage difference between its source and drain may be expressed as;

$$R_{DS} = \frac{L}{K' W}(V_{GS} - V_T)^{-1} \qquad (1)$$

where R_{DS} is the drain to source resistance, W and L are the FET width and length respectively, K' is the transconductance parameter, V_{GS} is the gate-source voltage drop and V_T is the threshold voltage (including any body effect).

Increasing the width, W, of the MOSFET will reduce the series resistance. However, the parasitic capacitance is approximately proportional to the product of width and length. The increase in parasitic loading capacitance will determine a maximum aspect ratio for the switch in a given application. The area used must also be taken into account, this effectively also sets a limit to the maximum aspect ratio. It should also be noted that the RC product for the switch has an approximate value of $R_0 C_0 L^2$, where R_0 and C_0 are arbitrary constants. Assuming that the length L is minimal (and so fixed), no amount of scaling by altering the width of the switch will change the RC product.

Ideally, a circuit element introduced for testing purposes should have little impact on even a sensitive

node (i.e. low drive power with possibly heavy load) and should in all cases have the absolute minimal impact on performance. However, breaking connections in test mode in some manner is normally essential to achieve both satisfactory testability and minimal test cost.

4.2 Direct Drive Access Strategies

One possible solution to avoid the series resistance of the MOSFET switches is simply to leave them out. Fig. 3 shows a modified version of Fig. 2 were the switching in the signal paths has been removed. Backdriving into the previous output stage is a serious problem here if there is

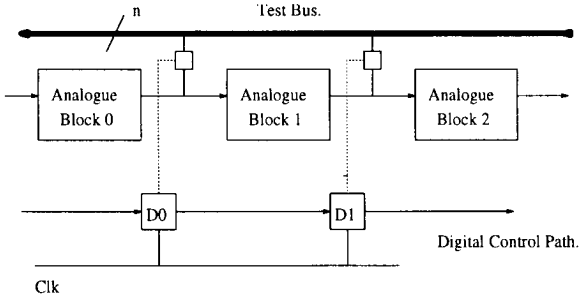

Fig. 3. Direct Drive into an Internal Circuit Node

an attempt to force a nodal voltage via the test bus. Large currents causing local heating and electrical stress as well as the inevitable degradation of the test signal can also be expected. It can be concluded that breaking electrical connections during test mode is problematic, but a brute force attack is certainly worse.

4.3 Switching in small signal paths

Integrating the switching function in small signal paths of a circuit will considerably reduce the effects of parasitic capacitance and resistance of the inserted switch. The small voltage swings seen (typically a few mV) mean that the current required to charge and discharge the parasitic capacitors is small and settling times are consequently short. Choosing a sensible place for switch insertion, as for M8 in Fig. 4 ensures that only a few uA's of current flows through the switch during even the largest output voltage swing, hence the effects of the switch resistance are small. This strategy forms the basis of the "swap-amp" DfT structure that will be described in the remainder of this paper.

5. Swap-amp design

Fig. 5. shows a schematic diagram of the swap-amp which forms the basic structure behind the DfT philosophy

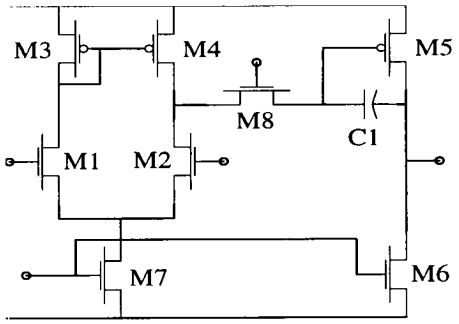

Fig. 4. The insertion of the switch M8 in the small signal path reduces the impact on circuit performance

presented. This amplifier has two input stages which are interchangeable using the external signal ***TEST*** and its complement $\overline{TEST}$. When ***TEST*** is low, switch ***S2*** conducts and the amplifier is configured into its "normal" mode. When ***TEST*** is high, ***S1*** conducts and the hardwired unity gain **"test"** input stage can then be used to propagate a voltage applied at input ***vector*** to the output. Two features of this scheme should be noted; First, the switching is done in small signal paths rather than large signal paths. This has the low-loading effects outlined previously. Second, the aspect ratios of the transistors in the test mode input stage can be made minimum sized since the common mode range and bandwidth requirements of the "test" input stage is generally much less than that of the "normal" input stage. As a minor benefit, the need for complimentary pass transistors is eliminated since the DC voltage level either side of the switches ***S1*** and ***S2*** is close to the positive power rail at all times.

It should also be noted that no mention has been made of the feedback configuration of the swap-amp. Provided the **"test"** input stage has sufficient performance to ensure

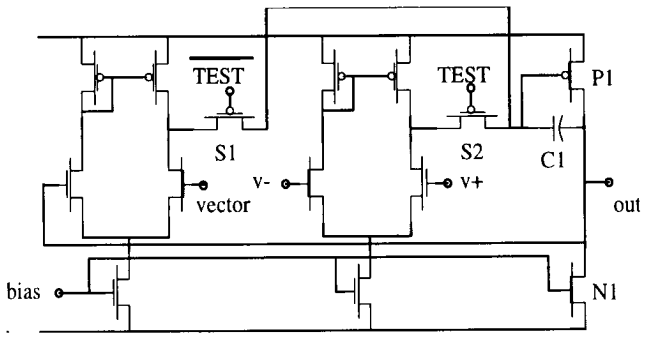

Fig. 5. Basic swap-amp structure

stability and the output stage has sufficient drive to overcome the feedback network, the actual feedback

configuration is of little consequence. This is a powerful feature of this DfT strategy.

5.1 Loading effect analysis.

For this analysis the swap-amp "normal" input stage is configured into unity gain mode, and a parallel load of 10pF and 100kΩ is applied to the output (Fig. 6a). The Miller capacitor C1 has a value of 4.68pF in both cases. A voltage step of 0V to +1V rising in 1μs is applied to the inputs during non-test mode. Switch **M8** is minimum sized (3μm by 3μm). As a second experiment the switch is moved so that it is in the large signal path between load and output node, shown in Fig. 6c.

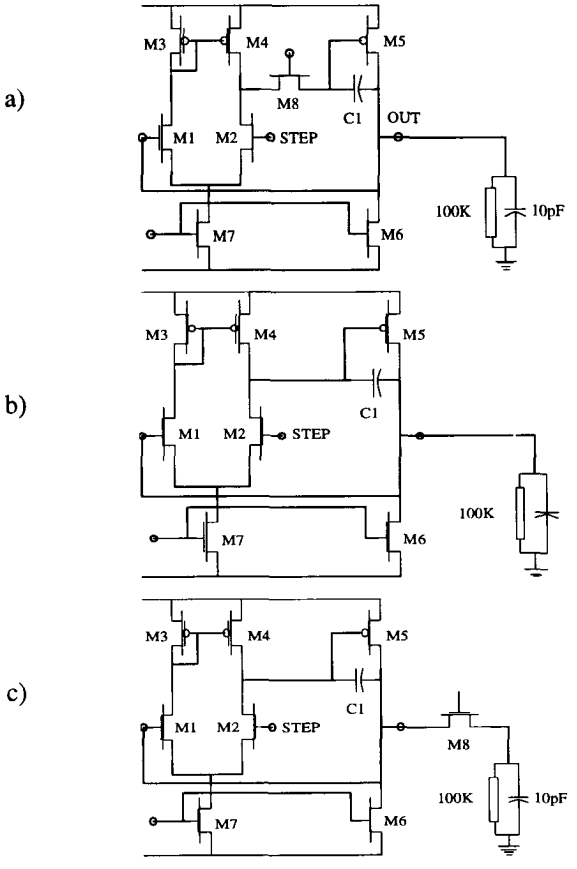

Fig. 6. Versions of the op-amp to be analysed. version (a) has the switch inserted in the small signal path, (b)) no switch inserted (c switch inserted in the large signal path

Also shown in Fig. 6b is the same amplifier but with no switches present. Fig. 7 shows a HSPICE simulation of the output voltages of the three amplifiers as the voltage step is applied. No obvious difference can be detected between the swap-amp and the non-switched amplifier plots but the action of the switch in the large signal path is obvious by its effect as a resistive divider in conjunction with the 100KΩ load and by a reduction in slew rate. Performing the necessary switching action within the small signal path shows obvious advantages in that bandwidth loss is greatly

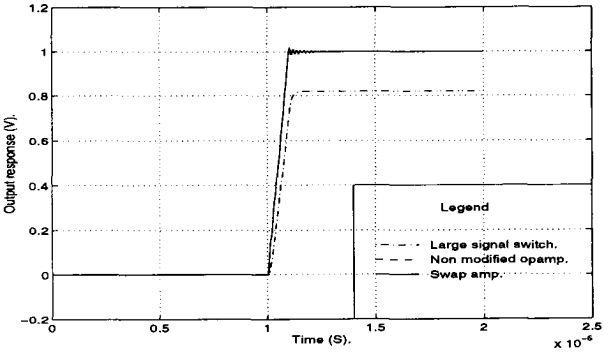

Fig. 7 HSPICE results for the circuits in Fig. 6

reduced and resistive dividers are not formed. The disadvantage is that small signal paths are not always abundant within designs in general and location of switches may become problematic. This is discussed in the next section.

6. Analogue DfT Scheme

The majority of analogue designs use analogue blocks with an operational amplifier driving the output node directly. This observation may be used to great effect in the implementation of a DfT philosophy. As mentioned in the previous section, it is possible to build an operational amplifier whose output voltage may easily be controlled in a test mode. The basis of this DfT strategy is that the controllable output of one block may be used to provide a set of voltage test vectors for a subsequent block. Fig. 8 shows how this is done.

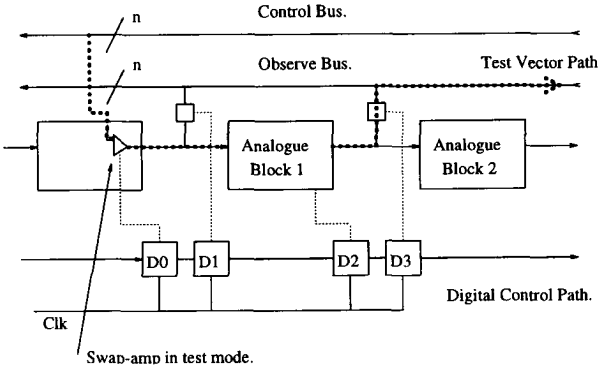

Fig 8.-The DfT strategy showing both access and observability features

This strategy also has the added benefit that inserting swap-amps into output node drivers is a sound idea from the point of view of design partitioning. In many applications, testability will be vastly improved by inserting a single additional access point into a design. However, monitoring the output of embedded blocks may in many cases be essential for optimal fault coverage. This is achieved by the use of analogue switches that place additional load on the output node. This will inevitably lead to a reduction in test mode performance over normal operation due to the reasons discussed previously. However, in non-test mode the effect of the observation switches is only to add a small parasitic capacitance to the output node of a block since all the observe switches are turned off. Hence performance loss in non-test mode is minimal and in practice it will often be possible to select a test output point that will be insensitive to this additional load.

7. PLL Test Circuit

The basic structure for the evaluation of the DfT philosophy described above is shown in Fig. 9. The reasons for choosing this structure are:

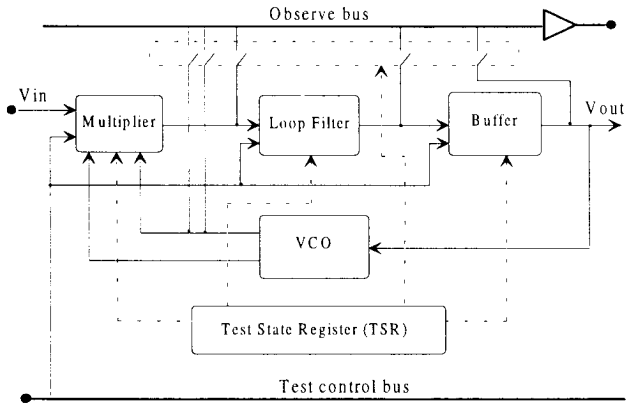

Fig. 9 PLL structure with DfT control

1. The PLL structure presents major testing problems due to the global feedback which makes isolation of cause and effect within the loop difficult. It also tends to mask soft faults [19] which may cause later problems due to reliability hazards or small functional changes with temperature.
2. Three of the four blocks have operational amplifier output nodes.
3. AC testing is necessary in addition to the usual DC testing to verify some of the circuit blocks such as the VCO and the loop filter [4].

A photograph of the fabricated chip is shown in Fig. 10. The test chip consists of two fault free versions of the PLL structure, one with the DfT modifications and one with no

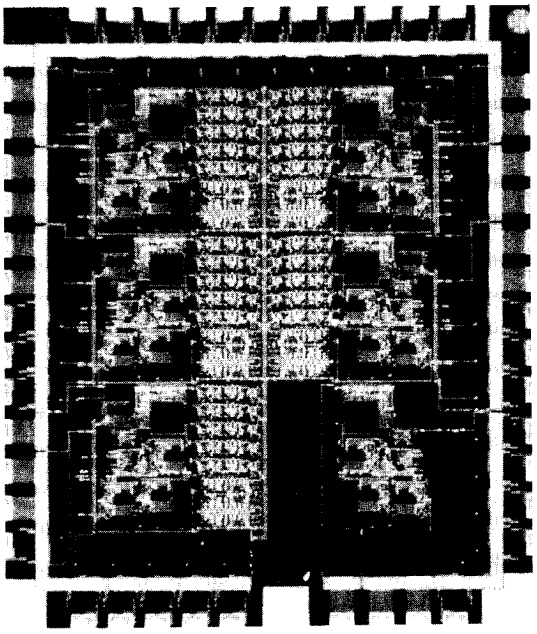

Fig 10. Test chip containing both faulty and fault free PLL circuits, with and without the DfT structures

DfT features. In addition, 4 copies of the DfT structure have been fabricated, each with a different defect inserted as described below. This enables performance evaluation on the DfT structures to be carried out against the non DfT structures and an assessment of the improvement in the fault detection capabilities to be made for each of the defects inserted. The device has been fabricated using the analogue 2.4μm double metal, double polysilicon Mietec process. The floorplan of the device is shown below.

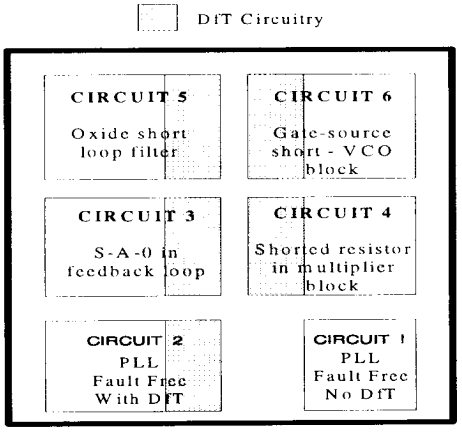

Fig 11. Floorplan of the test chip

7.1 Inserted Defects

The following defects have been designed into the replicated faulty versions of the PLL with integrated DfT circuitry.

7.1.1. Hard Faults PLL (circuits 3 & 4)

Two of the defective PLL circuits have had hard defects designed in. The first has a stuck-at-0 fault in the feedback loop as shown in Fig 12. Additional metal simulating a

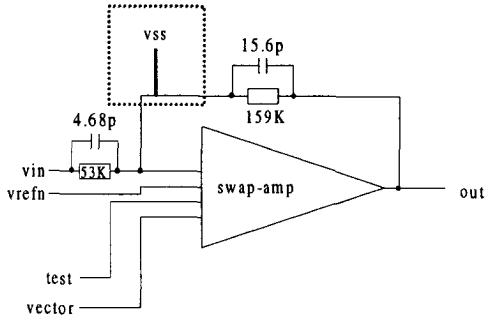

Fig. 12. S-A-0 short in feedback loop (circuit 3)

spot defect was introduced onto the layout. The second defective circuit has again had additional metal defined, but this time over the 4KΩ resistor snake in the multiplier block (Fig 13).

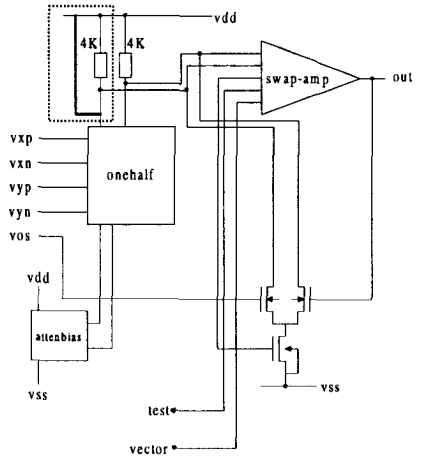

Fig. 13. Resistor shorted in 4 quadrant multiplier (circuit 4)

7.1.2. Soft Faults PLL (circuits 5 & 6)

The third defective PLL circuit has an oxide short as shown in Fig.14 fabricated in as a resistor snake in the loop filter. The 2nd soft fault fabricated into the fourth defective PLL circuit is a gate to source short in a P-FET in the VCO block

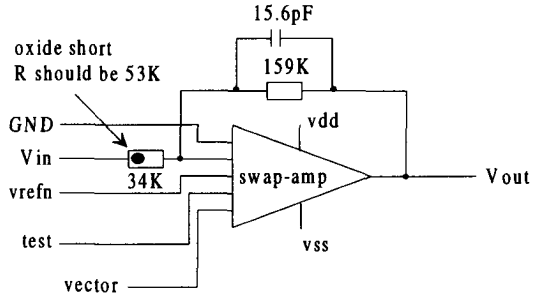

Fig. 14. Resistor snake shorted using a via to simulate gate oxide short in the loop filter block - (circuit 5)

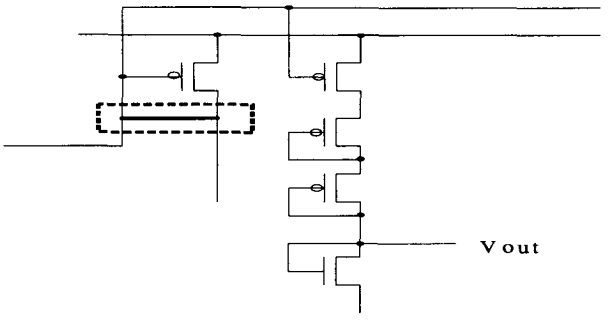

Fig. 15 - Gate-drain short in the VCO block.

8. Silicon results

10 sample chips were received from Mietec each of which contained a non-DfT PLL (circuit 1), a DfT PLL (circuit 2) and four DfT PLLs with faults designed in (circuits 3-6). Of these, 6 non-DfT and 8 DfT PLL circuit functioned. Non-functioning circuits had large DC offsets at the output node and were screened out on this basis.

A number of tests are available to evaluate the performance of a PLL such as DC offset, frequency capture range, frequency hold range, gain and locking time. A good initial test to use after the initial DC offset test is the frequency capture range of the PLL since this is approximately given by;

$$f_{capt} \approx \frac{1}{4} K_d K_0 A \left| F[j(\omega_i - \omega_{osc})] \right| \quad - \qquad (2)$$

where K_d is the gain of the four-quadrant multiplier block in Volts/Radian, K_o is the gain of the VCO in Radians/second Volt, A is the gain of the loop amplifier (V/V), ω_i is the input signal frequency, ω_{osc} is the VCO

centre frequency and $|F[j(\omega_i - \omega_{osc})]|$ is the amplitude response of the loop filter at the difference frequencies $(\omega_i - \omega_{osc})$. The frequency capture range thus includes elements of the transfer functions of all the major blocks of the PLL within one test. This is not true of either gain or hold range, neither of which are sensitive to the loop amplifier bandwidth.

Figure 16 shows a histogram of the frequency capture range of the non-DfT and DfT PLLs. Because of the small sample size it is difficult to draw firm conclusions but it is intuitively obvious that no major discrepancy exists between the two data sets. Both the average and spread of the two data sets is comparable.

If now the frequency capture range of the PLLs with the VCO output short are added to Fig. 16, shown in Fig. 17, then it is immediately apparent that there is a large shift in the faulty data set average compared with the previous two. This shift may be easily explained in that the amplitude of one of the VCO outputs is reduced by the

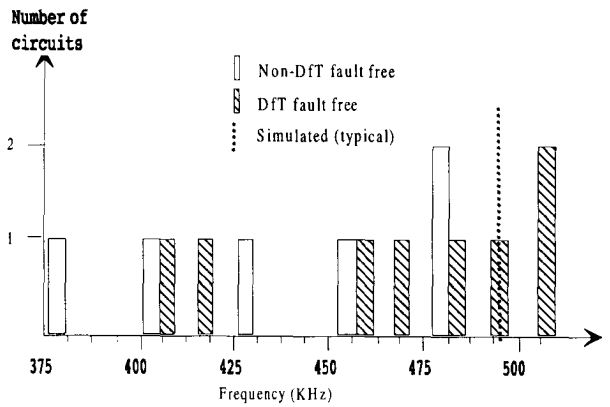

Fig. 16 - Capture range measurements on all functional samples of both the fault free PLL and PLL circuits with DfT

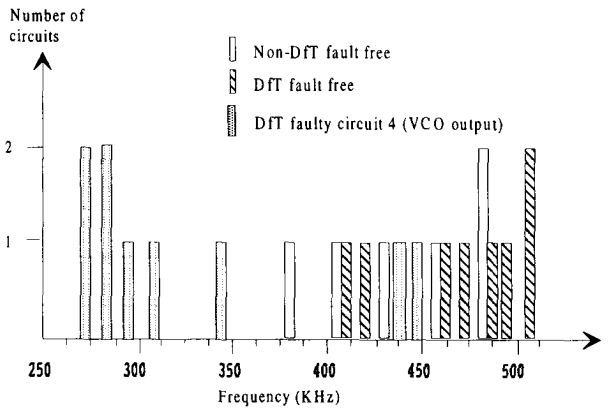

Fig 17 - Capture range for the DfT, non-DfT and faulty (circuit 4) versions of the PLL for all working samples

presence of the short circuit (see later). This has the overall effect of reducing the gain of the multiplier block because it is apparently presented with smaller input voltage magnitudes. The frequency capture range defined by (2) is reduced as a result. On the basis of a capture range test the majority of such faults are easily detectable.

However, it should be noted that two of the faulty PLL circuits show capture ranges of 444KHz and 436KHz which lie well within the normal response range. It has been found that the total loop gain of these two circuits is unusually high due to parametric shifts in the other blocks. The effect of the faults on the capture range are masked as a result.

Using the observe bus it is easily possible to look at the differential outputs from the faulty VCO block of the PLL with 436 KHz capture range. The results of this observation are plotted in Fig. 18 along with a fault free

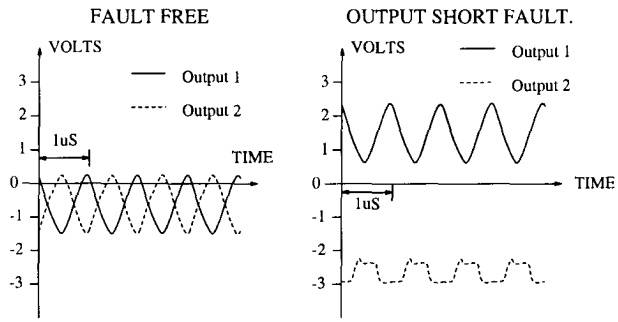

Fig 18 - a) fault free output from VCO output node and b) -VCO output response of faulty PLL version 2, IC number 7,- both measurements using the observe DfT feature

example for comparison. Major differences in the plots are obvious with a large DC offset of 4 volts appearing between the complimentary outputs of the faulty VCO. The reduction in signal amplitude of channel 2 of the faulty VCO is also obvious.

In switching internal nodes of the PLL onto the observe bus the effects of loading must be carefully considered. Figures 19 and 20 show the effect of this loading for the fault free DfT circuit of IC number 7. Gain and frequency hold range are used here since they most reflect the effects of loading. The performance shift caused by loading the VCO outputs with the observe bus (state codes 2 and 3) is obvious. Hold range is reduced at the upper frequency values and hence the total frequency range is reduced because the VCO becomes slew-rate limited and its output magnitude falls at high frequencies as a result. The reduction in gain is due to a reduction in the output magnitude of the VCO block again by slew rate limiting at high frequencies. In this example gain has been measured at the upper end of the frequency hold range. At lower

frequencies the effect is less pronounced because the slew rate limiting becomes lesser in effect.

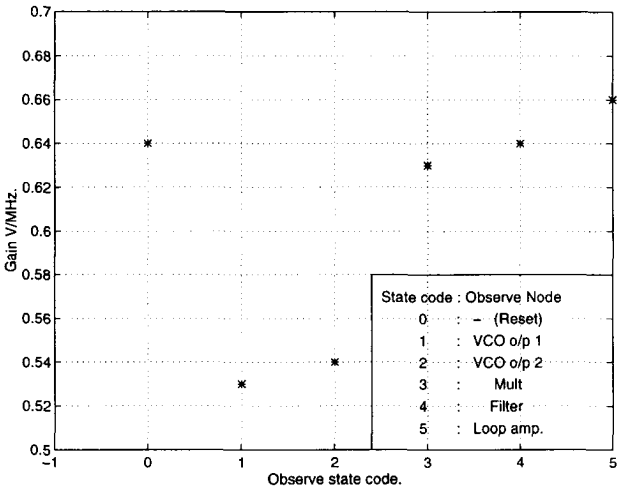

Fig 19 - Effect on the PLL gain of switching observability structures onto the test bus

State codes 3,4 and 5 of figs. 19 and 20 represent the output voltages of the multiplier, loop filter and loop amplifier respectively as they are connected to the observe bus. Within the measurement errors there is no detectable change due to loading because these outputs are strongly buffered and the additional loading of the observe bus has little impact on the overall performance.

It can be concluded that sensible use of the observe bus

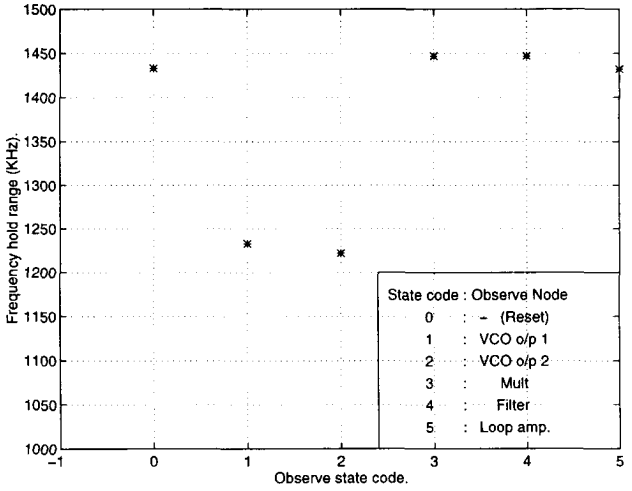

Fig 20 - Effect on the hold range of switching observability

allows on-line testing of the PLL if strongly buffered nodes are observed. In the case of the VCO outputs which are not strongly buffered, loading effects are noticeable at the higher frequency ranges. However, off-line diagnostics can be performed as for the traces shown in Fig. 18 and still yield useful results.

The soft defect inserted into the loop filter shown in Fig. 14 was anticipated to cause a small shift in the loop gain. In fact, of the 10 samples tested, 7 failed totally with large DC offsets at the outputs. Of the remaining 3, all yielded very poor performance with no observable lower lock and capture frequencies and very noisy outputs. These effects were not anticipated and the swap-amps were employed to locate the problem.

The Test State Register (TSR) was configured into state 0010 1000 where the multiplier swap-amp is in test mode and the output of the loop filter is connected to the observe bus. In this state the multiplier block is used to provide test vectors for the subsequent loop filter block. Table 1 shows the results of DC measurements of the gain

Test voltage	Output expected	Output measured
-0.100V	0.470V	0.971V
0.000V	0.000V	0.059V
+0.100V	-0.470V	-0.775V

Table 1 - DC measurements of the gain of the loop filter using the multiplier swap-amp.

of the loop filter. The cause of the large discrepancy between measured and expected values remains unexplained as yet but its effect is to saturate the loop amplifier which is the subsequent stage. As a result a large DC offset (in fact saturation) appears at the output node of the PLL and the VCO does not oscillate as a result. Using the swap-amp has made detection of this problem easy and has allowed location of a problem which was not originally anticipated.

9. Conclusions

A reconfigurable operational amplifier, called a swap-amp, has been built and described. The swap-amp facilitates exposure of faults within a custom built phase-locked-loop (PLL) circuit by providing means to invasively control voltage levels of the PLL internal nodes. Comparison of nominally identical PLL circuits in terms of frequency capture range has shown that the performance impact of introducing the swap-amp is negligible in normal operation mode.

A methodology based on an analogue observe bus has been described which allows observation of the internal voltage levels of PLL inter-block nodal voltages. It has been shown that use of this observability bus is feasible while the PLL is still performing its normal function, i.e. allowing on-line functionality evaluation, by measuring the gain and frequency hold range of the PLL while

simultaneously observing internal voltage levels of the PLL. It has also been shown that loading effects of the bus capacitance may cause shifts in the performance of the PLL if weakly buffered nodes are connected to the observe bus. Under these conditions the use of on-line performance evaluation is not recommended but use of off-line testing has been shown to be a very simple way of detecting faults such as the example short-circuit in the VCO output.
In particular, it has been shown that a short circuit fault in the VCO output leads to a number of faulty chips that are easily distinguishable on a frequency capture range test. However although the majority of faulty VCO chips fail this test it has been demonstrated that a number give obstensively normal results. Use of the observe bus allows the VCO fault to be easily distinguished from the fault free case.

The swap-amp in conjunction with the observe bus has been used to isolate a fault within several of the PLL chips which causes total failure of the PLL by saturating the output operational amplifier. Without the presence of the swap-amp structure, location and diagnosis of this fault would have been extremely difficult.

The present area overhead due to the swap-amps is minimal, comprising approximately 5% increase per modified operational amplifier. The corresponding figure is approximately 1% for the PLL circuit as a whole. The logic necessary to control the test state of the PLL, the TSR, represents an area overhead of approximately 100% which is not acceptable. A number of possibilities exist to significantly reduce this overhead.

1. Use of an Algorithmic State Machine rather than a "one-hot" TSR will reduce the number of necessary D-type flip-flop elements to four rather than the present eight to represent the present nine test states.
2. Much better designs of D-type flip-flop exist than the one used here. A area reduction of more than 50% is easy to foresee.
3. Use of a full-custom layout rather than the present automatic version will trim around 25% off the area necessary for the TSR.

The total accumulative reduction in area of the TSR is anticipated to be approximately one order of magnitude and the total resultant area overhead is estimated to be about 10%.

It should also be mentioned that the amount of observability and controllability applied to the PLL is excessive in this demonstrator chip with respect to that which is likely to be required. Reductions in the quantity of both observability and controllability will lead to a smaller TSR and a smaller area overhead as a result.

In a mixed-signal environment it is often the case that a number of digital signals are available for little cost during the test phase. If these signals could be employed in place of the TSR then the total area overhead is estimated to be about 1%, representing that of the swap-amps and obseve switches only.

9.1 Future Work.

The first step is to re-design the TSR with the proposals above and obtain an estimate of the total minimum area required for the TSR. Fabrication of this step may well not be necessary and results can hopefully be obtained quickly.

More investigation is necessary into the reasons for failure of a number of the PLL chips. Utilisation of the swap-amp and observe bus will facilitate this task and a subsequent paper on fault diagnosis is anticipated.

Other applications for the swap-amp need to be investigated. In particular only one architecture of swap-amp exists at present and there is almost certainly need for the re-configuration technique to be applied to transimpedance amplifiers and current mode devices to name only two.

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