MIXED-SIGNAL CUSTOM IC CONTROL PROCESSORS INCORPORATING DESIGN FOR TEST/SELF-TEST

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Abstract

With the continued move towards higher integration and the concept of "systems on a chip", the realisation of custom DSP chips aimed specifically at measurement/control systems is becoming a potential solution. Size reduction, operating speed increase, increased functionality and improved reliability can be achieved by using a single custom IC (Application Specific Integrated Circuit - ASIC) or Multi-Chip Module (MCM) solution with the majority, or all, of the electronics mounted in a single package. Here, a DSP core optimised for the application surrounded by the necessary Input/Output signal conditioning circuitry can be used. However, the increased level of integration requires suitable fabrication processes and effective "Design for Test" to ensure the integrity of both the design functionality and fabrication.

1. Introduction

The electronic controller within a typical closed-loop control system[1][2] requires a range of engineering disciplines to realise the final solution. Such a complex engineering task can raise a number of important issues in both what is the final aim of the task and how can it be realised. Issues include design time, utilising the appropriate technologies and the choice of implementation method to provide a high confidence level in the integrity of the final solution, both at the manufacturing and utilisation stages. Additionally, where problems do occur, the ability to identify and correct the problems is essential. This is particularly important within the field of microelectronics, which underpins the base electronics for many circuits/systems. Increasing application areas and device complexities require careful evaluation to ensure adequate testability[3] of these devices at minimal cost. After all, where silicon integrated circuits can consist of anything from a dozen or so, to in excess of 3 million transistors, where the forecast is for the ability to design devices with 20 million transistors[4] per device by the year 2000, the functionality of the devices is increasing, which in turn requires an additional means to ensure problematic devices are identified during device production and are not passed onto the end-user.

Whilst it is necessary to ensure that the designs realised are functionally correct, the application areas for these types of devices are ever increasing, producing additional problems in device evaluation. Control systems, which are discussed within this paper, are an ideal target application for custom integrated circuits (ICs). The idea here is to take the high level control algorithm and to implement it in a suitable technology, which provides the optimum solution for the given system requirements. Whilst the control algorithm can be mapped from the mathematical equation governing the control law to the electronics in a number of ways, see table 1, no

Electronic Circuit Type	Control Law Operations	Circuit Design Method
Analogue	Add, Subtract, Multiply, Divide Integrate, Differentiate	Hardware only (op-amp, transistor, passive components)
Digital	Add, Subtract, Multiply, Divide, Store	Hardware only, Hardware-Software Co-Design (combinatorial/Sequential logic, embedded code, microprocessor/DSP, custom processor)

Table 1 : Control Law - Electronic Circuit Mapping

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consideration is given in this table to which solution provides the best results and how can these be realised as an electronic circuit. Additionally, an area of the design decision process that is missing from the above description, which is in many cases an after-thought and can result in the need for system re-design, is the issue of the testability of the base electronics. This must be considered by the designer from an early stage in the design specification definition if it is have maximum benefit and minimise design time, and hence costs. The consideration of the testability at this early stage, referred to as *Design for Test (DfT)*, is not a new concept and is standard practice within the microelectonics industry. Integrated Circuits have come a long way since the first microprocessor designs and now the terminology "systems on a chip" is becoming widely discussed and is one of the goals for people wishing to provide high levels of functionality with minimal size requirements. Whilst this goal resolves a number of problems in providing the ability to perform complex functions in a small package, it creates new ones which need to be resolved. Whilst the aim of this higher integration has many advantages, particularly where size, weight and operating speed are important issues, allowing the designer requiring the base technology to take full advantage of the benefits a particular technology may have to offer, the designer must be supported with the best means of realising the design specification, which can be fabricated and ready for use in minimal time with a level of confidence that the device is fully functional and where appropriate, have the ability for self-test and diagnostics.

This paper will discuss the design of custom IC, also referred to as ASIC (Application Specific Integrated Circuit), based solutions for control system applications utilising re-usable library macros optimised for control. By reference to a design case study, the advantages of this type of approach will be discussed. As the "system on a chip" concept becomes widely established, the designer will be required to consider the design at a higher architectural level with the emphasis on the system needs in order to optimise the data flow between functional blocks (macros), minimise interconnect delays within the digital processing, minimising the power consumption of the device, allowing flexibility and reconfigurability, realising effective testability (on and off-line) in addition to producing a design that performs to the required specification whilst incurring minimal cost, both for the design generation and production testing of the device.

2. Custom ICs for Controller Operation

Since complex functions can be implemented on silicon, as analogue, mixed-signal and digitally based circuits, and for digital, as hardware/software or hardware only solutions, the types of functions typically required for control systems can be mapped as silicon based operations. Such solutions include PID[5][6][7] and fuzzy logic control[8] and have been proposed/demonstrated in a number of "off the shelf" programmable or custom devices. The question, from a testability perspective is how was the design generated to include specific modes of operation to check the integrity of the device, both from a device fabrication perspective and from a self-test whilst within the control loop? For digitally based designs, where would the partitioning of the hardware and (any) software be made, primarily for the circuit operation, but also to enable testability to be incorporated, which can aid the DfT approach since both hardware and software methods can be used to operate the test facilities? Utilising the existing circuitry also provides benefits in reducing the size of the design, hence costs as fabrication costs are dependent on the size of the silicon die and reduces the amount of additional circuitry required.

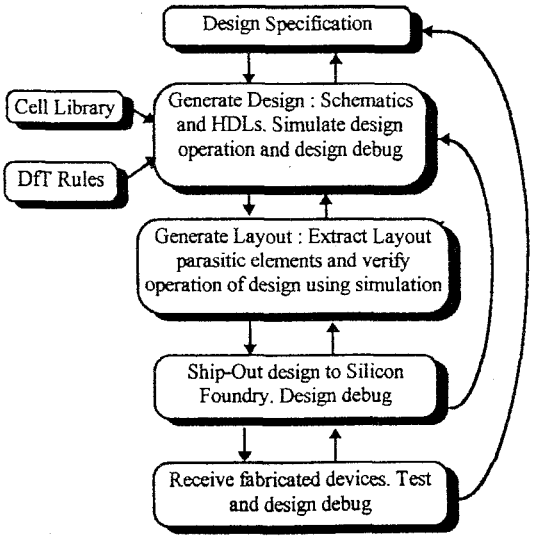


Figure 1 : Realising a custom IC solution

A number of ASIC controllers have been developed and demonstrated[5][6], providing solutions from devices specific to a single type of control system application through to generic architectures, incorporating differing levels of DfT. These have demonstrated how microelectronics can be used to generate both digital and mixed-signal designs, providing a number of the required functions required to interface to the plant and sensors. Figure 1 identifies a number of key steps in the design of such devices. For example, for a digitally based control algorithm to be interfaced to the plant and sensors in the analogue

domain, analogue to digital converters (ADCs) and Digital to Analogue Converters (DACs) are required. The choice of these is dependent on the particular system requirements and availability of these types of cells. For designs realised in a number of foundry processes, these can be found within the cell library provided by the foundry. Where these cells are deficient, the process user must design the cells at a full-custom level.

3. Why Design for Test?

Consider the situation. A control law is to be implemented as an electronic circuit. The only possible solution requires the use of an ASIC which comprises a digital core (e.g. controller DSP plus memory (ROM/RAM)) and analogue front and back-ends (ADCs and DACs). The silicon die is to be mounted directly into the housing of the machine it is to be controlling with minimal connections to the outside world. The system is such that the controller is to ensure that it has a self-check capability and can flag any errors, ensure the plant is placed in a safe operating mode should any errors be detected and then to provide a diagnostic capability to an external monitoring device through its' on-chip communications port. How is this to be done? The choice of solution will be based on a number of (usually conflicting) requirements, not the least device cost. Basically, there are two questions to be answered for the planned incorporation of testability :

1. What is the aim of the testing?
2. Where is the testing to be performed?

These must be considered during the design specification definition and are related to the fabrication process to be adopted. The decision is somewhat aided by the availability of cells within the design library. Specific cells are usually provided by the foundry to enable basic digital DfT to be incorporated, such as Scan Path Testing[3], but in the main it is the responsibility of the designer to ensure adequate testability is obtained. Additional macro cells such as multipliers, ROM (Read Only Memory) and RAM (Random Access Memory) can be provided and the choice there is usually whether to utilise BIST (Built-In Self-Test) or to exercise the design using an external tester. Again, the choice must be made for the particular design, adopting a suitable set of structured DfT rules, see figure 2.

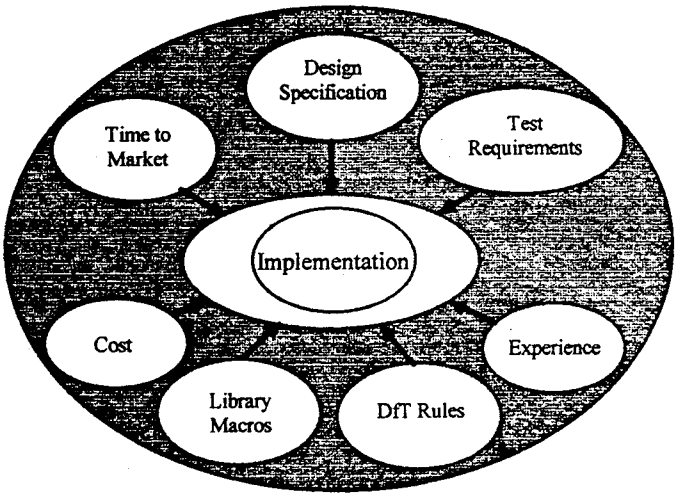


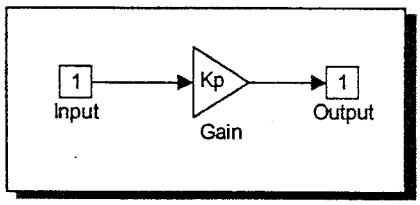
Figure 2 : Realising DfT

The self-test function can be designed to be made "off-line" incorporating device specific test modes of operation, or "on-line" where the design checks itself during the normal operation cycle. However, for "on-line" methods, it is required that the self-test exercises the device through an adequate sequence of events that does not corrupt data within the device, does not affect external devices and which targets potential faults that could occur during normal operation. For closed-loop operation, it may not be possible to exercise all circuitry within the design self-test since, for example, the controller effort signal at the device output must not be changed except to provide the required value. The results from any self-test function may potentially corrupt this data, so propagating an incorrect signal to the plant. Similarly, self-test must not corrupt sensor input data, so propagating incorrect controller input.

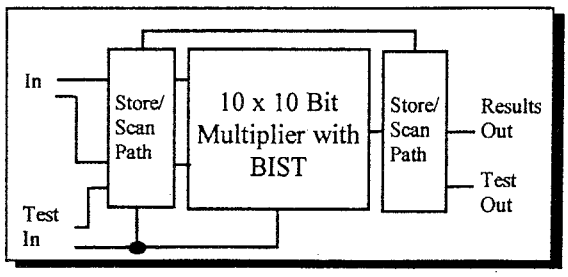
4. CACSD Vs Implementation

The design of the control system will, at some stage within the adopted design flow, require the use of a Computer Aided Control System Design (CACSD)[9] package such as MATLAB/SIMULINK[10]. Whilst this is essential to the development and analysis of the control algorithm, the implementation of the resulting control law may not necessarily have any relation to the hardware/ software system. The development stage using CACSD can either be independent of the implementation method or can be directed to an extent by providing a library of macros to perform allowed operations. Should these be linked to the ASIC library macros, then the

resulting ASIC design and testability issues can be assisted, since such a structured approach can utilise structured DfT methods that link the complete design, test and evaluation of the target design. Figure 3 shows how different representations of a single cell exist, here showing a MATLAB/SIMULINK (CACSD) schematic



MATLAB/SIMULINK Model for Proportional Gain Block



Block Level Schematic for Proportional Gain Block in a Controller ASIC Design

Figure 3 : CACSD Vs Library Macro

of a proportional gain block and the circuit level schematic of a 2s complement hardware multiplier to perform the action, along with additional BIST circuitry. The multiplier itself would be multiplexed within the digital processing core to enable the single cell to perform several multiplications, as described in the control algorithm.

5. Conclusions

This paper has presented a number of issues relating to the design of custom Integrated Circuit solutions for control system applications and the need to ensure that the devices are fully operational, including the design architecture, fabrication and "on-line" operation perspectives. The choice of how the device is to be created to be testable, including additional modes of operation to perform post-fabrication production testing and "on-line" self-test and diagnostics were discussed. Whilst the incorporation of DfT methods is essential, this does incur a cost penalty and so decisions need to be made with care and on a device-by-device basis. Ad-hoc methods are best replaced by structured DfT decisions and would allow the designer greater input in creating the optimal device, both for the operational and test modes.

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