# Investigations for Minimum Invasion Digital Only Built-In "Ramp" Based Test Techniques for Charge Pump PLL's

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## Abstract

Due to a number of desirable operational and design characteristics, CP-PLL's (Charge Pump Phase locked loops) have, in recent years become a pervasive PLL architecture. CP-PLL architectures are exploited for a variety of applications such as on chip clock generation, CRC (clock recovery circuits) and Radio frequency synthesis applications. This paper describes a simple, digital only, minimally invasive and fully automated test approach for high performance CP-PLL's that can be used to provide more information about the CP-PLL function beyond that obtained through the commonly used FLT (Frequency Lock Test). The test strategy described here allows the estimation of forward path (FP) gain and relative leakage in the forward path loop components. Applications of the test are focussed towards digital only testing of fully embedded CP-PLL's, however further test modifications could yield marked test time improvements for embedded and board level CP-PLL's incorporating multiple CP currents and or multiple loop filter (LF) configurations.

**Keywords:** Phase locked loop, Charge pump, Phase frequency detector, Voltage controlled oscillator, BIST, Dft, Test, Jitter.

## 1. Introduction

In recent years the CP-PLL has become a commonly used M/S (Mixed Signal) building block. A popular application for the CP-PLL is for on chip clock regeneration. All other on chip functions will be reliant on the PLL function, thus it is essential that it is verified correctly. Unfortunately, problems relating to test time, and test access, can lead to the PLL being insufficiently tested. Often only a simple FLT is implemented on the PLL. Although the FLT will uncover many internal hard faults, [1][2] it does not generally provide sufficient information relating to short-term transient characteristics (instability and jitter effects). Parameters, such as CP mismatch, CP leakage, CP non-linearity, LF (loop filter) leakage, voltage controlled oscillator (VCO) non-linearity and static phase offset can have a significant impact on PLL performance. In consequence there has been recent interest in methods that can provide enhanced PLL test support.

Initial focus for the test strategy described in this paper is towards fully embedded CP-PLL's. These types of PLL's are generally used for on chip clock synthesis, and in many situations comprise the only analogue circuitry on a large digital SOC (System on Chip). In consequence of this fact a significant motivating factor is towards tests that can be facilitated using a digital only tester. Furthermore, it must be emphasized that for PLL's incorporating embedded loop filter components, the physical capacitance of the main LF capacitor is relatively small (in the order of 100pF) when compared to external components, also considering that the LF node is a critical controlling node of the PLL, screening of this node is usually required. Thus in direct consequence, another test motivation is to facilitate tests without access to the LF nodes.

It must be noted that although the main focus of this paper is towards the test of fully embedded CP- PLL's, many of the suggestions are directly applicable to the test of "Chipset" PLL's that have external LF components. PLL's utilising external LF components are widely used in cellular RF (Radio Frequency) applications, however, in the trend towards miniaturization it is likely that many of the current chipset applications will become fully embedded. In either case the volume of communications applications is great and in consequence, any test methods that have the potential of reducing test time or allow reliable fast screening of defective components are to be preferred.

Further explanations and motivations towards BIST solutions, such as reduced pin count and better integration into a higher level test plan are provided in [3].

Valuable information concerning the characteristics mentioned in the previous sections can be generated by applying stimulus to the PLL FP whilst the PLL is operated in an open loop (OL) configuration. Using

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selected sequences allows extraction of information appertaining to FP gain, FP non-linearity, and leakage and mismatch in critical FP blocks. It will be explained in later sections of this paper, that any of these errors can lead to close in phase noise (or jitter) on the PLL's output. Any direct measurement of jitter at the PLL output will include jitter due to the aforementioned errors as well as jitter due to oscillator noise. Although the test approach mentioned in this paper does not cover direct measurement of jitter, this does not mean that the problem is disregarded. It is recognised that certain non-idealities will produce output jitter. However, it is also noticed that PLL jitter is not the only parameter of importance relating to PLL evaluation. Other parameters include the FP gain estimates and estimates of settling time (from the FLT) are equally important. In many communications applications settling time and linearity of the FP components will be particularly important. As the FP gain measurements are relatively simple to make when compared to jitter measurements, and will uncover some chief jitter contributors it is sensible to carry out these tests prior to any more elaborate jitter measurements, thereby facilitating "fast binning" of defective components. Suitable references concerning non-idealities and their relationship to phase noise are provided in section 3. For completeness, concerning on-chip jitter measurement techniques, various direct methods have been suggested [4][5][6] but all require a clean reference clock for sampling purposes, this clock may not be available for all applications. In addition, [7][8] give methods of jitter extraction without an external reference clock.

In recent years various solutions for PLL BIST (Built In Self Test) have been presented [4][9]. All of the BIST techniques use a common method of measuring the VCO output frequency to give an indication of the test output response. The test method proposed in this paper uses the same approach for response evaluation, however, the method of stimulus injection is innovative, requiring only the insertion of one T flip-flop into the PLL input path whilst the PLL is in test mode. Furthermore, response monitoring is based upon measurement of relative and absolute FP component leakage rates during a "hold mode". Although the "hold mode" is carried out in an open loop configuration, application of identical signals to the PLL inputs emulates an ideal locked condition. Note that this condition will only be true for the most commonly used PFD (Phase and frequency detectors). The technique allows measurement of leakage / mismatch effects that would normally not be observable whilst the PLL is in a closed loop configuration. Measurement of leakage and mismatches in this way has not been mentioned previously. Principles of this test approach are provided in sections 2 and 3. Note that the flip-flop and signal redirection circuitry are switched out of the critical signal paths when the PLL is in mission mode. In addition, techniques to allow relative measurements of multiple loop settings are provided in section 4. These techniques are to the author's knowledge entirely new.

A summary of the paper including further and ongoing work is provided in section 5.

## 2. Basic PLL architecture and operational description.

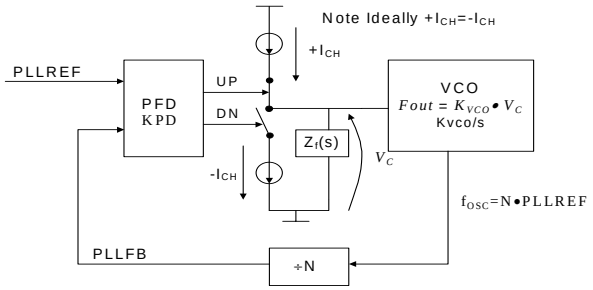



**Figure 1 Basic PLL architecture**

*KPD = Phase detector gain = Ich/2π (A $r^{-1}$)*

Zf(s) = Loop filter transfer function

*Kvco = VCO gain* *($r\ s^{-1}\ v^{-1}$)*

In figure 1 PLLREF and PLLFB are pulse streams. The phase frequency detector is an edge sensitive device that closes UP or DN for a time proportional to the time difference between the PLLREF and PLLFB edges. This action charges (or discharges) the LF (Zf), thus $V_C$ increases (or decreases), and $f_{osc}$ increases or (or decreases).

In normal operation, connection of the blocks as shown, allows generation of an output signal that is phase aligned to the input signal. Further information on CP-PLL operation can be found in [10][11][12].

To further illustrate the operation of the PFD, LF and CP combination, the waveforms for PLLREF = PLLFB / 2, with the PLL in an open loop configuration, are illustrated in Fig. 2. This basic operation can be exploited to facilitate testing of the forward path blocks of the PLL.

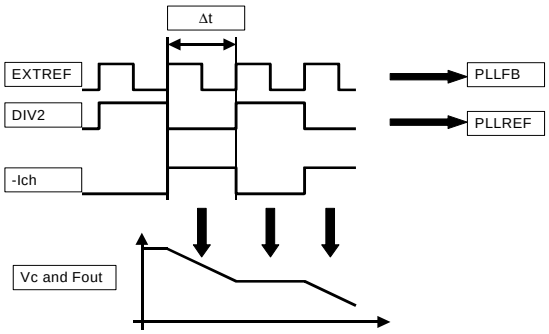



**Figure 2 Wave forms for PLLREF = PLLFB/2**

(Note: Extref is the external clock reference to the PLL and DIV2 is the divided output derived from EXTREF. Also the bottom graph indicates that Vc changes in proportion to the input stimuli and that the frequency output of the PLL (Fout) will change in proportion to Vc ) It is important to note that in figure 2 if the signals on PLLFB and PLLREF are swapped Vc($F_{out}$) will increase.

## 3. Ramp generator circuitry and vector application.

When considering generic digital only test of embedded CP-PLLs the following main constraints were identified.

- No access to critical analogue PLL nodes, e.g. the loop filter node.
- The test must be fully autonomous.
- Outputs must be in a digital only format.
- Hardware overhead should be small enough to allow the circuitry to be included as part of the PLL core.

Further identification of critical nodes and generic test methodologies are given in [9]. With this in mind the underlying principles of the test are given below.

It must be noted that the term "Ramp" in the context of this paper does indicate that the test input stimuli is a ramp, but indicates that the output response of the PLL, is in the form of a ramp (cf. figure 2)

### 3.1. Forward path transfer equations for open loop CP-PLL.

Figure 3, illustrates a commonly used configuration for Zf(s):

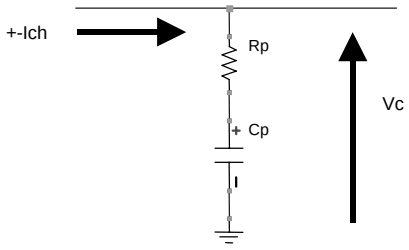



**Figure 3 Typical loop filter configuration.**

For a positive input current (Ich) the continuous time domain response for this network is:

$$Vc(t) = Vstart + Ich \cdot \left( \frac{t}{Cp} + Rp \right) \qquad (1)$$

(Where t represents the time the input current is applied for, and Vstart is the initial value of Vc.)

Equation (1) is valid for a constant current, however when considering the waveforms of figure 2 we note that the applied drive current is essentially zero for a portion of the cycle, hence the voltage drop across Rp is removed and only Vc remains. Thus (1) is modified as.

$$Vc(t) = Vstart + Ich \cdot \left( \frac{t_N}{Cp} + Rp \right) - Ich \cdot Rp \qquad (2)$$

and (2) can be rearranged to yield

$$Vc(t) = Vstart + Ich \cdot \left( \frac{t_n}{C_p} \right) \quad (V) \qquad (3)$$

(Where $t_N$ represents the total accumulated time of the current pulses.)

The above equations are valid for a linear CP structure. From (1), (2) and figure 2 it can be seen that forcing a time delay between the edges of PLLFB and PLLREF whilst the PLL is in an OL configuration will allow the CP and LF components of the PLL to be exercised. This technique can be used to allow direct mesurment of the forward path PLL blocks (FP gain estimation).

From [11] the Laplace domain open loop transfer function of figure 1 is

$$Ho(s) = KPD \cdot \left( Rp + \frac{1}{s \cdot Cp} \right) \cdot \frac{Kvco}{s} \qquad (4)$$

Taking the inverse transform of (4) and modifying as in 2 yields.

$$ho(t) = \left[ Ich \cdot \left\{ \frac{tN}{Cp} + Rp \right\} - Ich \cdot Rp \right] \cdot \frac{Kvco}{2\pi}, \ (\text{Hz}) \qquad (5)$$

Using (5) it is possible to obtain a measure of the FP PLL gain in terms of frequency change at the PLL output with respect to a time delay applied at the input.

### 3.2. Test architecture.

The basic test architecture is illustrated below.

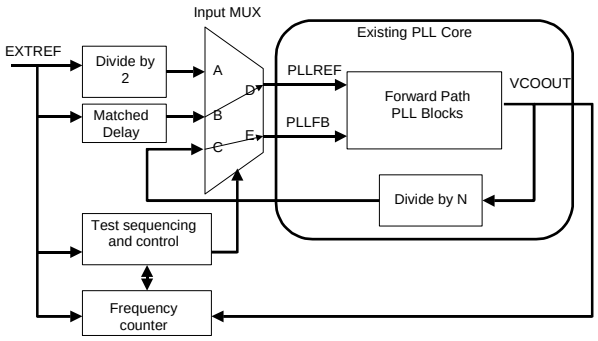



**Figure 4 Basic test architecture**

In figure 4 the connection arrows indicated in the Input MUX block show the PLL connected in normal operational mode. The most important part of the Input MUX design is ensuring that delays are matched for the signal paths in operational mode and test mode. For example, in figure 4 the matched delay block compensates for the delay of the divide by two block. Careful matching of the delays will help to mitigate any constant offset errors that will affect measurement accuracy, and most importantly will ensure that test circuitry does not adversely effect the PLL operation. A simplified diagram of the input MUX is shown below. The dashed lines indicate the signal flow when the PLL is configured in a normal operational mode.

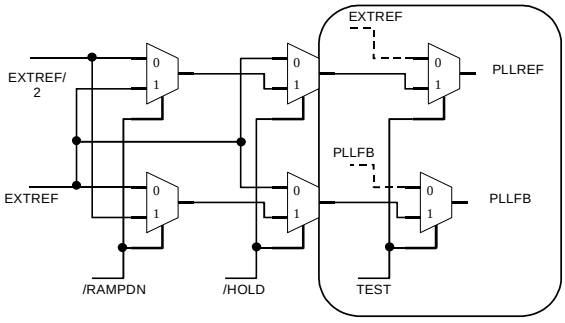



**Figure 5 Detail of input multiplexer**

As can be seen in figure 5 when the PLL is in normal operational mode only one 2 input MUX delay is present in each PLL input path. It is likely that to achieve optimal performance for a high speed PLL system, the highlighted MUX circuitry would have to be subject to hand layout techniques. However, this will be an insignificant overhead when weighed against the added value in terms of test access. It is important to note that as the test mode circuitry (non highlighted circuitry) is operated at relatively low speeds, the matching requirements for this circuitry is not as severe, thus automatic layout can be used for the remainder of the test circuitry. In addition, it must be mentioned that all of the referenced BIST techniques [3][4] include multiplexers in the signal paths, therefore the same design constraints will apply, especially when considering high speed and high performance PLL's.

The Input MUX (and other depicted circuitry) has been evaluated on an FPGA and by using symmetrical design techniques, delay matching errors present at PLLREF and PLLFB have been minimised. The propagation delays between the input signals from the multiplexer have been examined on an oscilloscope and appear to introduce negligible delays.

It is important to note that recently tests have been published that propose application of stimulus injection directly to the charge pump switch control inputs [4]. However, the UP and DN CP switches are not operated on a cyclic basis, with current being applied continuously to the LF structures during ramp up and ramp down mode. A major draw back of this approach is that for practical CP-PLL implementations the switches are constructed from PMOS and NMOS transistors and during each operation charge is stored on their associated capacitances and subsequently discharged to the loop filter node. A continuous application of current will not highlight effects due to charge injection; additionally errors in circuitry often used to cancel charge injection effects, may not be exercised.

### 3.3. MUX connections and output results for basic test vectors.

The following table describes the tests carried out for various Input MUX connections (cf fig 4)

| Step | Description | MUX Connections | | Result |
|---|---|---|---|---|
| 1) | Frequncy lock test (normal operation) | D=B | E=C | F1 |
| 2) | Ramp down (OL) | D=A | E=B | F2 |
| 3) | Hold mode (OL) | D=B | E=B | F2 |
| 4) | Ramp up (OL) | D=B | E=A | F3 |
| 5) | Hold mode (OL) | D=B | E=B | F4 |

**Table 1 Multiplexer connections**

(Note that F# indicates the frequencies measured at the end of each test phase.)

Using the above connections in conjunction with suitable sequencing will allow comparison of counted output frequencies (F1 – F4) against expected results. The table below outlines typical information that can be inferred from the tests.

| Step | Description | Information | Value |
|---|---|---|---|
| 1) | Frequency lock test | Ensures lock is attained Sets reference | F1 |

| | | | |
|---|---|---|---|
| | | frequency<br>Exercise all PLL components at maximum frequency (with N set to Nmax) | |
| 2) | Ramp down | Gain of forward path PLL components. | F1-F2 |
| 3) | Hold mode | To allow measurement of F2. | |
| 4) | Ramp up | Gain of forward path PLL components.<br>CP / VCO non-linearity (with extra stages). | F2-F3 |
| | | Charge pump mismatch. | F1-F3 |
| 5) | Hold mode | Loop filter leakage / Charge pump leakage.<br>Excessive phase offsets in the forward path. | F3-F4 |

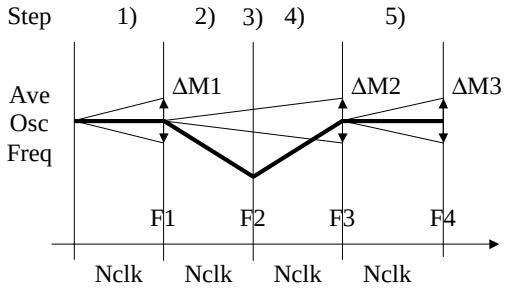
**Table 2 Summary of output response from tests.**

Note that in step 1) if the feedback divider (cf fig 1) is set to its maximum setting $F_{out}$ will be at a maximum. Enforcing this requirement for the test will ensure that all of the PLL components are exercised at maximum operational speed, after this, simple functional tests will be adequate for feedback divider testing.

Also in steps 2 and 3 applications of the stimuli over different ranges of $F_{out}$ will reveal any excessive non-linearity in the FP blocks.

A further important point to note from table 2 is that excessive CP mismatches or Loop filter leakage will lead to "close in" phase noise or jitter on the VCO output when the PLL is in lock [11][13]. Note that, for embedded CP-PLLs the LF storage component is usually constructed using large MOS capacitors with the gate oxide (GO) as the dielectric. Spot defects causing GO faults can be common [14], and will lead to "leaky" LF components, this in turn will contribute to short term fluctuations of the LF voltage, that will in turn contribute to jitter of the PLL output. Therefore it is proposed that the basic tests are carried out before any more elaborate jitter measurement techniques are applied. A recent paper concerning investigation of PLL noise sources [15] identifies power supply coupling mechanisms as a major contributory factor to PLL VCO jitter. Further useful material concerning jitter measurement is given in [16]. Correlation of phase noise and jitter to FP non-idealities and power supply coupling is being carried out as further work.

A sketch of the typical output response for the sequences of table 1 is provided below in figure 6.




F# = Measured frequencies after each test step.
ΔM# = Allowable tolerances on each measurement.
Nclk = Number of clock cycles that are derived from EXTREF. Each test step is run for an equal number of cycles.

**Figure 6 expected outputs for Ramp based tests.**

To further illustrate the test concept, the output voltage at the loop filter node for a CP-PLL with the following component values and test settings is shown in figure 7.

| Ichp | KPD | Rp | Cp | Kvco |
|---|---|---|---|---|
| 1mA | $159uAr^{-1}$ | 680 | 470nF | $2\times10^{6}r\ s^{-1}\ v^{-1}$ |
| **Extref** | **Textref** | **Ncycles** | **ΔTn(Ichp)** | **Fstart** |
| 100KHz | 10us | 20 | 100us | 3MHz |

**Table 3 Test and simulation parameters.**

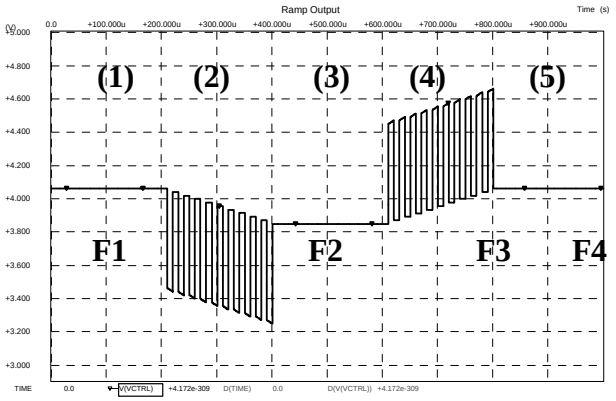



**Figure 7 Output waveforms from PLL LF node (cf figures 1 and 3).**

Comparisons between the predicted output frequency shift and the measured output frequency shift (F1-F2) are given below.

| IP=1mA | | |
|---|---|---|
| **Value** | **Measured** | **Calculated** |
| ΔVc | -212.658mV | -212.8mV |
| $\Delta F_{out}$ | 68.02KHz | 68KHz |
| **IP=1.2mA** | | |
| ΔVc | -255.316mV | -255.319 |
| $\Delta F_{out}$ | 84.6391KHz | 81.2705KHz |

**Table 4 Comparison of results**

(Measurement results have been taken from M/S simulations and correlate well with measurements carried out upon actual hardware.)

Further basic tests have been carried out on actual hardware to provide an indication of the link of jitter to leakage of the loop filter node. The PLL used for the test was a 74HCT9046A PLL and the component values used are the same as for table 3. Note however, for this circuit the nominal output frequency was 2.5MHz. Leakage of the loop filter node was emulated by placing various resistors in parallel with Cp. Measured results are provided in table 5 (cf fig 8).

| Res Value (ohm) | V max | V min | Fmax MHz | Fmin MHz | Jitter Pk-Pk (ns) |
|---|---|---|---|---|---|
| None | 2.488 | 2.238 | 2.4038 | 2.3041 | 1 |
| 1M | 2.063 | 1.813 | 2.2124 | 2.1088 | 4.5 |
| 680K | 1.919 | 1.706 | 2.1368 | 2.0833 | 5.2 |
| 100K | 1.556 | 0.9831 | 1.8116 | 1.7301 | 8 |

**Table 5 Jitter and loop filter leakage**

The average output frequency of the PLL was measured to be 2.5 MHz for each case, which indicates that these effects will not be uncovered by a simple FLT. Further tests were made with a 10Kohm and 1Kohm resistor. For these cases jitter was measured as 28ns and 158ns respectively, however in the latter case the average output frequency was measured to be 1.7MHz. Estimates of the jitter were made using a Tektronix 11402 oscilloscope. Plots of the loop filter voltage were taken from an Agilent 54622D oscilloscope and are shown below.

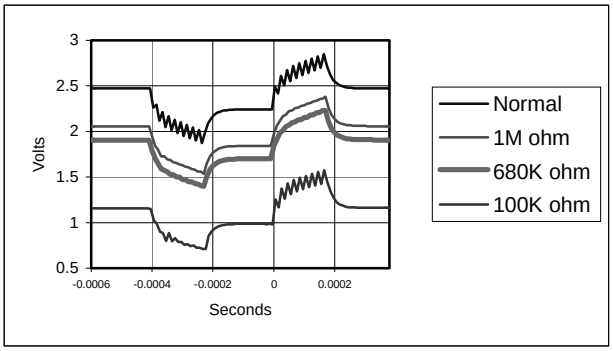



**Figure 8 Loop filter output voltage versus leakage resistance.**

(Note that the order of the above outputs corresponds with the order of the resistance values used i.e. the normal (no resistance) plot is the top output graph)

In the currently developed hardware, to realise a full BIST solution, limit values are stored on chip and compared against the output results using a magnitude comparator. Results can be provided as a pass / fail flag; however an option will also be included to allow extraction of actual measured values.

At present for the applied tests the gate count is less than a thousand.

## 4. Application for functional verification of multiple charge pump current and loop filter component settings.

Numerous PLL applications require that analogue components in the PLL can be altered. Other published methodologies only concentrate on measurement of a fixed PLL. Modification of components is generally required to facilitate alteration of the loop dynamics, so that the PLL can function over wide operational ranges. Common modifications to the simple architecture of fig 1 include provision to allow multiple CP current settings and loop filter settings to be used for the PLL.

Both of the above methods are used in embedded PLLs and board level synthesiser chipsets.

If applications require that adjustable components are to be alterable during the operational lifetime of the PLL it is mandatory to verify all used settings. Unfortunately, full operational verification for multiple loop filter and CP settings is time prohibitive, and can be difficult to realise when considering embedded PLL test. Even in the case of PLL chipset test, where direct access to the important PLL nodes is permitted, direct measurement of parameters such as multiple CP currents can be time consuming.

The sequences proposed in section 3 can be used to provide a relative test to allow verification of multiple charge pump current or loop filter component settings. The basic principle of the test considering the case of multiple CP currents is outlined below.

1) Initially $F_{out}$ of the PLL is set to provide a reference frequency. Setting of the datum frequency can be achieved by relocking the PLL after the ramp tests have been applied.
2) The stimuli of section 2 are applied for N cycles of PLLREF with the largest CP current (*Ichref*) setting activated.
3) At the end of N cycles place the PLL in hold mode and measure $F_{out}$. Note N remains the same for all tests.
4) Repeat steps 1 to 3 for all other smaller magnitude CP Currents (*Ichn*).

From the results of the above test it is easy to show using equation (4) that

$$\frac{\Delta Fn}{\Delta Fref} \cdot Ichref \approx Ichn \quad (6)$$

and

$$\frac{\Delta Fn}{\Delta Fref} \approx \frac{Ichn}{Ichref} \quad (7)$$

(Where: ΔFn is the frequency change corresponding to the associated CP current setting, and ΔFref is the frequency change corresponding to the main CP current.)
Therefore with knowledge of *Ichref* all other CP currents can be deduced. Also, even if direct measurement of *Ichref* is impractical an estimate of matching between currents can be obtained. This type of test can also be carried out for multiple loop filter settings. To illustrate the concept further a CP-PLL circuit with: Rp = 680ohms, Cp = 470nF, and KVCO = 2Mrad/s was simulated.
The simulated results for CP currents of 1 to 5ma with input stimuli applied for 20 cycles of PLLREF are given in figure 9.

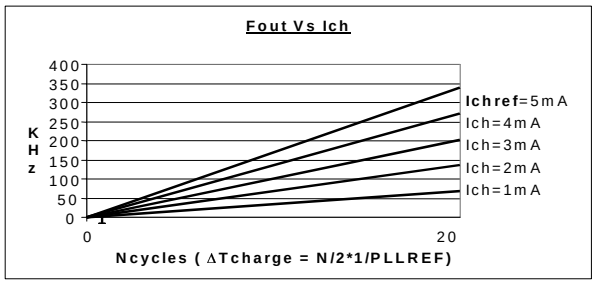



**Figure 9 Change in OP Freq Vs CPCurrent**

Comparisons of the outputs of the tests are provided in the following table.

| Ichn | ΔFn KHz | ΔFn/ΔFref | ΔFn/ΔFref*Ichref |
|---|---|---|---|
| 5mA* | 339* | 1 | 5mA |
| 4mA | 270 | 0.8 | 4mA |
| 3mA | 203 | 0.6 | 3mA |
| 2mA | 136 | 0.4 | 2mA |
| 1mA | 68 | 0.2 | 1mA |

**Table 6 Illustrating method of multi CP match estimation**

(In the above table all values are rounded to 1d.p.
* Indicates the datum measurement.)

For the relative tests described in this section the following constraint applies:
The VCO control voltage must be relatively linear over the measurement range.
Even in the worst case, that is, when no direct measurement of a reference charge pump current is possible, the tests will still produce an accurate measurement of relative matching between the CP currents. Furthermore the test will provide direct indication of basic functionality of the component switching circuitry. For a full BIST solution the test response outputs can be evaluated on chip against a stored set of calculated limit values.

## 5. Conclusions and further work.

This paper has presented promising techniques for the test of embedded CP-PLLs that can reveal valuable information about the forward path PLL Blocks. In addition, ideas have been presented that allow functional relative tests to be carried out for multiple PLL settings, which does not seem to have been covered in other test approaches. All test vectors have been evaluated through simulations and hardware prototyping techniques. Further work will focus primarily upon investigation of alternative vector sequences for the test, to allow extraction of more operational details. In addition, some work will be carried out into accurate correlations of phase noise / jitter to forward path block operation and adaptation of the proposed tests to allow coarse jitter estimation.

## Acknowledgement

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## References

[1] Dalmia M, Ivanov A, Tabatabaei S, "Power Supply Current Monitoring Techniques for Testing PLL's", Proc ATS 97, pp 366-71.

[2] F Azais, M Renovell, Y Bertrand, Ivanov A, Tabatabaei S, "A Unified Digital Test Technique for PLL's; Catastropic Faults Covered" Proc 5th IMSTW.

[3] M. Burbidge, A Richardson, A Lechner, "Test Techniques for Embedded Charge Pump PLL's; Problems, Current BIST Techniques, and Alternative Suggestions.

[4] S. Sunter, A Roy, "BIST for Phased locked loops in digital applications", IEEE ITC99, pp532-540.

[5] G W Roberts, M Hafed N Abraskharoun, "A Stand Alone Integrated Test Core For Time And Frequency Based Measurements", Proc. Int. Test Conf, 2000, pp 1031-1041

[6] A DeHon, "In-System Timing Extraction and Control Through Scan-Based, Test-Access Ports", M.I.T Transit Project, Transit Note #102, 1994

[7] A Chan, G W Roberts " A Synthesizeable, Fast And High-Resolution Timing Measurement Device Using A Component-Invariant Vernier Delay Line", ITC01proc, pp858-867

[8] Fluence, "VCOBIST", IEEE DAC 99.

[9] S. Kim, M Soma, “An Effective Defect-Oriented BIST Architecture for High Speed Phase Locked Loops”, IEEE VLSI Test Symposium 2000, pp231-236.

[10] F M Gardner, “Charge-Pump Phase-Lock Loops”, IEEE Trans Comm, 28th Nov 1980, pp 1849-1858.

[11] B Razavi (Editor), “Monolithic Phase-Locked Loops and Clock Recovery Circuits; Theory and Design”, IEEE Press 1996, ISBN 0780311493.

[12] R Best, “Phase Locked Loops, Design Simulation and Applications”, 4th Edition, Mc-Graw-Hill, ISBN 0071349030

[13] D Banerjee, “PLL Performance Simulation and Design” Copyright 1998 National Semiconductors.

[14] M Sachdev, “ Defect Oriented Testing for CMOS Analog and Digital Circuits”, Kluwer Academic Publishers, 1998, pp 37-38 and 79-81, ISBN 0-7923-8083-5.

[15] P Larson, “Measurements and Analysis of PLL Jitter Caused by Digital Switching Noise”, IEEE Journal of Solid-State Circuits, July 2001, pp1113-1120.

[16] K. Jenkins, J Eckhardt, “Measuring Jitter and Phase Error in Microprocessor Phase-Locked Loops, IEEE Design and Test of Computers, Apr-Jun 2000, Issue 17, Vol 2, pp 86-93

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