A Current-Source Modular Converter for Large-Scale Photovoltaic Systems.

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A thesis submitted for the degree of

Doctor of Philosophy

July, 2023

Declaration

I, Saud Alotaibi, confirm that the presented research in this thesis is my own and was written and originated entirely by me. It has not been submitted previously to any other university or similar institution that led to the award of a degree. The research was conducted at the University of Lancaster, United Kingdom (UK), between January 2019 and February 2023.

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Abstract

The world is shifting toward renewable energy sources (RESs) to generate clean energy and mitigate the stress of global warming caused by CO_2 emissions in recent decades. Among several RES types, large-scale photovoltaic (LSPV) plants are a promising source for meeting ambitious clean energy targets and being part of power generation. With the progress of high-power modular inverters, new opportunities have arisen to integrate them into LSPV systems connected to medium-voltage (MV) grids to obtain high efficiency and reliability, better system flexibility, and improved electrical safety compared with string or central inverters.

This thesis presents and implements a new current source three-phase modular inverter (TPMI) based on a novel dual-isolated SEPIC/CUK (DISC) converter. The TPMI is designed with a single power processing stage comprised of series-connected DISC submodules (SMs) to deliver MV into the utility grid. It outperforms conventional high-power inverters in terms of modularity, scalability, galvanic isolation compliance, and distributed maximum power point tracking (MPPT) capabilities.

The DISC converter employed as an SM in the proposed TPMI generates bipolar output (i.e., both positive and negative voltages). In addition to having step-up and step-down capabilities with a continuous input current, this converter shares

an input side inductor, thereby reducing the number of components. The DISC structure, modulation method, operation, novel state-space model, and parameter design procedure are analysed in details. Then, simulation results are presented to validate the theoretical and analytical analyses of the DISC converter.

The proposed TPMI inverter is subsequently integrated into the LSPV grid connection to prove its suitability for such applications. In the theoretical analysis, the advantages of TPMI structure over conventional topologies are discussed. Then, the modulation technique, and operational concept are presented, followed by a dedicated control strategy is implemented by adding a system and SM-level controllers. The system controller is required for the generation of uniform duty ratios for all SMs in order to regulate the power transfer. The SM level controller is introduced to ensure equal current and voltage distribution between SMs and to compensate for minor discrepancies between the various parameters. The entire TPMI system is demonstrated through MATLAB and Simulink simulations, with the objective being to deliver the rated (1 MW) power from the PV modules under normal operation, uniform shading, and partial shading conditions and to match PV generation with the grid's power demands. A downscaled 3-kW TPMI inverter was developed in the laboratory to validate its feasibility experimentally with its control strategy in different operating conditions. Finally, the TPMI performance is compared with selected current source inverter topologies, which shows that TPMI obtains good efficiency within the context of existing state-of-the-art current source converters.

Then, the TPMI structure is modified by redesigning its DISC SMs, which provides several benefits, including a reduction in the number of switch devices operating at high frequency, thus decreasing switching losses, and an increase in efficiency. In

this study, a half-cycle modulation (HCM) scheme is developed for the switches, and the operation of a modified DISC SM is analysed. Simulation and experimental results validate the performance of the modified TPMI topology and demonstrate its suitability for LSPV applications. According to the results of the comparison, the maximum power efficiency of the modified TPMI structure is 95.5%, which represents an improvement over the original TPMI structure.

Publications

These are the key contributions of this Ph.D. thesis, and are divided into journal and conference papers. Some contributions to this study can deviate slightly from the main subject matter, but they add to and strengthen the knowledge gained throughout the Ph.D. process. The four journal papers are the main part of this Ph.D. thesis and address several aspects of a state-of-the-art modular multilevel inverter, a novel structure of a three-phase modular inverter (TPMI) based on a dual isolated sepic/cuk (DISC) converter, and the characteristics of the proposed inverter's operation, modeling, and control. The following chapters introduce the analysis and outcomes, which are described in further detail in each part. Additionally, some conference papers have been published to present partial results on the proposed inverter for PV energy systems.

Journal Papers

1. **Saud Alotaibi**, Ahmed Darwish, B. W. Williams. "Three-phase inverter based on isolated SEPIC/CUK converters for large-scale PV applications". In: *International Journal of Electrical Power & Energy Systems*, vol. 146, p. 108 723, 2023

2. **Saud Alotaibi**, Xiandong Ma, and Ahmed Darwish. "Dual Isolated Multilevel Modular Inverter with Novel Switching and Voltage Stress Suppression". In: *Energies 15.14 (2022)*, p. 5025

3. **Saud Alotaibi** and Ahmed Darwish. "Modular multilevel converters for large-scale grid-connected photovoltaic systems: A review". In: *Energies 14.19*

(2021), p. 6213

4. Ahmed Darwish, **Saud Alotaibi**, and Mohamed A Elgenedy. "Current-source single-phase module integrated inverters for PV grid-connected applications". In: *IEEE Access 8 (2020)*, pp. 53082–53096

Conference papers

1. **Saud Alotaibi**, Ahmed Darwish, Xiandong Ma, B. W. Williams. "A New Four-Quadrant Inverter Based on Dual-Winding Isolated Cuk Converters for Railway and Renewable Energy Applications". In:*The 10th International Conference on Power Electronics, Machines and Drives(PEMD 2020)*. Vol. 2020. IET. 2020, pp. 926–931

2. **Saud Alotaibi**, Ahmed Darwish, Xiandong Ma, B. W. Williams. "A new modular three-phase inverter based on sepic-cuk combination converter for photovoltaic applications". In: *The 9th Renewable Power Generation Conference (RPG Dublin Online 2021)*. Vol. 2021. IET.2021, pp. 259–264

3. Ahmed Darwish, **Saud Alotaibi**, and Mohamed A Elgenedy. "Tri-State Cuk Inverter with Power Decoupling for Photovoltaic Applications". In: *The 9th Renewable Power Generation Conference (RPG Dublin Online 2021)*. Vol. 2021. IET. 2021, pp. 198–203

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My sponsors deserve much of the credit as well. Your support made it possible for me to spend time in Lancaster, which has been a life-changing experience. This Ph.D. work would not have been done without the support of the Saudi Arabia Cultural Bureau and Shaqra University.

I want to convey my appreciation to my parents, Hameed Al-thiabi and Sheikha Al-thiabi, and my siblings for their unwavering belief in me. I cannot adequately

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Contents

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Nomenclature

$2L - VSI$	Two level voltage source inverter
AC	Alternating Current
$C5$	Cuk converter
C_c	Cuk capacitor
C_n	Negative output capacitor
C_p	Positive output capacitor
C_r	Primary capacitor
C_s	SEPIC capacitor
$CF - DAB$	Current-fed dual active bridge converter
CHB	Cascaded H-Bridge
CM	Common-mode
CMS	Continuous modulation scheme
$CO2$	Carbon dioxide

CSC	Current-source converter
D	Duty cycle
DAB	Dual active bridge converter
DC	Direct Current
$DERs$	Distributed energy resources
$DISC$	Dual isolated SEPIC/CUK
DMS	Discontinuous modulation scheme
DSP	Digital signal processor
EMI	Electromagnetic interference
ESR	Equivalent series resistance
$F-DAB$	Forward dual-active bridge converter
f_o	Grid frequency
f_s	Switching frequency
FB	Full-bridge
FC	Flying capacitor
$G5$	SEPIC converter
GW	Gigawatts
HB	Half-bridge

HCM	Half cycle modulation
$HFTs$	High-frequency transformers
$HVDC$	High-voltage direct current
$IGBTs$	Insulated gate bipolar transistors
kWh	Kilowatt hour
L_1	First output inductor
L_2	Second output inductor
L_n	Input Inductor
LFT	Low-frequency transformer
$LSPV$	Large-scale photovoltaic
$MLCs$	Multilevel Converters
MMC	Modular Multilevel converters
MPP	Maximum power point
$MPPT$	Maximum power point tracking
MV	Medium-voltage
MW	Megawatts
N	Transformer turns ratio
n	Number of submodules

NPC	Neutral point clamped
PR	Proportional-resonant
PV	Photovoltaic
PWM	Pulse-width modulation
$RESs$	Renewable energy sources
S_{o1}	First output switch
S_{o2}	Second output switch
SAB	Single active bridge
SiC	Silicon carbide
SMs	Submodules
t_s	Switching time
THD	Total harmonic distortion
$TPMI$	Three-phase modular inverter
TWH	Tera Watt Hour
UN	United Nations
VSM	Virtual submodule
ZVS	Zero voltage switching

Chapter 1

Introduction

1.1 Overview

The economic and social progress of modern society's growth is directly tied to the availability of energy sources. Over 770 million people worldwide live in rural areas without access to electricity, along with some countries and parts of the world suffer from acute power shortages [1]. Historical and current energy generation sources are dominated by fossil fuels such as coal, oil, and gas, as well as nuclear power as shown in Fig 1.1 [2]. However, academics, scientists, and engineers worldwide consider them environmentally damaging due to their impact on climate change and global warming. According to United Nations (UN) studies, if emissions continue at their current rate, the average global temperature will increase by $5.8°C$ by the end of the next century [3]. Furthermore, the vulnerability of fossil fuel prices, combined with the uncertain future of crude oil, has influenced the policies adopted by various countries, resulting in a greater emphasis on green technologies to meet their energy demands. Furthermore, nuclear energy is dangerous and requires an extremely high level of protection [4].

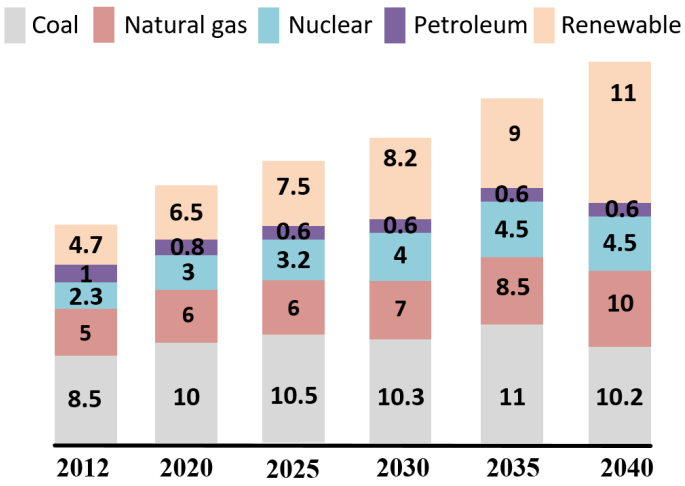


Figure 1.1: Net global electricity generation (TWH) and its forecast through 2040 [2].

This significant challenge reflects the world's noticeable shift away from this form of energy towards risk-free alternatives [5]. Despite the aforementioned energy sources have been in use for a long time, their previously negative impacts demand a large and coordinated shift to a more promising alternative. Consequently, many governments are pursuing renewable energy sources (RESs) and encouraging zero- or low-carbon technologies [6].

Several countries have taken the lead in transitioning their energy systems to becoming carbon-neutral. This transition is mainly driven by government regulation and incentives, as well as industrial developments in areas such as communications, manufacturing, automation, and power electronics. In this era of energy transition, economic and social progress have allowed the development of sustainable energy sources that are extremely reliable and efficient, as well as being capable of supplying energy at a range of power levels. RESs are considered as superior alternative energy sources and a possible solution to the finite supply of fossil fuels and their environmental impact [7].

As seen by the historical trends in Fig 1.2, progress in clean energy has been continually improving. The global renewable energy community projects that they will be able to provide at least 26% of worldwide electricity generation by 2020, which is up from 8% in 2019 [8]. The remarkable pace of the RESs capacity expansions is likely to continue, with 270 gigawatts (GW) expected to become operational in 2021 and 280 GW in 2022. Among all RESs, solar and wind energy are the top and are the most rapidly developing renewable energy sources [9]. Therefore, these two forms of RESs are predicted to have a significant impact on the supply side of distribution networks in the future.

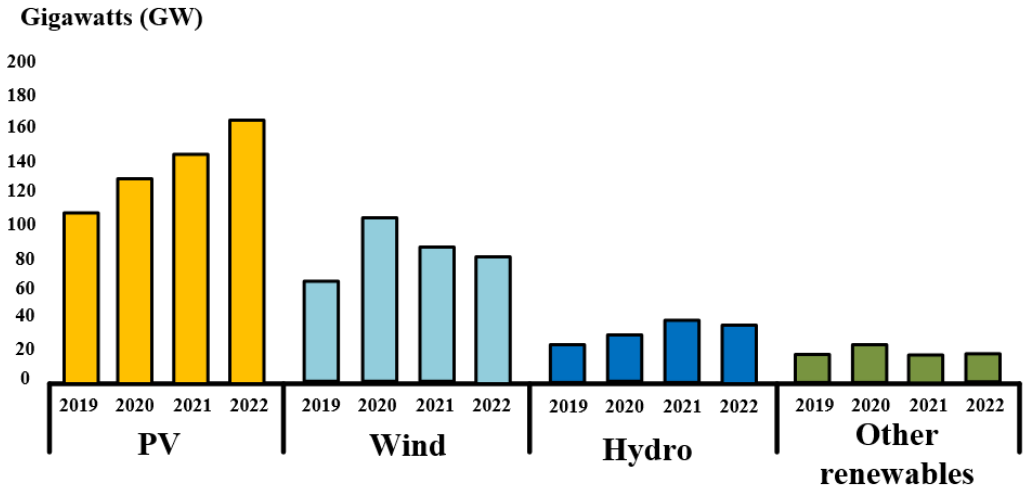


Figure 1.2: Global renewable energy capacity [8].

Solar photovoltaic (PV) energy generation systems are becoming a significant part of expansion plans for distributed energy resources (DERs) due to their (a) environmentally friendly and pollutant-free technology; (b) high rate of return on investment; and (c) widespread availability. Global PV expansion is expected to accelerate as power electronics technologies improve and the cost of PV modules decreases, making PV systems an attractive option for a low-cost energy source that

can be developed and put into operation in less than a year [10]. The cost of PV energy is forecasted to continue to fall because of increased economies of scale and additional technological improvements in the industry. According to [11], the levelized cost of electricity (LCOE) in PV energy decreased by 77% between 2010 and 2018, from 0.37 USD per kWh to 0.085 USD per kWh, and the average declining energy price is predicted to be 0.02 USD per kWh by 2030 and 0.05 USD per kWh by 2050.

Fig 1.3 and Fig 1.4, show the global installed electricity capacity from 2010 to 2018, and its predicted capacity for 30 years. Globally, 40 GW of capacity was installed in 2010 at a rate of 17 GW per year. Similarly, global capacity installed in 2018 totalled 480 GW, with a 94 GW annual deployment [12].

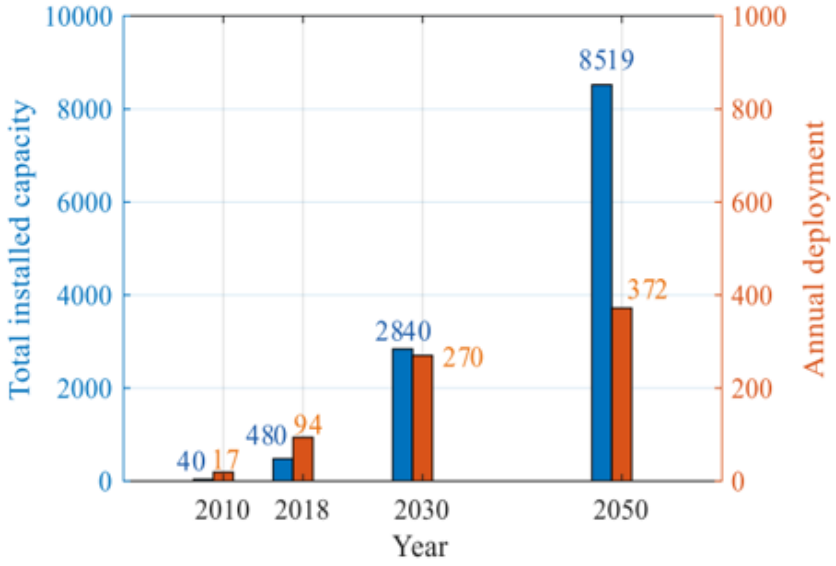


Figure 1.3: Photovoltaic capacity and deployment per GW [12].

The continents of Asia, Europe, and North America are still in the top three in terms of the amount of solar power generated [13]. As of 2030, Asia is predicted to maintain its dominance in the worldwide market with an installed capacity of 1860

GW, while North America will come in second with an installed capacity of 437 GW. By 2050, the installed capacity will continue to expand, and Asia continues to lead the global market with a total capacity of 4.837 GW. North America, with 1.728 GW, is predicted to be the second-largest PV market, followed by Europe, with 891 GW [13].

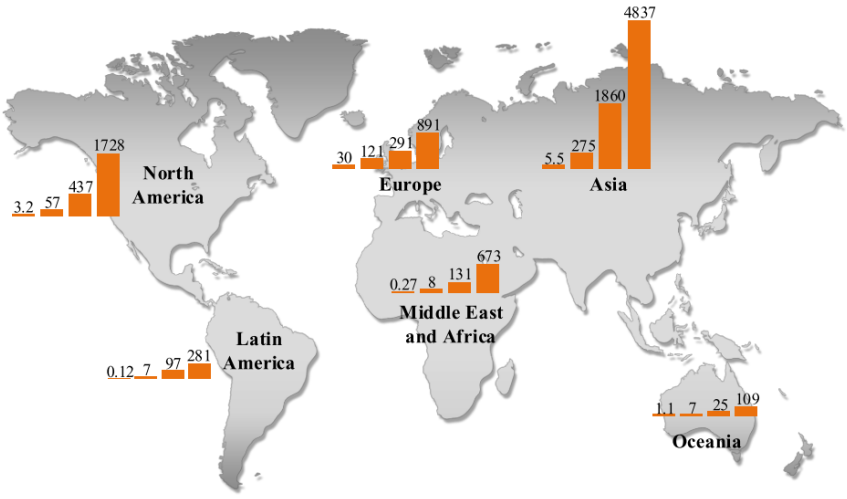


Figure 1.4: Each continent's photovoltaic capacity [13].

The considerable disparity between continents is largely explained by investment levels. Asia is predicted to invest 113 billion dollars per year until 2050, followed by North America at 37 billion dollars per year and Europe at 19 billion dollars per year [13]. According to the policies and investments of many nations, the majority of the increased power is generated through large-scale PV (LSPV) plants with output power over 1 MW [14]. The size and number of completed LSPV plant projects in 2018 totaled approximately 235, all of which had power levels of at least 50 megawatts (MW) and were situated in at least 37 countries[15].

The industry needs to be ready for such a significant increase in available power

over the next 30 years. Therefore, new and improved technologies are expected to be developed to better integrate PV power generation into the grid. These new developments are aimed at opening up new markets for the usage of this energy source, as well as producing more efficient PV panel technologies, more adaptable power systems, and novel power converter topologies for handling a high-density of power. This thesis investigates modular inverter structures for use in LSPV applications, with a focus on developing new topologies for power converters that can accommodate higher levels of power generation in the future.

1.2 Configurations of PV systems

Different designs and configurations have been employed to integrate PV systems into the grid [16]. Fig 1.5 shows the most common configurations: central, string, multi-string, and AC modules. Selecting one configuration over another depends on several aspects, such as power output, location, cost, and availability, which are all summarised in [17], [18].

1.2.1 Central Configuration

A central inverter configuration is composed of a central DC/AC converter connected to many PV modules in a series to form a string. The disposition of PV strings is connected in series to deliver a proper level of DC voltage on the DC side. A typical central structure is that of a single-stage energy conversion process, which reduces expenses and improves the efficiency of energy conversion. In the case of LSPV power plants, a number of central inverters are implemented in parallel to a low-frequency

transformer (LFT) that is used to step up the low voltage level (540-690 V) to the medium voltage grid level (20-30 kV)[19].

1.2.2 String Configuration

A string inverter configuration is a simplified form of the central inverters, where each individual PV string and inverter are placed as a single-phase connection. This configuration allows each string its own maximum power point tracking (MPPT) controller. This flexibility provides better MPPT performance and increases the total power generation in uneven conditions compared to the central configuration. Power converters with galvanic isolation and two conversion stages can be used to eliminate leakage currents and prevent voltage levels from exceeding the limit allowed in the PV modules. Usually, DC-DC converters equipped with high-frequency transformers (HFTs) or DC-AC converters equipped with LFTs can be employed [20].

1.2.3 Multi-string Configuration

This is an advanced string inverter configuration that allows the use of multiple strings and DC/DC converters connected to a central inverter. In this context, it allows the orientation of the maximum power point (MPP) to be set for the individual PV string which is different from the configurations of central and string, where all strings have the same orientation [18]. In comparison to the previous configurations, this one allows for independent MPPT operation, which results in maximum power harvesting from the PV source and thus increases total efficiency [20].

1.2.4 AC-module Configuration

The AC module integrated inverter system shown in Fig 1.5(d) is comprised of a single solar PV module, and its individual inverter is connected to the utility grid. In this way, an inverter with its own MPPT controller allows for the elimination of the DC bus and the reduction of configuration costs, allowing for more scalability and flexibility [21]. However, the main challenge is designing an inverter capable of boosting the PV module's low voltage to a level compatible with the utility grid voltage [22].

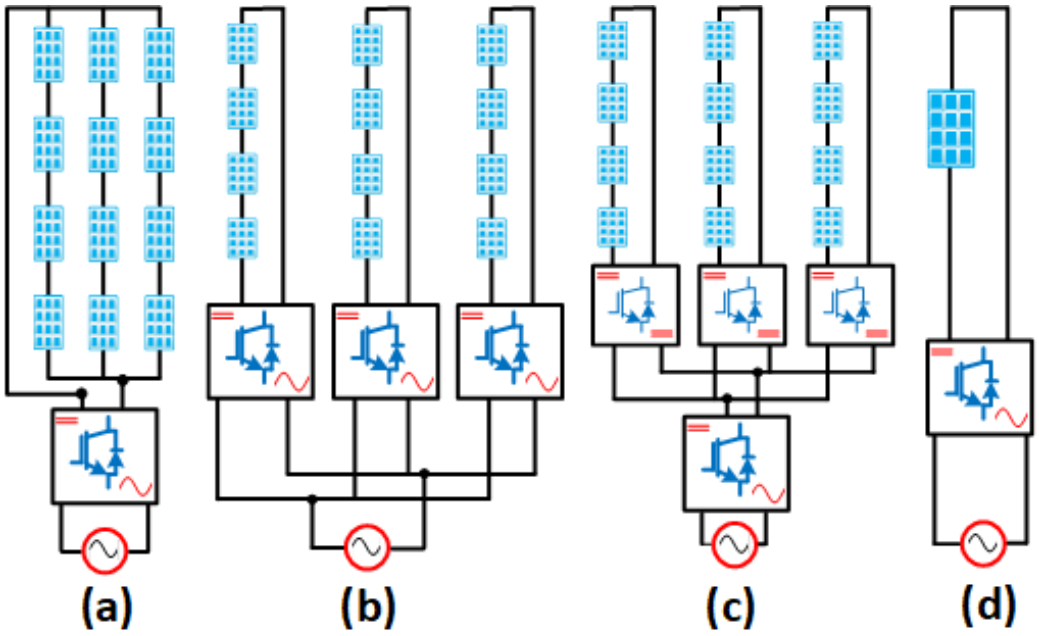


Figure 1.5: LSPV configurations (a) Central, (b) String, (c) Multi string, (d) AC module.

1.2.5 Comparative analysis of PV configurations

According to the analysis in [16], [22], the four configurations are evaluated in terms of operation factors such as performance, power losses, and cost, as shown in Table 1.1.

General categories	features	Central	String	Multi-string	AC module
Performance	Robustness	High	Low	Medium	Very-Low
	Availability	Low	High	Medium	Very-High
	Flexibility	low	High	Medium	Very-High
	MPPT efficiency	Low	High	Medium	Very-High
Power losses	Mismatching	High	Low	Low	Very-Low
	Switching	High	Low	Medium	Very-Low
	Dc side	High	Low	Medium	Very-Low
	Ac side	Low	Medium	Medium	High
Cost	Installation	Medium	High	Medium	Very-High
	Maintenance	Low	Low	High	Very-High

Table 1.1: Comparative aspects of LSPV configurations.

The first category of performance assesses robustness, availability, flexibility, and MPPT efficiency. It is seen that the central configuration is the most robust in comparison to other configurations. A single central inverter is responsible for managing the energy generated by hundreds of PV modules at the same time. However, the central structure is harmed by the PV module's partial shading conditions, which can disturb the MPPT control and reduce the total DC voltage, reducing availability, flexibility, and MPPT efficiency significantly. On the other hand, string and AC model configurations perform well for all general characteristics, but their robustness is limited [23].

In relation to the power loss category, power mismatches have a detrimental effect on central configurations. These losses are unavoidable in any PV module group

because of their condition-dependent nature (e.g. partially shaded, degradation of PV string, cloud coverage, dust, cooling). Furthermore, it is important to consider switching losses, which can vary depending on the devices and the control of the PV inverter. Switching losses are also significant in central inverters due to the PV modules sharing the same dc current, complicating the MPPT operational controller [20].

In addition, the DC or AC side losses associated with the length of cables are a concern for LSPV power plant losses. Initially, DC losses in central inverters are quite high because of the parallel connection of several PV strings to the same DC bus. In contrast, it has low ac losses since the LFT is located quite close to its inverter. On the other hand, string and multi-string topologies offer lower DC losses than central inverters because they can scale up dc voltages via a DC-DC stage with galvanic isolation. However, extra electronic components are necessary to accomplish this task. In the case of the AC module configuration, the performance is superior to other configurations, with the exception that the losses are fairly high on the AC loss scale [16].

The final category takes into account the cost of installation and maintenance. In comparison to other configurations, a central configuration is by far the cheapest system. This feature makes the central topology an attractive option for LSPV projects. In other configurations, as the number of inverters increases, installation and maintenance costs become too high [22].

To summarise, the central configuration has the following characteristics: high robustness; low flexibility; significant losses due to power mismatches and DC cables; low ac side losses; and cheap installation and maintenance costs. Alternatively, string

and multi-string configurations offer excellent flexibility and availability, with minimal DC side losses and high installation and maintenance cost as the power levels increase. AC module configuration performs well in terms of flexibility, simplicity, and MPPT efficiency. However, the major drawbacks of the ac module arrangement are its capability to deliver the grid power level, high cost, and the possibility of a decrease in power density.

In this context, a possible research field is a modular current source inverter, where the structure is a promising research topic for improving PV yield and power conversion efficiency of grid-connected PV systems.

1.3 Challenges of PV systems

1.3.1 Availability and Lifetime

There is a significant difference between the normal inverter lifespan (5 to 15 years) and the lifetime of PV modules (around 25 years). Inverters are widely viewed as the weakest component of PV systems in terms of operation and maintenance [24]. According to [25], inverters were responsible for 37% of unplanned maintenance and 59% of the total cost of repairs in a 50-megawatt (MW) PV plant. These failures are to blame for the high costs, which include not only service costs but also energy losses caused by the PV power plant's downtime [26].

However, DC-link capacitors (usually electrolytic types) are considered a fundamental cause of the limited lifetime of commercial PV inverters [27]. Presently, most high-power PV converters require sizeable electrolytic capacitors to handle low-frequency ripples and meet power quality standards. Even though electrolytic

capacitors have a high capacitance density, they are considered very unreliable parts [28]. Furthermore, electrolytic capacitors are 30 times less reliable than non-electrolytic capacitors in the same operational conditions [29]. Moreover, high solar power variability and operation at high-temperature ranges impair electrolytic capacitors' lifetime due to their considerable equivalent series resistance (ESR) and low breakdown voltage [30]. Consequently, the typical lifespan of a conventional PV system is less than ten years.

Eliminating electrolytic capacitors from the design of PV systems and replacing them with capacitors with long lifetimes can be an effective approach to improving the lifetime of the PV system [31]. Continuous input current source converters have been widely researched as possible topologies for using long-lifetime capacitors such as film capacitors to obtain high-reliability PV systems with non-electrolytic capacitors [32]–[34].

1.3.2 Limitations of Voltage Source Inverters

A two-level voltage source inverter, commonly referred to as a 2L-VSI, is a typical structure for connecting PV systems to the grid. This topology is used due to its low cost and simplicity [35]. Nevertheless, the output voltage of 2L-VSI is always switching between the maximum and minimum DC voltage levels, resulting in a high dv/dt and a significant degree of electromagnetic interference (EMI), particularly at high switching frequencies. Because input and output currents are discontinuous, considerable filtering devices are required to reduce current ripples and EMI [36]. In addition, there are extra costs and also weight connected with the higher volume and weight of the 2L-VSI topology due to its voltage buck nature, which requires a boost

dc-dc converter to match the PV voltage and track (MPP) [37].

The restricted voltage rating of commercially available semiconductor devices is an additional disadvantage of the 2L-VSI topology [38].The voltage rating of commercially available insulated gate bipolar transistors (IGBTs) is approximately 6.5 kV. Moreover, these devices should be de-rated by a factor of 0.5 to account for the device's commutation voltage and to improve the reliability of 100 failures in time (Vcom@100FIT) which means that the 2L-VSI voltage is restricted to 3.25 kV [39]. A series connection of IGBTs can also provide difficulties due to mismatches in the characteristics of the IGBT devices and the gate-driver circuits, requiring the installation of snubber circuits, and complicating the 2L-VSI's operation and its control [40].

The limitations of 2L-VSI prompted academia and industry to explore alternative techniques, such as a new power electronic technology based on Multilevel Converters (MLCs) for high-power applications. The key features of these topologies are modularity, scalability, redundancy and high power density operations that can allow integration into the grid without (LFT), and a better power quality [41].

1.3.3 Leakage Current in PV systems

Grid-connected PV systems require extra care to comply with grid codes. Accordingly, international authorities have established several widely acknowledged standards for PV systems, which are necessary to avoid safety concerns [42]. The main source of these safety problems and concerns is the existence of capacitance C_{PV} between the PV cells/module and the grounded frame, as shown in Fig 1.6. As can be seen, a direct ground (earth) current path from the PV module to the power grid is formed

due to lack of galvanic isolation [43].

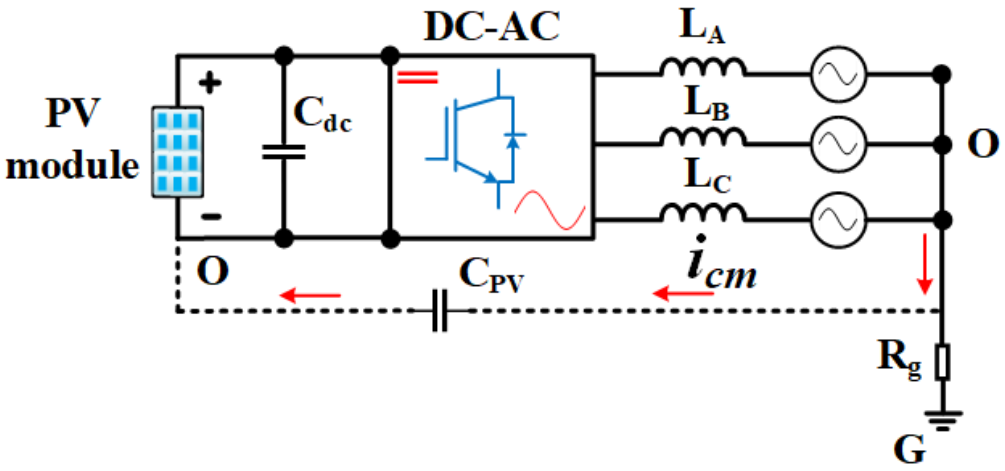


Figure 1.6: Three-phase grid-connected PV inverter [42]

The resonant circuit, which is comprised of the massive stray capacitance C_{PV} in this path (also referred to as the ground capacitor) and the inverter's output L-filter on the grid side, can be excited by a variable common-mode (CM) voltage, resulting in the flow of a high-amplitude capacitive CM current (i.e., leakage current i_{cm}). This current has both low-frequency and high-frequency switching and line components. In this case, harmonics are introduced into the grid, degrading system efficiency, undermining electromagnetic uniformity, and posing potential protection and safety hazards (electric shock) [44].

In addition, the size (or even weight) of the PV array, the DC lines connecting the array to the DC-AC power inverter, and environmental factors all play a role in determining the amplitude of the leakage current. These aspects make it far more difficult to completely eliminate leakage currents in practice than was previously assumed [45].

The solution explored in this thesis uses an isolated inverter based on small-size

high-frequency transformers (HFTs). The HFTs are considered a mandatory part of the proposed inverter and a viable alternative to low-frequency transformers, as they provide galvanic isolation, a smaller footprint, and increased voltage gain. Therefore, HFTs are increasing system reliability and improving human safety in the PV field.

1.4 Research Motivation

With present global energy demands and industrial consumption patterns, everyday increases in electricity generation are required. RESs such as wind and solar, which are anticipated to continue expanding their capacity, account for a sizeable share of the world's electricity generation. In addition, LSPV energy is gaining significant market share and will likely be widely deployed in the future due to developments in technology, cost reduction, and high reliability.

Due to the significant growth in global LSPV power generation, there is the potential for a variety of concerns and challenges in this field that will need to be addressed to improve energy yield. These challenges include; increasing the output per square foot of PV modules; ensuring constant power generation to meet demand at all times; simulating inertia to mitigate the effects of the absence of synchronous generators; and designing a new configuration of power converters capable of managing high densities of power generation.

A conventional LSPV power plant is mainly composed of PV modules that are connected in series/parallel combinations to form PV arrays and strings, as shown in Fig 1.7. These arrays and strings are then connected to dc-dc converters that ensure MPPT operation and boost the dc voltage. The dc-dc converters' outputs are connected to a common DC bus. The common dc bus is then connected to the utility

grid via a step-up transformer by a central dc–ac inverter [46].

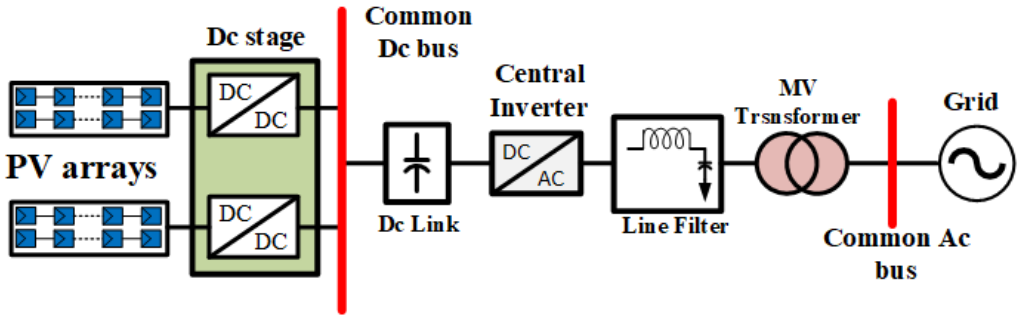


Figure 1.7: Conventional large-scale PV plant conversion system [46].

Although this configuration is common for PV grid-connected systems, it does not yet meet all the technical and cost-effective requirements for PV systems. This configuration requires the use of bulky and heavy LFT, large line filters, and boost converters, which considerably increases the weight and volume of the energy conversion system, its operating costs, and losses [47]. Employing this single central inverter system to supply high power to the main grid is challenging due to the power rating restrictions of existing power inverters and the semiconductor [48]. In addition, the vast number of PV modules connected in series in a PV array is controlled by a common MPPT algorithm, which can limit the system's overall power output of the string [49]. Thus, the configuration of the power converter unit is still under consideration.

A new energy conversion system could be found to continue to cope with the cost and to boost the LSPV power plant's performance. MLCs have gained considerable interest in PV power plants due to their superior physical modularity and scalability, high power density, independent MPPT control, fewer AC and DC filters, which are also smaller in size, a better harmonic spectrum, and fault-tolerant operation.

However, the implementation of MLCs often comes with some challenges, such as galvanic isolation requirements, distributed MPPT operation, and power mismatch. It is important to keep searching for novel configurations to develop a suitable converter design capable of meeting the future trend of PV systems.

1.5 Research Aim and Objectives

1.5.1 Aim

The Ph.D. research is conducted in light of the widespread deployment of LSPV power plants and the necessity for innovative power electronics topologies, which can operate at medium or high power and voltage levels. Consequently, this thesis embodies research undertaken on a three phase modular current source inverter (TPMI) based on submodules (SMs) of a novel dual-isolated SEPIC/CUK (DISC) converter.

The proposed TPMI topology is selected for the study because it offers a high output power density, galvanic isolation, suppression of bulky LFT and electrolytic capacitors, reduction in the number of switch components, and simplification of power stage design. Each of these merits and potential disadvantages will be discussed in more depth in the following chapters.

1.5.2 Objectives

As discussed above, the modular current source power electronics technologies will play important roles in the LSPV systems. The main research objectives are:

- To present a logical classification of high-power converters starting with MLCs and modular isolated converters. Their possible submodule configurations have

been investigated for integrating LSPV systems into medium-voltage (MV) AC grids.

- To propose a new current source converter SM topology with continuous input current for maximum power extraction and relatively low output ripples. The proposed topology is a descendant of both Sepic and Cuk, so it is possible to filter the PV system using a small film capacitor rather than a large electrolytic capacitor.

- To investigate a state space model of the proposed SM converter in order to identify and comprehend how the design parameters were picked, as well as to provide a reliable model of the TPMI topology .

- To explore a novel modular isolated inverter based on the DISC SMs to improve the energy conversion of PV plants. The proposed TPMI has several advantages over the conventional centrally installed system, such as modularity, scalability, fault tolerance, and better performance during shading conditions because of the use of distributed MPPT controllers.

- To propose a modified structure of the TPMI topology to reduce the number of switches and switching conduction losses. The modified structure employs a new modulation technique that operates in half cycles only.

- To develop a control technique for regulating the voltage and current fed into the grid. The DISC SMs with high-order open-loop transfer functions require rigid compensators for stable and reliable operation. Thus, a proportional-resonant (PR) controller has been designed to inject pure active power and obtain a higher

level of stability. The PR controller is straightforward in design and validates simply on standard DSP boards.

- To evaluate the proposed inverters performance under a variety of conditions using real-time simulation models.
- To create a scaled-down, low-voltage hardware testbed to experimentally validate the feasibility of the proposed inverters.

1.6 Thesis Outline

The thesis format consists of six chapters. Each chapter begins with a brief explanation of the thesis until that point and a summary of the chapter's aims. This is included to improve the thesis' readability and permits each chapter to be read independently.

Chapter 1 gives background context and configuration details for LSPV power plants. It includes a brief introduction to the challenges of PV systems, as well as the limitations of a conventional voltage source inverter and the leakage current. This is followed by a statement of the motivation, aims, and objectives of the thesis. It concludes with an overview of the thesis outline.

Chapter 2 presents a survey of a state-of-the-art multilevel inverter, which can be employed in PV power plants. This chapter compares the suitability of conventional MLCs and alternative topologies for LSPV applications. The final recommendation is to use an isolated TPMI structure, which is accompanied by its advantages.

Chapter 3 provides the details of a new DISC SM. The study covers operational concepts and modulation-switching techniques. A novel dynamic model is introduced

that acts as a theoretical foundation for the following design of the selected parameters and control strategy.

Chapter 4 discusses the analysis and design of the TPMI topology based on DISC SMs for processing and delivering a high level of power to the grid. The modular system's modes of operation and modulation techniques are described. The control system and its corresponding strategies are explained. A system-level controller and an SM-level controller are included in the analysis, it also proposes the PR compensator, which has been effectively implemented to regulate the output current and comply with the most recent grid codes. Finally, the control burden is reduced by allowing the use of low-cost DSP boards. Following this is the validation of the proposed inverter based on simulation and experimental results.

Chapter 5 investigates a modified DISC SM structure that improves the performance of the proposed TPMI by reducing switching losses. By adding an active switch and a diode to the AC side of the DISC SM and replacing two active switches with the diodes, the resulting SM can assist in reducing switch conduction losses and improve the inverter's efficiency. The operating principle and modulation scheme for this structure are described and the control system and its implications are presented. Both simulation and experimental results are provided to validate the performance of the improved structure.

Chapter 6 provides a summary of the thesis, focusing on the major contributions and how they relate to the original research objectives. This chapter concludes with recommendations for future research that would expand upon the results of this thesis.

Chapter 2

State of the Art Review

This chapter provides a detailed literature analysis that places the research objectives in the context of recent developments in power electronics. A summary of the challenges associated with high-power inverters in the LSPV system is included. In this chapter, the most common MLC topologies are investigated, and the disadvantages associated with their use in LSPV systems are reviewed.

Modular isolated converters are given special consideration in LSPV applications because they are a promising technology that aims to reduce extra conversion stages and improve system availability. Therefore, this chapter provides an insightful study of their possible configurations, and the most recent contributions to the field are explored to propose a novel and exciting inverter topology for improving the performance of LSPV systems.

2.1 High power PV inverters

A wide range of PV inverter systems with diverse characteristics is now available due to the rapid growth of LSPV applications over the past few years and the increased competition among companies in the market. The high-voltage grid-tied PV inverter system has substantial challenges, as in other high-power and industrial applications. Some of these challenges are galvanic isolation, power imbalances, and a central MPPT operation [47].

Firstly, the grid requirements, such as galvanic isolation, are met by placing LFT between the inverter and the grid. The bulky scale of LFT imposes additional limitations on the size and cost of the inverter. Moreover, the partial shading scenarios bring many challenges for the PV inverter systems, as these systems suffer from voltage variation and their operating point can shift away from the maximum power point (i.e., the MPPT controller can settle at the local maxima points instead of the global maximum), as shown Fig 2.1. Consequently, the maximum power output of the PV modules is reduced [50].

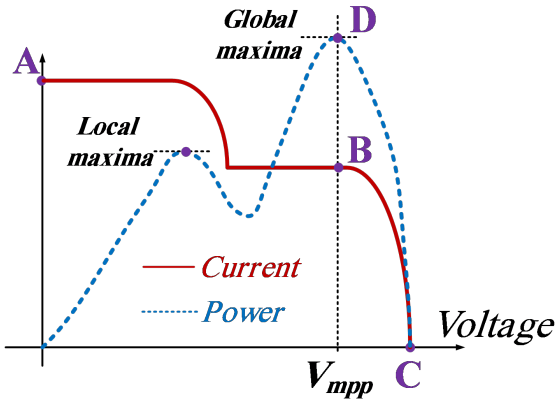


Figure 2.1: Current-voltage (I–V) and power-voltage (P–V) curves for PV module under partial shade.

Furthermore, the connection of a high number of PV modules can limit the system's overall output power, particularly when a central MPPT controller is employed for them all. With partial shading conditions, some of the PV modules will be shaded while the others are not in the same series string, especially when they are spread over a roof or a wide area. In this case, the unshaded PV modules will be affected by the shaded ones, and the total extracted power from the PV system will be significantly reduced [51].

Due to the previously mentioned challenges, extensive research on high-power density converters and novel control strategies is required for further development of LSPV power plants. Consequently, the selection of LSPV power converters depends on a variety of operational and technological considerations for high-performance conversions. These are the most key considerations [52]:

1. **Initial Expense:** since the initial cost of the power converter is only a percentage of the total cost of the LSPV power plants, it should be kept as low as possible to make LSPV systems competitive with other energy sources [53].

2. **Maintenance:** it is preferred to reduce the required maintenance for inverters as much as possible to ensure the long lifespan of the PV system. This is crucial because inverters are usually considered vulnerable parts in PV systems [54].

3. **Efficiency:** the power converters in LSPV systems that operate at multi-MW rates are preferred to have high efficiency. Therefore, the power converter is favourable with its included features, such as its efficient control strategies, low power losses, and reduced switch stress. [55].

4. **Reliability:** the modular structure of the PV power inverters gives additional degrees of freedom for handling failure accidents and the capacity to maintain operation and reduce system downtime. This feature is not just for LSPV applications; it is essential for high-reliability applications such as uninterruptible power supply applications (military installations or emergencies) [56].

5. **Power quality:** the voltages and currents generated by the power inverter must comply with power quality specifications. Increasing the number of levels in the inverter reduces total harmonic distortion and dv/dt stress on the semiconductor devices. Although the system's power density and cost increase, its output filter requirement decreases. [57].

6. **Galvanic isolation:** the purpose of galvanic isolation is to prevent leakage currents from entering the PV installation. Usually, this is accomplished by the use of LFT, but it can also be embedded in some inverters via HFT.[58].

7. **Size and weight:** the lightweight and compact converter topology provides numerous degrees of freedom to reduce cost and power losses. This propriety is essential for applications with space or weight restrictions, such as offshore, space, and automotive applications [59].

8. **Grid compliance:** this is an important principle for grid-connected PV systems. The power inverter is preferred to have the fault-ride-through capability, grid support, and voltage/frequency conversion [60], [61].

2.2 Multilevel converters

Both academia and industry have demonstrated an increased interest in developing MLC topologies to provide new solutions for high-power LSPV applications. MLCs are a form of power electronic converter that can distribute DC voltage to many modules and generate three or more stepped output voltage levels [62], [63]. These topologies have several advantages over traditional two-level converters, such as a high power density, lower voltage stress on semiconductor switches, and less need for filtering on both the DC and AC sides [64], [65]. There are two main groups of MLCs: single DC source converters and multicell topologies [66]. This literature will provide an introduction to the MLCs, discuss the main topologies, and present different SM circuit designs and output voltage waveforms are depicted. In the following subsections, several MLCs will explain which are used in high and medium power PV plants. This will allow for a comparison of their performance for this application, as well as a discussion of the advantages and disadvantages associated with each topology.

2.2.1 Single DC source converters

Early MLCs used common dc sources with either a single dc-link capacitor or a series connection of capacitors on the dc side [67]. In this family of converters, the neutral point clamped (NPC) and flying capacitor (FC) topologies are usually found in the central configuration of PV power plants [68], [69]. Furthermore, many other topologies belonging to this family have been proposed and discussed in several literature reviews [70]–[72].

2.2.1.1 Neutral Point Clamped Topology

The neutral point-clamped (NPC) converter (alternatively called a diode-clamped converter) operates from a single DC source. The DC link is divided into different levels by capacitors, and these voltage levels are clamped by diodes. The NPC topology is preferred for MV motor drives applications. The most common power converters on the market are the ACS 1000 converter, which has a three-level NPC, and the ACS 5000 converter, which has a five-level NPC [73]. A three-level NPC with three converter legs is described in [74]. In a single-phase operation, the NPC converter can have either a single-leg design or a double-leg design. Each topology has its own advantages and disadvantages.

Half-bridge (HB) (single-leg) converters are limited to using just half of the available DC link voltage, whereas full-bridge (FB) (double-leg) converters face challenges with common-mode voltage. A HB three-level NPC, illustrated in Fig 2.2, is composed of capacitors C_1 and C_2 that generate voltage levels of $V_{dc}/2$ and $-V_{dc}/2$, respectively, and these voltages are clamped by diodes D_1 and D_2 [75].

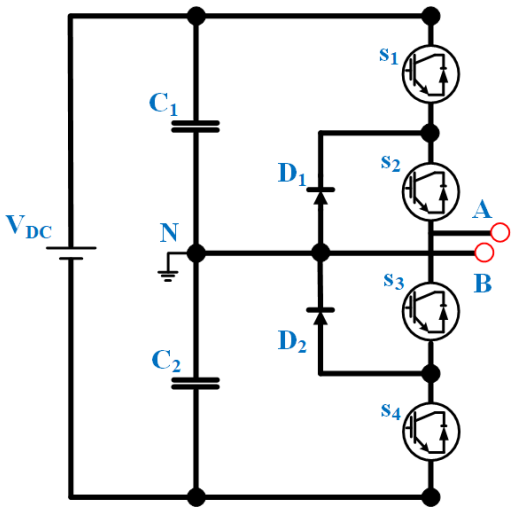


Figure 2.2: A three-level single-phase NPC.

Fig 2.3 shows the output voltage waveform of the single phase for the HB three-level NPC. The output voltage has an additional zero-voltage level, so the converter then has three voltage levels rather than two. The power quality of the output voltage improves as the number of levels increases and the shape more closely resembles a sinusoidal waveform. In addition, the voltage stress on the semiconductor devices would be lower because more devices would share them, but the number of capacitors would increase.

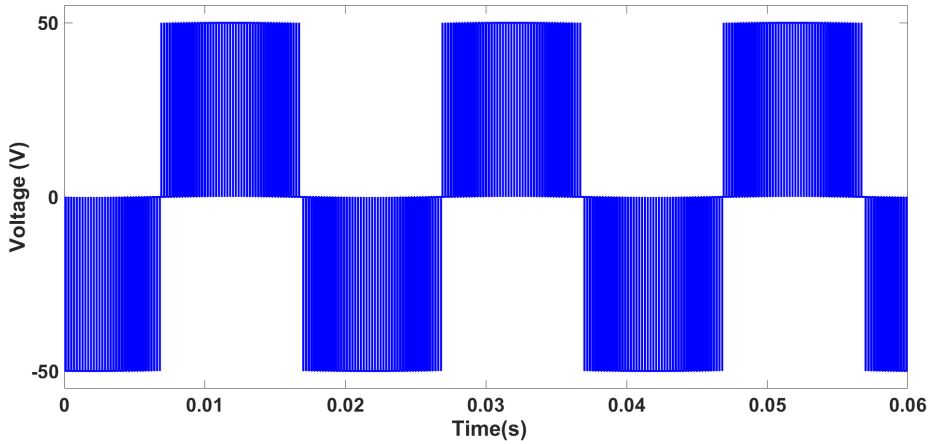


Figure 2.3: Output voltage waveform of HF3-NPC.

In terms of increasing output voltage levels, the NPC provides a diversity of topology possibilities. One option for a 5-level NPC is to add another leg to a classic HB 3-level NPC to form a FB 5-level NPC [76]. The single phase of the FB 5-level NPC topology is shown in Fig 2.4. This converter adopts the FB topology so that the DC link can be used in its output waveforms to its full capacity. Fig 2.5 shows the output waveform in which the 100V DC link is completely utilised.

An alternative way of generating a 5-level NPC is to augment the HB design with additional capacitors and diodes, as shown in Fig 2.6. Both the HB 5-level NPC and the FB 5-level NPC have five output voltage levels, but the HB 5-level NPC is

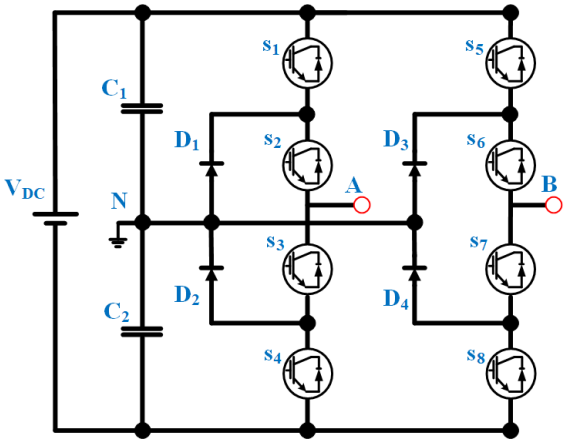


Figure 2.4: 5-level FB NPC.

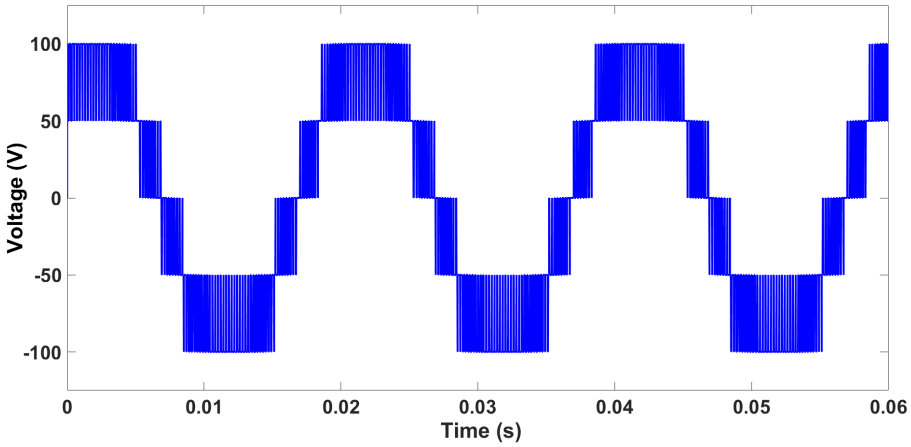


Figure 2.5: Output voltage waveform of 5 level FB NPC.

comprised of two additional diodes and four additional capacitors compared to the HB 3-level NPC [77].

Moreover, the output levels delivered by the HB 5-levels NPC differ from those provided by the FB version, which are $V_{dc}/2$, $V_{dc}/4$, 0, $-V_{dc}/2$, and $V_{dc}/4$, as it is presented in Fig 2.7. Although HB 5-levels NPC has a lower DC-link utilization than FB 5-levels NPC, this topology does not suffer the same common-mode voltage issues [78].

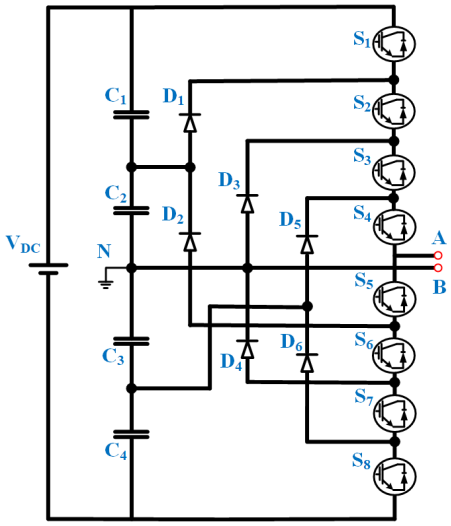


Figure 2.6: 5-level HB NPC.

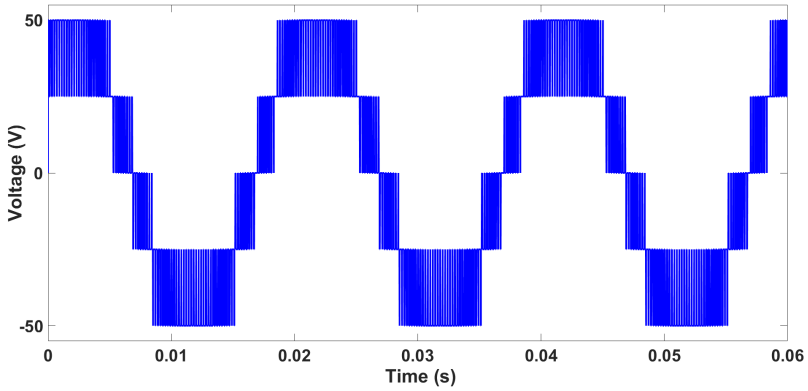


Figure 2.7: Output voltage waveform of 5 level HB NPC.

HB or FB structures are not the only versions to build an NPC converter. It is possible to design a structure that reduces the number of active switches by combining an NPC with a FC topology, as discussed in [79]. The research described in [80] focuses on a hybrid 5-level NPC and T-type inverter to enhance output voltage and reduce the number of power components.

However, the NPC topology suffers from unbalanced voltages exerted by the DC link capacitors with increasing output power, which can increase the total harmonic

distortion (THD) of the output voltage and damage the switching devices due to overvoltage breakdown. This issue can be addressed by adjusting the modulation technique to compensate for the DC-link capacitor voltage unbalance [81]. However, this increases complexity and requires the use of two additional voltage sensors to measure the capacitor voltages. Furthermore, a high number of clamping diodes will be required with increasing output voltage levels which contributes to increasing the cost, size, modulation, and control complexity . Therefore, These issues pose a significant obstacle to the use of NPCs as MLCs in LSPV power installations.

2.2.1.2 Flying Capacitor Topology

The FC topology is a modified version of the NPC in which the clamping diodes have been replaced by auxiliary capacitors that generate additional output voltage levels. Fig 2.8 shows HB FC topology with three output levels, which requires four switching devices. One of the most problematic aspects of this topology is the capacitor charge balancing for efficient operation, which can be challenging to maintain due to the high number of capacitors and the lack of clamping diodes. In this case, the voltage of the capacitors should be maintained at $V_{dc}/2$ to keep the output voltage levels balanced and ensure that all switching devices have the same voltage stress [82].

Fig 2.9 illustrates the output voltage waveform of the HB 3-level FC. The output voltage is balanced and transitions between $V_{dc}/2$, 0 , and -$V_{dc}/2$. While the number of levels in an FC topology increases, there are more redundant states for each output voltage level, giving the designer additional freedom in maintaining capacitor voltage levels. Although this is an advantage, higher output levels require balancing a large number of capacitors [83].

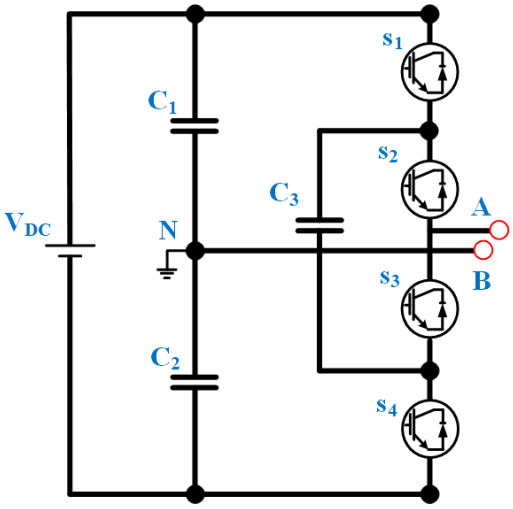


Figure 2.8: A three-level of FC topology.

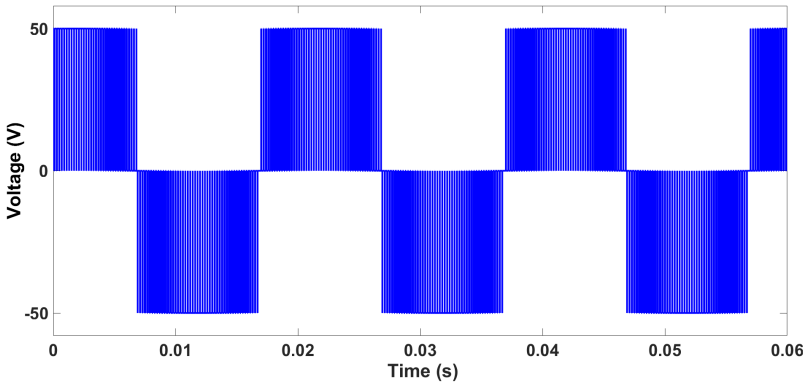


Figure 2.9: Output voltage of three-level FC.

With additional flying capacitors, it is possible to form a HB version of 5-level FC, as shown in Fig 2.10. The total number of capacitors is increased to ten, with four of them placed as DC link capacitors and the remaining six as flying capacitors to provide the voltage levels $V_{dc}/2$, $V_{dc}/4$, 0, $-V_{dc}/4$, and $-V_{dc}/2$. Fig 2.11 illustrates the output voltage waveform of a 5-level HB FC topology [84].

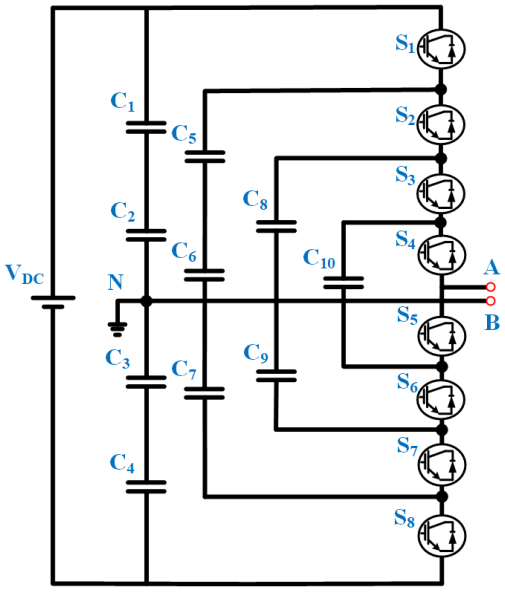


Figure 2.10: A five level of HB FC.

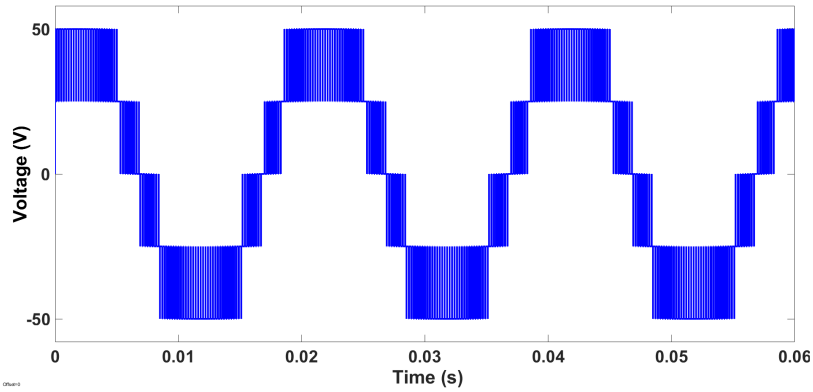


Figure 2.11: Output voltage of 5 level HB FC topology.

An inverter based on FC topology can be modularized and expanded to accommodate higher voltage levels and greater power density [85]. Although the FC topology is cheaper than the NPC topology, it has some limitations that prevent it from being employed as MLCs for a high-power solar PV system [86]. Firstly, many capacitors need to be employed to match the voltage of the MV grid, requiring a complicated

control technique to complete the pre-charging operation of the flying capacitors to meet the voltage-level specifications. Thus, the operation becomes more complicated and expensive at high power levels [87].

In addition, the FC topology requires a common DC link formed by a high number of PV modules connected in series, therefore the MPPT operation is centralized, which decreases its modularity and efficiency. ALSTOM has recently developed a six-level hybrid system for PV applications to reduce the effects of pre-charged flying capacitors and problems with voltage regulation. This system combines three levels of an FC system with two levels of an inverter system and uses an auxiliary balancing circuit [88]. However, this is insufficient to make the MV grid's voltage safe.

In a similar way to the NPC, the FC topology does not provide galvanic isolation between the PV arrays and the grid-connected output side. Consequently, the use of heavy and bulky transformers remains necessary for isolation [89]. For these reasons, the NPC and FC MLC topologies are not able to meet all of the requirements of medium-and high-voltage PV applications.

2.2.2 Multicell converters

In contrast to the family of single-dc sources, the multicell converters have been designed to operate at higher voltage levels. Multicell converters are formed from a series of connections of converters, also known as submodules (SMs). This simplifies the process of operating at high voltages and continuing with reduced capacity during failures. Since SMs are connected to separate dc supplies, they can be added or removed easily. Cascaded H-Bridge (CHB) and Modular Multilevel Converters (MMC) are among the common multicell converters used in HVDC systems [90], [91].

The next subsections introduce these converters found in PV applications.

2.2.2.1 Cascaded H-Bridge Topology

The CHB-converter topology is a promising MLC option for large-scale PV applications. CHBs are made up of several cascaded H-bridge SMs with separate DC power sources on their input sides. CHB topologies offer several advantageous features that make their use in large-scale PV applications promising [92]. The structure's scalability allows for the generation of high voltages, as the voltage levels can be increased. The CHB modular design provides the capability to replace any SM that unexpectedly fails, which helps in increasing the overall system availability. Moreover, its structure guarantees independent MPPT control among all PV arrays [93]. For PV applications, the CHB topology was proposed in three different configurations: with separate PV modules, a common dc link, and a common magnetic link [50].

Separate PV modules configuration

The first form of CHB topology in PV applications is the traditional three-phase CHB MLC, as depicted in Fig 2.12, where each H-bridge is directly connected to the PV array to collect the maximum amount of power, referred to as a single-stage conversion. Based on this structure, a small number of PV modules will be connected in a series to create a DC supply for each H-bridge [94]. This type of connection can increase the efficiency of solar PV systems because each PV string operates independently under its own control, resulting in improved MPPT performance [95]. However, the H-bridge is vulnerable to leakage current due to the parasitic capacitance between the PV modules and the ground. In addition, the system will become more costly and difficult to control as the number of PV modules increases [96].

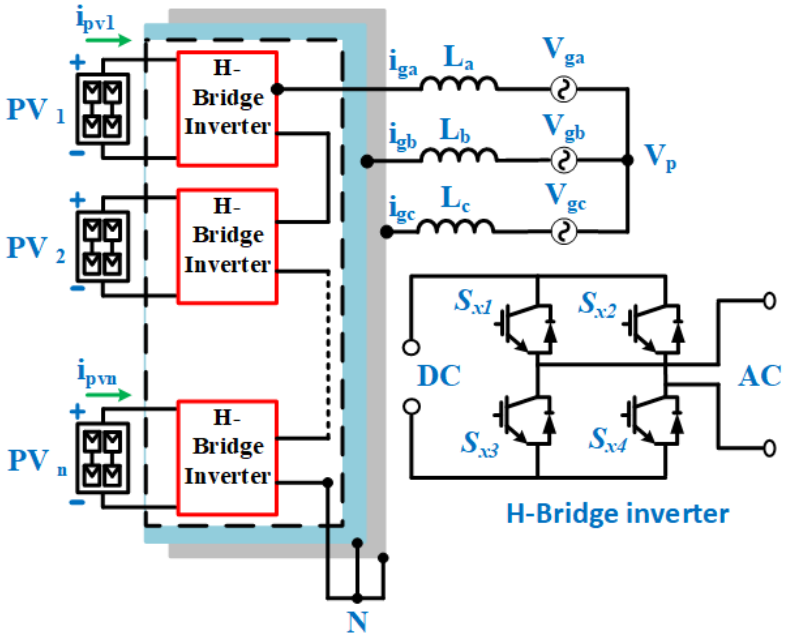


Figure 2.12: A three-phase CHB.

Another configuration of the CHB topology is using DC/DC converters (known as a two-stage conversion) in the LSPV system. Isolated DC/DC converters are used to prevent leakage currents, track the MPP of each PV module, and increase the voltage. In [97], [98], an isolated current-fed dual active bridge (CF-DAB) was used, as shown in Fig 2.13, to provide the required galvanic isolation and grounding, as well as a higher degree of control freedom. In addition, the authors suggested using film capacitors instead of large electrolytic capacitors, which are the least reliable parts of power converters, to reduce the ripples in the current coming in from PV converters.

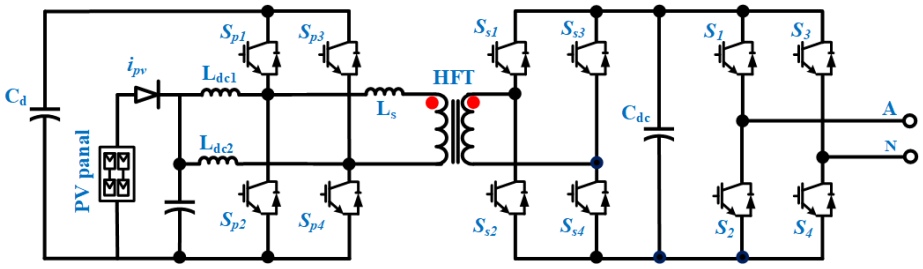


Figure 2.13: A CF-DAB converter with CHB based on SM.

In [99], further development of the CHB topology with an isolated DC/DC converter is proposed using an isolated forward dual-active bridge (F-DAB) converter. Its design, shown in Fig 2.14, provides galvanic isolation for the PV modules, as well as the ability to boost voltage and decrease EMI. Moreover, it is considered an alternative to CF-DAB converters because bidirectional power flow is not required for PV applications. Compared to other unidirectional converters, the F-DAB has better features, such as a higher power density and lower prices.

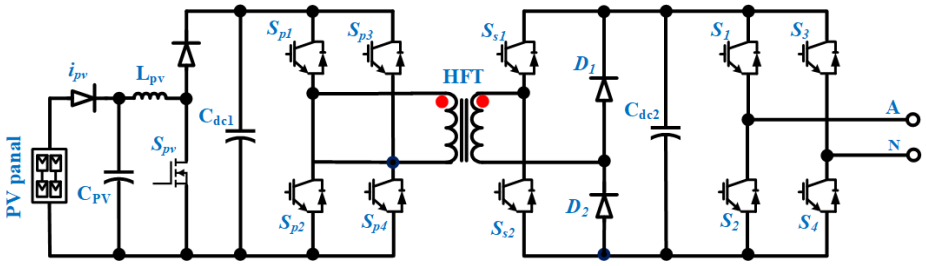


Figure 2.14: A F-DAB converter with CHB based on SM.

In this context, an isolated single active bridge (SAB) can be added as SM to the CHB topology to form a seven-level CHB prototype, as was proposed in [100]. As shown in Fig 2.15, each SM is made up of PV modules linked to a unidirectional SAB with a HFT to insulate PV arrays and increase the voltage gain. Moreover, the SAB converter was developed to operate with unbalanced PV power generation. However,

a DC-DC converter with a CHB topology has a two-stage power conversion, which results in higher power losses, and the need for extra filtering capacitors makes the conversion system bulky and decreases the lifetime of the converters.

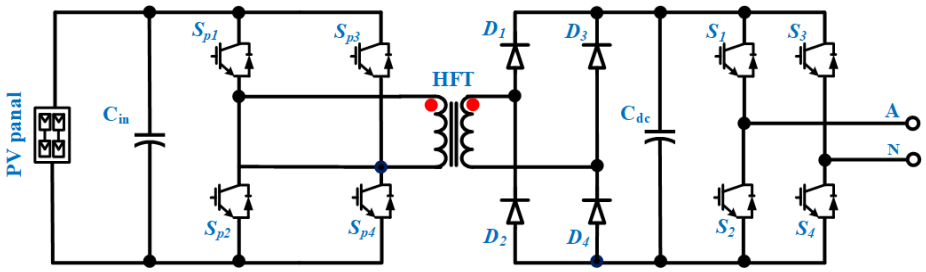


Figure 2.15: A SAB converter with CHB based on SM.

Reference [101] describes a new version of the CHB MLC that decreases the number of switches by adding an auxiliary circuit in a PV system that is integrated with the grid, as shown in Fig 2.16. However, it still lacks the isolation necessary for a PV system and grid connection, so it can cause to have high leakage currents. Due to the lack of electrical isolation, parasitic capacitances build up between the PV arrays and the ground, causing damage and posing a safety risk.

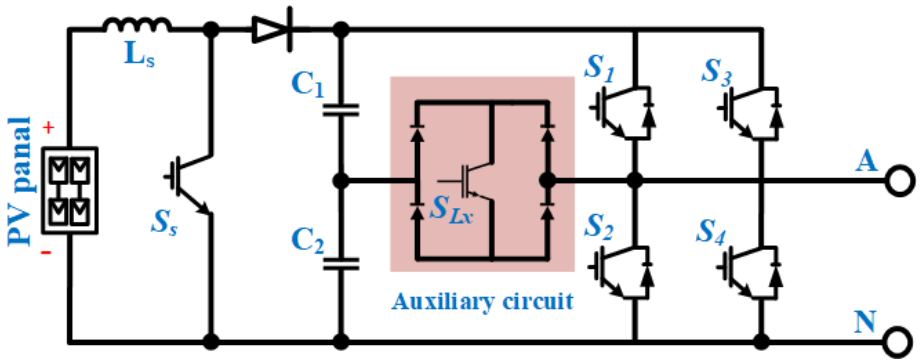


Figure 2.16: A single CHB SM with an auxiliary circuit.

A configuration with ac–ac conversion (using a cycloconverter) can reduce the stage of power conversion and improve system efficiency. Consequently, a modified

CHB converter based on a cycloconverter circuit was used to make the MLC CHB topology [102]. In the system shown in Fig 2.17, the DC voltage is converted to AC using a full-bridge inverter. Furthermore, each secondary of the transformer is then connected to a full-bridge AC–AC converter to produce output AC voltages. Although the number of power conversion stages is lower in the proposed topology, adding more switching devices would increase the total cost.

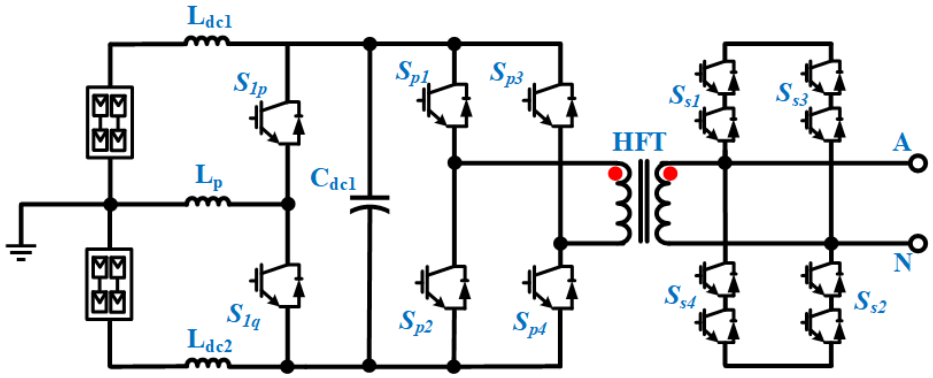


Figure 2.17: Modified CHB converter based on a cycloconverter.

A common dc link configuration

The second version of the CHB topology is formed in the LSPV system by using a common dc-link, as shown in Fig 2.18. This has been introduced as a solution to address voltage imbalance challenges in PV converters caused by partial shading, uneven solar irradiation, uneven module degradation, and different ambient temperatures [103]. In [104], it was suggested to use a modular structure with a common DC link, where the PV modules and their DC/DC converters are connected to a common DC bus. Then, isolated flyback DC/DC converters are used as the active front end for each port to provide galvanic isolation and independent MPPT control. Although fly-back converters are noted for their cheap and simple design when

compared to other isolated topologies, they suffer from discontinuous input currents that increase generated harmonics and decrease the converter's efficiency. Moreover, The direct connection of many sources via a common dc-link presents some challenges, including isolation and the requirement for additional control circuits to compensate for voltage imbalance and common mode.

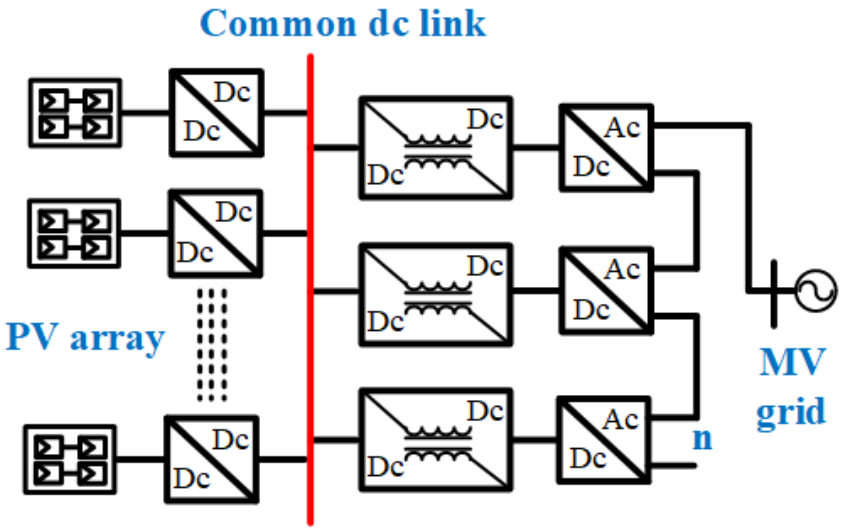


Figure 2.18: A CHB MLC with a common DC bus.

A common magnetic link

A common high-frequency magnetic link is introduced and employed in the CHB configuration for LSPV plants. Several paper studies have analysed the benefits of employing a CHB MLC topology with a common high-frequency magnetic link in PV systems [105], [106]. For instance, the need for multiple isolated DC/DC converters and a common DC link can be eliminated, resulting in a decrease in the number of conversion stages and an increase in performance efficiency. Fig 2.19 presents the CHB topology with a common high-frequency magnetic link developed in [106] for direct integration of PV sources. The PV arrays are connected to a common magnetic

link, which feeds the converter's H-bridge cells with isolated DC power. The shared magnetic link was proposed to improve the insulation of PV modules, handle voltage unbalances, and limit their effects on grid currents. However, The modular inverter structure is compromised by a shared magnetic link, which reduces the system's overall reliability because of the resulting loss of modularity. Furthermore, the inverter topology has a limited power rating for high-frequency switching operations due to the high leakage inductance and power handling capability of the switching devices.

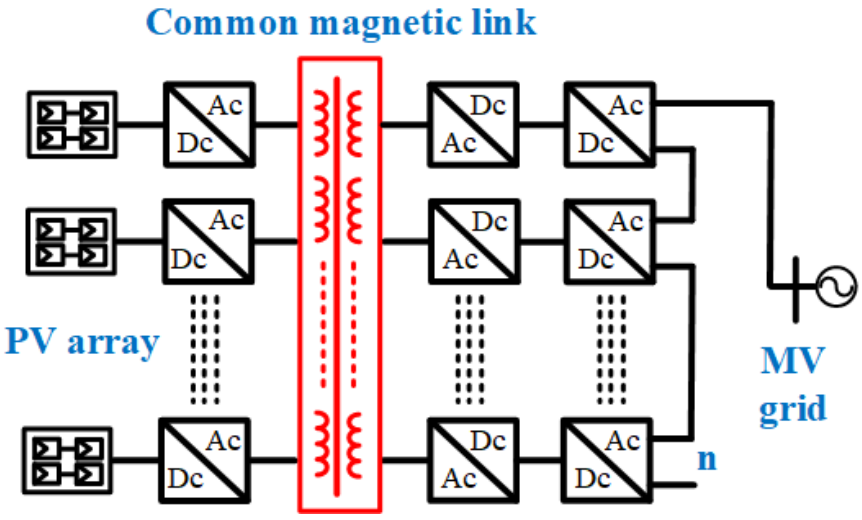


Figure 2.19: A CHB MLC with a common magnetic link.

As an alternative to a high-power magnetic link, [107] proposes the use of several low-power magnetic links to improve modularity and reduce leakage inductance. Fig shows 2.20 a modular CHB topology with several magnetic links developed for three-phase PV grid-connected applications. High-frequency magnetic links are used to connect the H-bridges, with one primary winding connected to the PV arrays and three secondary windings for the three-phase grid connection [108]. However, the described circuit demands an additional unit with magnet links, which expands the

footprint of the converter. Consequently, the design and cost of the magnetic core remain the major obstacles.

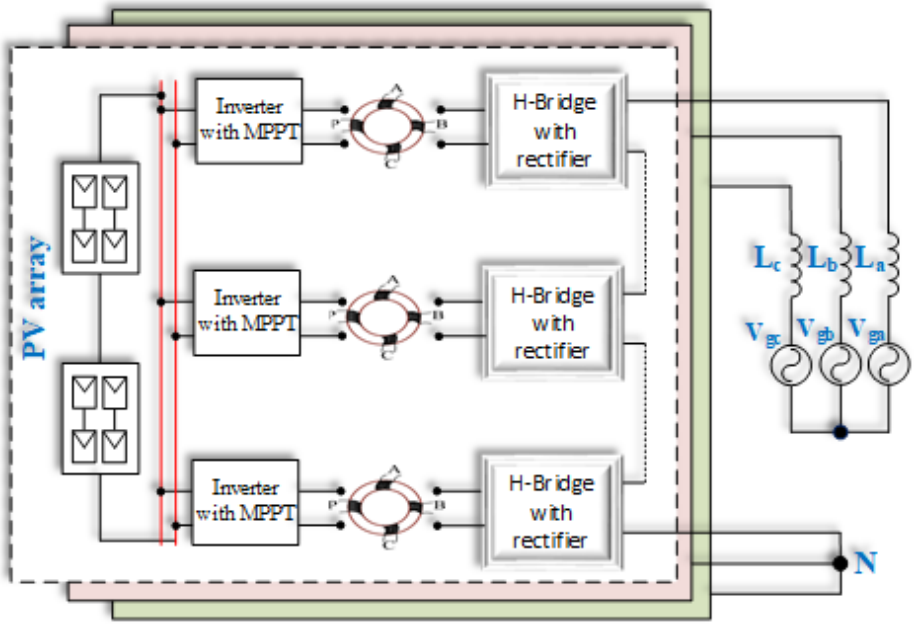


Figure 2.20: A CHB MLC with several magnetic links.

2.2.2.2 Modular-Multilevel Converter Topology

The modular multilevel converter (MMC) topology was introduced in 2003. It possesses a high degree of modularity and scalability, comparable to the CHB topology. However, it has a shared DC supply, similar to the NPC and FC topologies [109]. The MMC structure is formed from upper and lower arms with many SMs connected in series. These SMs are designed as either a HB or FB with a parallel connection of floating DC capacitors. Having a floating capacitor on each SM allows for using a single DC supply but increases the control complexity. In addition, an MMC needs an inductor in each arm because a circulating current flows through them during regular operation [110].

The MMC topology is a promising technology for industrial MV converter applications such as industrial motor drives [111], high voltage dc transmission [112], and STATCOM [113] due to its advantageous properties, such as its reliance on a single dc source, its capability to control the internal power flow, its high modularity, and its scalability. Although the MMC topology has been widely studied for a variety of developing applications over the past several years, only a few research papers have focused on its applicability in LSPV systems. [57]. There are two versions of MMC topologies that can be used in PV applications: one with a common dc-link and the other with separate PV arrays connected to their own SMs.

A common dc-link connection

In [114], a developing MMC topology with a common dc-link was considered. As shown in Fig 2.21, the proposed structure eliminates the PV modules connected to the dc side of the MMC and connects a PV module in parallel to the capacitor of each SM of the MMC. This study introduced a new capacitor balance voltage based on the modulation control of the virtual submodule (VSM) employing the so-called selective virtual loop mapping. The control strategy is based on modifying the loop mapping relationships between the VSMs and the real SMs to balance the capacitor voltages despite the presence of asymmetrical SMs, which makes voltage balancing easier for a large number of SMs while requiring no additional computational effort. However, the large number of PV modules are connected in series to provide a common DC link, and the MPPT is operated centrally. This drastically reduces the power generated under partial shading conditions [108].

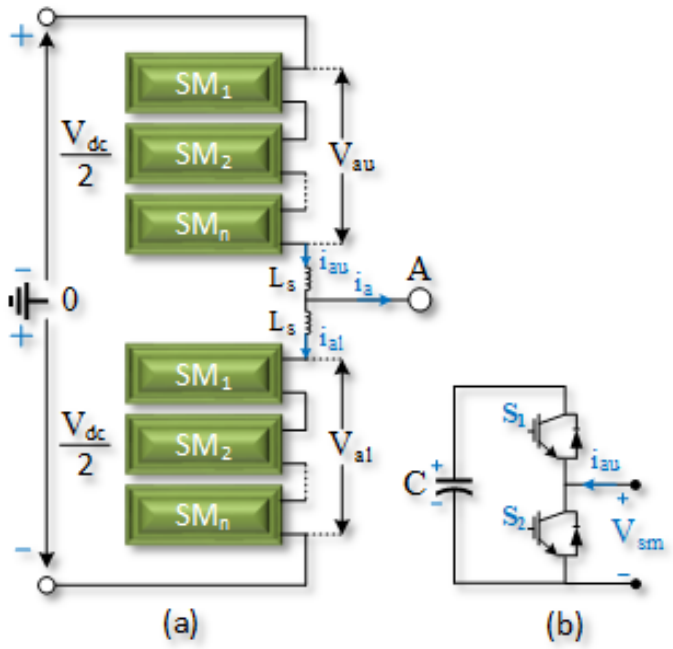


Figure 2.21: (a) MMC topology with a common DC link, (b) SM.

In the same context, a modified MMC circuit topology for PV distributed generating systems was described in [115]. The circuit design replaces arm inductors with an open-ended transformer and divides arm inductors into two windings. The suggested modification can reduce the voltage rating of the power devices, the size of the SM capacitor, and the needed DC bus voltage. However, it still possesses the central MPPT issue, which hinders the extraction of maximum output power from the PV systems.

Another structure of MMC with a common DC link is the topology, which is connected to a DC link comprised of many PV arrays integrated into the SMs. This topology allows independent MPPT control and operates effectively under shading conditions [116]. The topology structure is composed of several SMs that are directly connected to the DC link. A redundancy SM was added to each arm to compensate

for the voltage drop caused by partial shading. The topology control can address the MPPT multi-peak optimization issue and balance the power between the converter arms under partial shading conditions. Even though MMC-based PV integration is a viable option, the high number of components makes the system more expensive and less reliable without galvanic isolation.

Separate PV arrays connection

Similarly to the CHB topology, MMC topology systems use an isolated dc/dc converter stage to connect the PV modules to the MMC topology's dc/ac conversion stage to achieve galvanic isolation and improve MPPT control performance [117], as depicted in Fig 2.22.

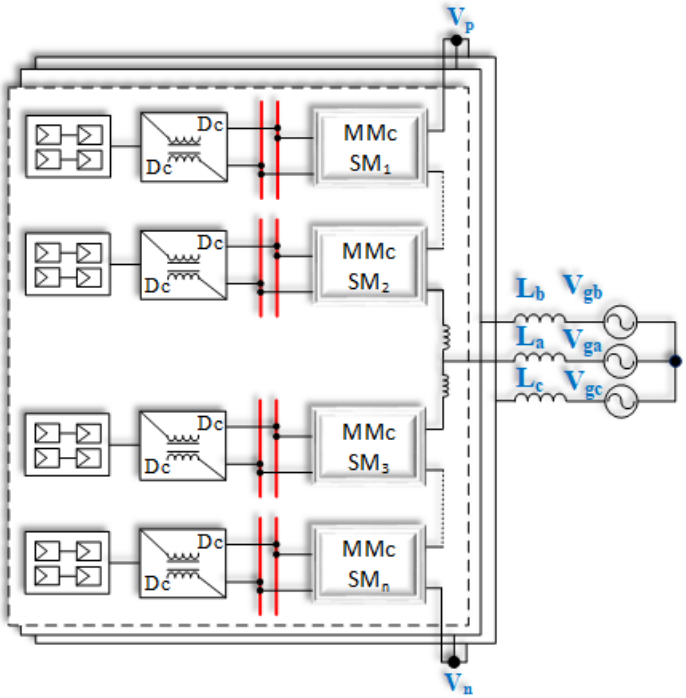


Figure 2.22: MMC topology with a stage of isolated dc/dc converter.

A simple isolated flyback converter was proposed to be the isolated stage to connect the PV modules to FB MMC SMs, which ensures the PV modules' distributed MPPT operations and grounding [118]. This independent MPPT control will contribute to extracting the maximum available power from the PV modules. However, the discontinuous nature of the fly-back converter's input currents contributes to the necessity for a large electrolytic capacitor, which reduces system reliability. Similarly, an isolated DAB converter was employed to connect PV modules to a HB of MMC SMs [119]. The proposed isolated DAB converter provides independent MPPT control and the grounding of PV modules. However, the use of DAB for the isolation stage is unnecessary as bidirectional power flow is not required in PV systems. In addition, the number of switches and extra circuits that come with DAB raises the cost and lowers the power density.

In [120], a different version of the MMC topology is shown that has fewer switches and is based on a unidirectional DC converter for the isolated stage, as shown in Fig 2.22. In this version, a group of parallel PV arrays is connected to the HB SMs by an isolated single SAB converter to transmit PV power to the grid. The suggested circuit can address any power imbalances between the MMC arms while keeping modularity, simple scalability, and independent MPPT control. Moreover, its control approach can balance the power between the MMC phases by injecting only the DC component of the circulating current while limiting the AC circulating currents to a minimum, which boosts the MMC's stability and decreases its internal losses. However, the MMC's output has more harmonics because the SAB converter's secondary side is not controlled. This makes the SAB converter less efficient.

Table 2.1 provides several performance metrics for configurations of CHB and

MMC converters found in the literature.

A summary of CHB and MMC converters				
Topology Fig	Distributed MPPT	Galvanic isolation	Modularity	Challenge
Fig 2.12	High	Low	High	Power balancing
Fig 2.18	High	High	Low	Voltage balancing and common mode
Fig 2.19	Low	Low	Low	Power balancing
Fig 2.20	High	High	High	Complex design
Fig 2.21	Low	Low	High	Circulating current
Fig 2.22	High	High	High	Arm power balancing

Table 2.1: Comparison of CHB and MMC based on performance considerations.

2.3 Modular Isolated MV converters

New PV inverters have been developed and made available as alternatives to existing topologies to make them more appropriate for PV applications at the MV level. These topologies are inspired and designed to use power converters in their SMs to improve power conversion; they are known as modular isolated converters [50]. They are in between the CHB and MMC topologies; hence, they possess outstanding features, such as modularity, scalability up to high-voltage or high power, low stress on the power switches, and a high degree of reliability [121]. In addition, these topologies offer a promising future for PV applications by providing galvanic isolation, distributed MPPT control, and the elimination of mismatch power in order to maximise the power output of their SMs [122].

Although LFTs are conventionally used to provide the necessity of galvanic isolation in PV applications, they have some shortcomings [47]. The recent development of silicon carbide (SiC) technology has introduced the use of HFTs due to the improved performance of SiC switches in high switching frequency applications [123]. Employing HFTs in these SMs allows the removal of the bulky LFTs and the operation at a high switching frequency of more than 20 kHz, thus reducing their overall size and increasing their power density [50]. Consequently, several SM circuit topologies for use in PV inverters have emerged. These SM topologies can be interconnected according to their input and output sides. The four possible connections are input-parallel output-series (IPOS), input-parallel output-parallel (IPOP), input-series output-parallel, and input-series output-series (ISOS) [124]. Therefore, there is always a tradeoff between PV requirements and the cost, loss, and complexity of SM. These aspects should be considered by the designer of a high-power inverter with a large number of SMs.

The flyback converter is a well-known topology because of its simplicity and low cost, and it can be designed to connect with a PV-tied grid to offer both isolation and unidirectional power flow, as shown in Fig 2.23 [125].

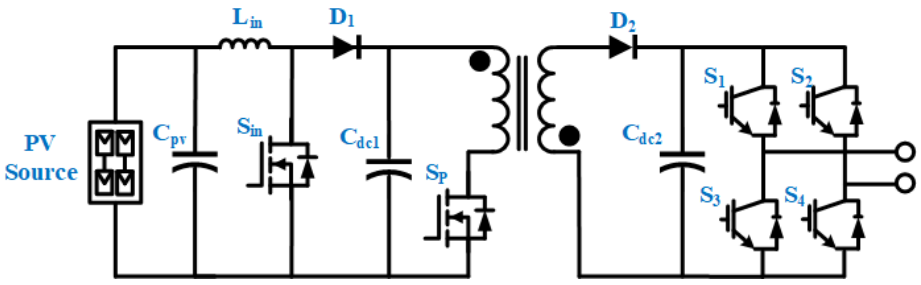


Figure 2.23: A single SM of flyback converter.

In [126], a three-phase modular fly-back topology inverter is presented. The

proposed inverter structure consists of parallel SMs based on modular isolated flyback converters with a suitable power level. These SMs are connected in parallel on the DC input side and differentially on the grid side. The performance of flyback benefits from HFTs to provide voltage-boosting and galvanic isolation. Multiple fly-back SMs are connected in parallel to allow current distribution, resulting in an increase in the apparent switching frequency and a corresponding reduction in the size of HFTs. Although the proposed structure is modular, the power capability does not rise proportionally with the number of SMs. To add more power to this structure, more SMs and PV modules must be connected in parallel with the ones that are already there. Thus, it is more suited to low-power applications, as seen by the results. Moreover, the flyback suffers from discontinuous current nature at the input and output sides, which is likely to limit the conversion efficiency [127].

Amongst several SM circuits, DAB converter, as described in Fig 2.24, is a suitable option for developing medium- or high-voltage power converters [128]. The modular DAB SM structures, such as input-series-output-parallel and input-series-output-independent output, are widely used for integrating LSPV into grids [129]. Due to their galvanic isolation, soft-switching capability, high power density, and simple control, they have the capability to achieve zero voltage switching (ZVS) and switch frequencies up to one megahertz [130]. However, they feature a relatively high number of switches, which contributes to a higher price and greater power loss. Moreover, they offer bidirectional power flow regulation, which is unnecessary for PV applications.

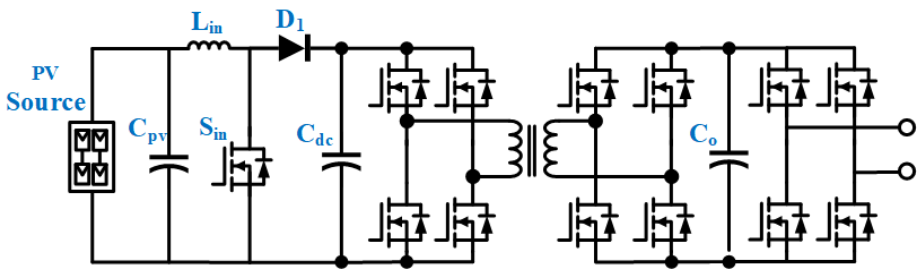


Figure 2.24: A single SM of DAB converter.

In the same context, a silicon voltage fed (VF)-DAB SM for the structural converter of a modular isolated converter was reported in reference [131]. The recommended SM employs polypropylene film capacitors in place of typical electrolytic capacitors because of their relatively long lifetime and suitability for high-frequency operation. However, the unsymmetrical duty cycle control greatly increases the current through the transformer, which, in turn, increases the stress on the switches and probable saturation of the magnetic cores. To address this problem, a CF-DAB topology was presented as a way to limit the current flowing through the transformer [132]. The reliability of the system is increased because of the use of a film capacitor in the topology. Therefore, It is possible to realise an MPPT with no ripple at low frequencies that maximises the harvesting of PV energy [133].

Commonly, isolated unidirectional modular converters are designed to be compatible with the uni-directional character of the power flow in PV systems. Compared to other bi-directional SMs, theirs use fewer switches, which lowers the system's losses and costs. In [134], the SAB converter SM was designed to reduce the number of power switches and to provide unidirectional power flow. The modular SAB SM converter is presented in [135] and its SM connections are based on (IPOP)to obtain a higher power output. Even though the SAB is a simple and reliable converter with

a four-diode rectifier on the secondary side, the absence of control over the secondary side allows additional harmonics to enter the output current, hence reducing the converter's reliability.

To address SAB limitations, Semi-DABs were designed to permit independent control of the secondary side with only two active switches, as opposed to the DAB's four, as shown in Fig 2.25 [136]. Comprehensive semi-DAB analyses, designs, and experiments were conducted in reference [137]. Compared to DAB, semi-DAB has a wider ZVS range for output voltages and fewer active switches.

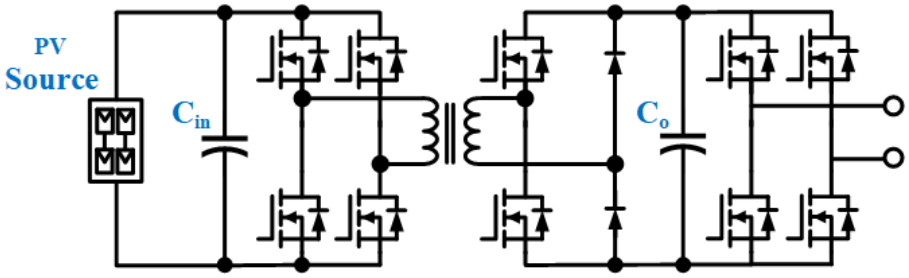


Figure 2.25: A single SM of Semi-DAB converter.

A prototype of F-DAB was employed in a cascaded multilevel structure to provide unidirectional power flow in a PV system [138]. The suggested F-DAB produces an industrial prototype of the SM converter with a much higher power density than other unidirectional topologies while using the same control as traditional DAB converters. The performance of different SM topologies is compared in many aspects in the table below Table2.2.

SM Topology					
Aspect	Flyback	DAB	SAB	Semi-DAB	F-DAB
Switch number	1	8	4	6	6
Power density	Low	High	Medium	High	High
Power flow	Unidirectional	Bidirectional	Unidirectional	Unidirectional	Unidirectional
Advantages	Low cost and simple control	High efficiency	Simple control and Low cost	ZVS operation	Compact, simple control
Disadvantages	Poor efficiency	High cost and switching losses	High output harmonics	Switching losses	High cost

Table 2.2: Comparison of the performance of several SM topologies.

To summarise, semi-DAB and F-DAB topologies are viable options for unidirectional power flow applications. However, the fundamental disadvantage of unidirectional modular isolated topologies is that they cannot be used for night-time STATCOM operations. As these topologies only allow regulated power flow in one direction from PV to load, control is lost if the flow is in the opposite direction [139].

Another interesting implementation of novel isolated current source converters with a modular structure has been developed for medium and higher PV grid-tied systems [33], [140]. In this study, selected isolated power converters are used and tested as SM candidates. A comparative study is presented to investigate the dynamic performance of four candidates' Buck-Boost SM converter topologies. These topologies are referred to as C5 (Cuk), F5, G5 (SEPIC), and P5 converters, as shown in Fig 2.26. Their symmetrical SMs connections are based on a modular structure with series output connections to generate a high output voltage. According to

the performance characteristics of these SMs topologies, both the CUK and SEPIC converter topologies can improve efficiency and accomplish inverter-wide objectives [32].

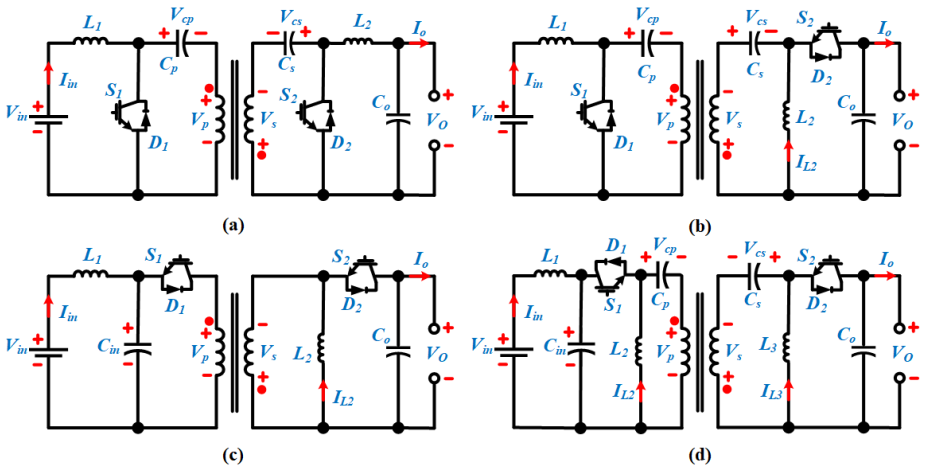


Figure 2.26: Buck-Boost isolated SM converters (a) Cuk (C5), (b) F5, (c) Sepic (G5), and (d) P5.

2.4 Research Prospects

Following the success of modular isolated power converters in high-voltage PV grid applications. There is increased demand for energy conversion with continuous input current flow. Cuk and SEPIC topologies have inherent continuous input currents, so they are preferred for maximising power extraction in modular isolated converter configurations.

Therefore, in this research, a grid-connected PV system will be investigated as the building block for the modular isolated converter in order to design a new SM topology that is a descendant of both Sepic and Cuk, where the total input current is continuous and the converter does not require a large electrolytic capacitor. In

this context, a new three-phase modular current source inverter (TPMI) based on the SMs of a novel dual-isolated SEPIC/CUK (DISC) converter has been developed to compete with existing converters in a well-established field.

2.5 Chapter Conclusion

This chapter introduced the high-power inverters that have received great attention in LSPV applications over the past few years. The information presented in this chapter provides knowledge of the structural basics, as well as the benefits and drawbacks of various inverters. In addition, the expected directions that future research on modular isolated converters will likely follow have been taken into consideration. Therefore, the present aim is to develop a highly efficient, highly reliable, and cost-effective modular isolated inverter based on SMs of power converter that addresses high-power PV inverter concerns so that it can be seriously considered as an alternative to existing MLCs. As a result, the modular isolated inverter could be able to compete with MLCs that are already on the market.

Chapter 3

A Dual-Isolated SEPIC/CUK Converter

There is a global trend toward using renewable or distributed systems with a modular structure to reduce costs and improve the efficiency of energy conversion systems [49], [141]. Consequently, the demand for compact converters that employ small passive components is increasing. Most dc-ac converters implemented in PV energy systems require large electrolytic filtering capacitors at both input and output. With a continuous current feature, the PV system can be filtered by using small film or plastic capacitors instead of large electrolytic capacitors. This can make the system more reliable and extend the life of the inverter [142]. In addition, PV systems require galvanic isolation; hence, the HFT converters are a promising possibility [58].

This chapter presents a new DISC converter used as a submodule of the proposed TPMI topology. The DISC converter is a possible structure for continuous-input dc-dc and dc-ac converters that do not require the installation of a bulky and unreliable electrolytic capacitor. Moreover, the novelty of the DISC structure is that it embeds

the HFT with one primary winding and dual secondary windings to achieve galvanic isolation. This can address the leakage current problem in PV systems and step up or down the input voltage. This chapter presents the DISC converter feature and discusses its advantages, particularly for PV applications. The following section explains the modulation scheme to ease the operation of the DISC converter, then, the steady-state average is explored. For this reason, a novel steady-state model is developed for an 8^{th} order DISC converter. A detailed explanation of the design principle behind the proposed converter's parameters is then presented. Finally, it concludes with the simulation results to validate the various design decisions.

3.1 Structure and features

The concept of a dual isolated SEPIC/CUK (DISC) converter is derived from the combination of two conventional isolated SEPIC and Cuk converters, each of are shown in Fig 3.1 [140], [143]. The following is a list of the characteristics of these converters that are most pertinent to the DISC converter:

- These converters have an input structure identical to one another on the input side; the only difference is the location of the inductor and the switch on the output side.
- They both generate the same amplitude output voltage for a given input voltage and duty cycle, as their voltage gain ratios are the same.
- The Cuk converter has a negative output voltage polarity, while the SEPIC converter has a positive output voltage polarity.

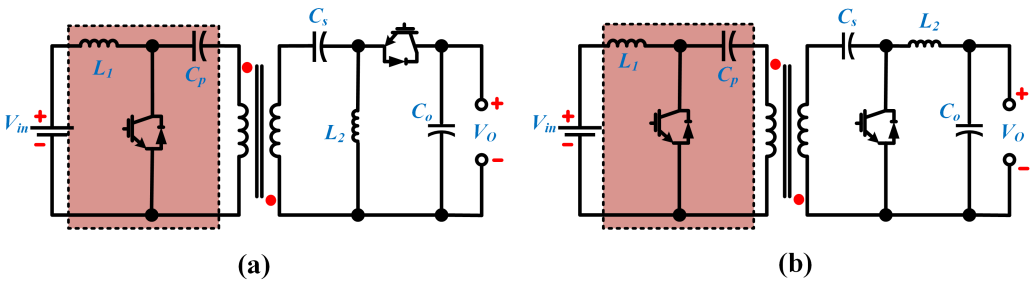


Figure 3.1: Topology (a) SEPIC and (b) Cuk converters.

The new DISC converter will be adapted as the SM in the proposed TPMI, with each SM being connected to PV arrays. The DISC converter is constructed by merging the input stages of the SEPIC, and Cuk converters and their output stages are connected in parallel, as depicted in Fig 3.2. The DISC converter's structure comprises the following components:

- One switching device: more specifically, it is an input stage ground-reference switching device.
- Two switching devices: one for the Cuk and SEPIC outputs respectively.
- Three inductors: one for the input and one each for the Cuk and SEPIC outputs.
- One transformer core with one primary winding and two secondary windings. Energy flows through it instantaneously from the input side to the output side.
- Five capacitors: Three middle capacitors for energy transmission and one output capacitor for each of the Cuk and SEPIC outputs.

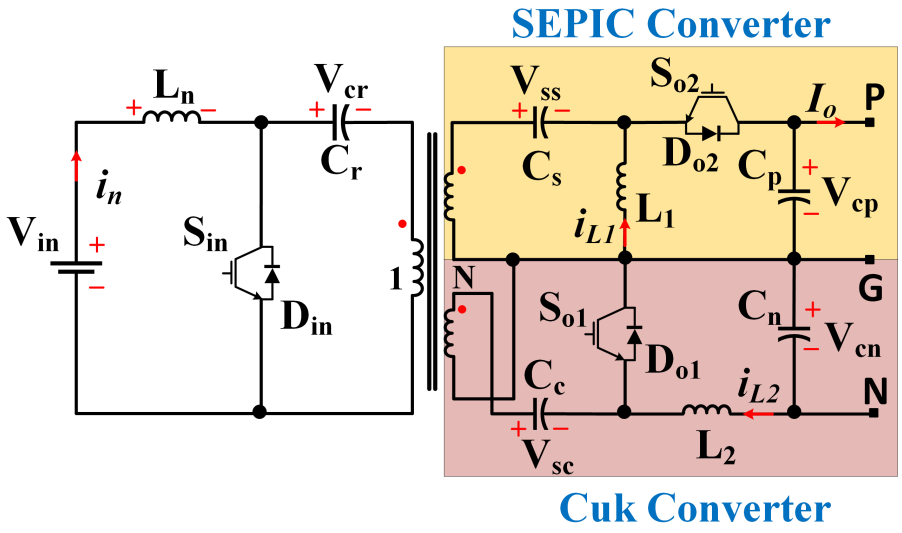


Figure 3.2: Topology of DISC converter.

The DISC converter can generate two symmetrical dc voltages with a neural point, resulting in balanced dual output voltages without the need for further voltage balance control. The proposed DISC is a current-source converter (CSC) that improves the performance of the MPPT controller by providing a continuous current. Thus, it is possible to use a plastic or film capacitor filter instead of a bulky electrolytic capacitor to reduce ripples on the input and output sides and to extend the lifetime of the PV system. Its structure can fit a compact HFT inside to obtain galvanic isolation, which is crucial for effectively addressing current leakage issues in PV inverters.

The most distinguishing feature of DISC is that the output switches S_{o1} and S_{o2} receive the same gate signal. Therefore, their output voltages are comparable in amplitude but they differ in polarity. The output voltage of the top structure (SEPIC) is positive, whereas the output voltage of the bottom structure is negative. In the same context, the output switches S_{o1} and S_{o2} operate in a complementary way to

the input side switch S_{in}. In addition, antiparallel diodes should be included in these switches so that the output current can be chopped when it is negative.

The DISC's voltage gain ratio is equal to the sum of the output voltages of the Cuk and SEPIC converters in a steady state. Because both of these converters are buck-boost converters, the voltage gain ratio of the DISC is:

$$\frac{V_O}{V_{in}} = \frac{2ND}{1-D} \tag{3.1}$$

The steady-state duty-cycle ratio and the HTF's turns ratio are represented by D and N, respectively. Compared to conventional buck-boost converters, the output voltage of the DISC is twice as high. The DISC converter is capable of delivering both significant step-up and step-down voltage conversion ratios, giving step-up conversion for duty ratios larger than 0.5 and step-down conversion for duty ratios less than 0.5. Moreover, the HFT can contribute to boosting the voltage gain by simply increasing the number of N if necessary.

3.2 Modulation Scheme

The modulation technique is employed to define the switching operation of the DISC converter to achieve the desired output. The gate signals for the DISC converter switches are generated by a comparison between the modulation and carrier signals. The modulation signal is a sinusoidal duty cycle and it is operated at the grid frequency. It can be tuned as $t_o = \frac{1}{f_o}$ where f_o is the frequency of the grid line. The switches of the DISC converter require a high switching frequency to increase power density which is achieved by generating a triangle carrier signal with a switching

interval of $t_s = \frac{1}{f_s}$. Here is the switching frequency, denoted as f_s.

This concept of modulation is referred to as sinusoidal pulse width modulation (SPWM), and it is a common modulation technique since it is straightforward and quick to apply in conventional DC/DC converter circuits [144], [145]. Consequently, the proposed modulation signal has a duty cycle calculation for the buck-boost DISC converter. It is obtained from the DISC converter's duty-voltage ratio as follows:

$$D = \frac{V_O}{2N\left(V_{in} + V_O\right)} \tag{3.2}$$

3.3 Operation principle

The DISC converter study's operation comprises of an analysis the converter's topology in its many switching states. In a similar way to the majority of DC-DC converters, the DISC converter can operate in either a continuous conduction mode (CCM) or a discontinuous conduction mode (DCM). The DCM operation has a number of benefits, such as increased efficiency (due to zero current turn-on), reduced inductor size, and better stability.

The DCM operation is slightly more complex for high-order converters such as the SEPIC and Cuk converters but remains intuitive. These converters are more complicated because they have two inductive parts. There is doubt about whether they enter DCM when the current in the input inductor drops to zero or when the current in the output inductor drops to zero. To operate in DCM, the converter should enter a third switch state; hence, the diode current must become zero for these converters. This happens when the total current of the two inductors is zero, which is the only time the diode turns off, making the DCM switch state [146].

The definition of DCM operation in the DISC converter is associated with some challenges due to the use of three inductors and also the incorporation of three switching devices. Therefore, the operation of the DISC converter in CCM mode is taken into consideration in this thesis. From the viewpoint of the input current, it is essential to maintain a minimal ripple. From the output current's point of perspective, keeping CCM ensures that the output voltage does not become load dependent and reduces the size requirements for capacitors.

The DISC converter operation can be subdivided and analysed into two switch states:

1. The 'ON' state of the input switch S_{in}, as shown in Fig 3.3, in which the input switch device is closed (considered a short circuit) and both output switches S_{o1} and S_{o2} are open (considered as an open circuit).

2. The 'OFF' state of the input switch S_{in}, as shown in Fig 3.4, is in which the input switch device is opened (considered an open circuit) and both S_{o1} and S_{o2} switches are closed (considered as a short circuit).

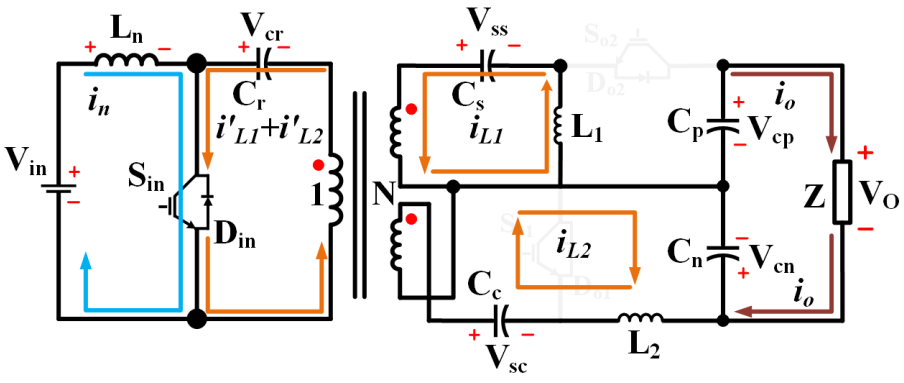


Figure 3.3: ON state.

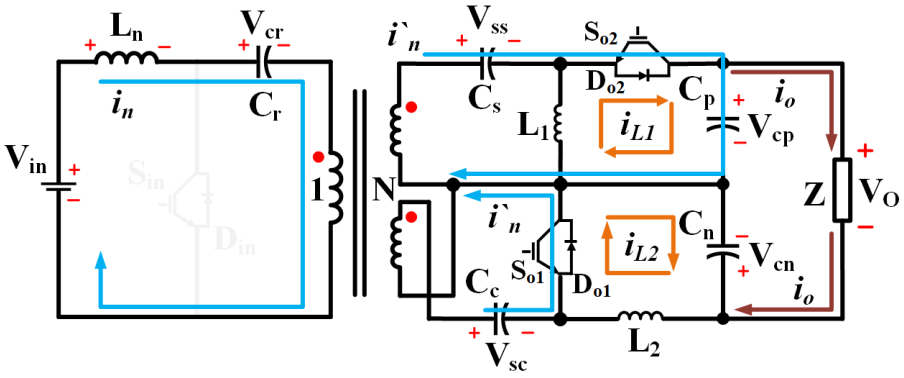


Figure 3.4: OFF state.

The steady-state operation of the DISC converter is detailed in full below (assuming ideal components for the sake of clarity):

- **State 1**

  By turning the input switch S_{in} 'ON', the input inductor's right side is shorted to the ground, causing the input current to rise accordingly $V_{in} = L_n \frac{di_n}{dt}$ and the energy stored in its magnetic field increases according to $E = \frac{1}{2} L_n i_n^2$. The switch has now grounded the positive terminals of the primary capacitor (C_r), SEPIC capacitor (C_s), and Cuk capacitor (C_c), meaning their right-hand side terminals have a negative potential with respect to the ground. The list below contains further explanations for *State 1*.

(a) As the upper output inductor L_1 is placed between the negative potential terminal of the primary and SEPIC capacitors and the ground, a positive voltage arises across it, causing its current to increase. This current goes from its terminal connected to the ground, through the inductor, the primary and SEPIC capacitors, and the switch, before returning to the ground. This results in the transfer of the energy stored in the primary and SEPIC capacitors to the

upper output inductor. By opening the upper output switch S_{O2}, the positive output capacitor then supplies the load, which causes its voltage to fall as it discharges.

(b) In the 'on' state of the input switch, the current through the output inductor L_2 rises because the voltage on the left side of the inductor is greater than the voltage on the right side. This results in the transfer of energy from the primary and the Cuk capacitors to the bottom output inductor. A square wave with a negative amplitude has been produced on the right-hand side of the Cuk capacitor. This voltage is applied to the LC filter, which then takes the average of this square wave voltage to make a smooth negative DC output voltage.

- **State 2**

  In contrast to the previous state, the output switches S_{o1} and S_{o2} are now both ON, whereas S_{in} is now OFF. The input inductor L_n attempts to maintain its current flow by producing a positive voltage when the output switches are turned ON. Thus, the right side of the input inductor has a voltage greater than the left side due to the left side of the inductor being clamped at the input voltage. This results in the input inductor current flowing into the primary, Cuk, and SEPIC capacitors, as well as via the output switches. With the input inductor current decreasing and the voltage across the inductor becoming negative as the right-hand side voltage grows larger than the input voltage, it is shown that the inductor discharges some of the energy stored in its magnetic field into the capacitors, increasing their voltages according to the equations $I = C\frac{dv}{dt}$ and $E = \frac{1}{2}CV^2$. At this point on the output side, the current is still flowing through both output inductors, but instead of passing through the

transfer capacitors, the inductors discharge their energy to the output through the output switches. The behaviors by which output inductors release their stored energy are explained as follows.

(a) In the upper (SEPIC) output, the output inductor L_1 supplies both the output and recharges the positive output capacitor C_p.

(b) At the bottom of the Cuk output, the output inductor L_2 releases its energy to the negative output capacitor C_n and then its voltage increases as it charges.

Component	State 1	State 2
L_n	Charging	Discharging
L_1	Charging	Discharging
L_2	Charging	Discharging
C_r	Discharging	Charging
C_S	Discharging	Charging
C_C	Discharging	Charging
C_p	Discharging	Charging
C_n	Discharging	Charging

Table 3.1: A summary of the DISC converter's steady-state CCM operation.

In reality, these four-step processes are only two states, and they are mentioned here for convenience in order to explain the operation process. A summary of component behaviour in the CCM operation of the DICS converter is provided in Table3.1, and the key operating waveforms that are generated by the DISC converter are shown in Fig 3.5.

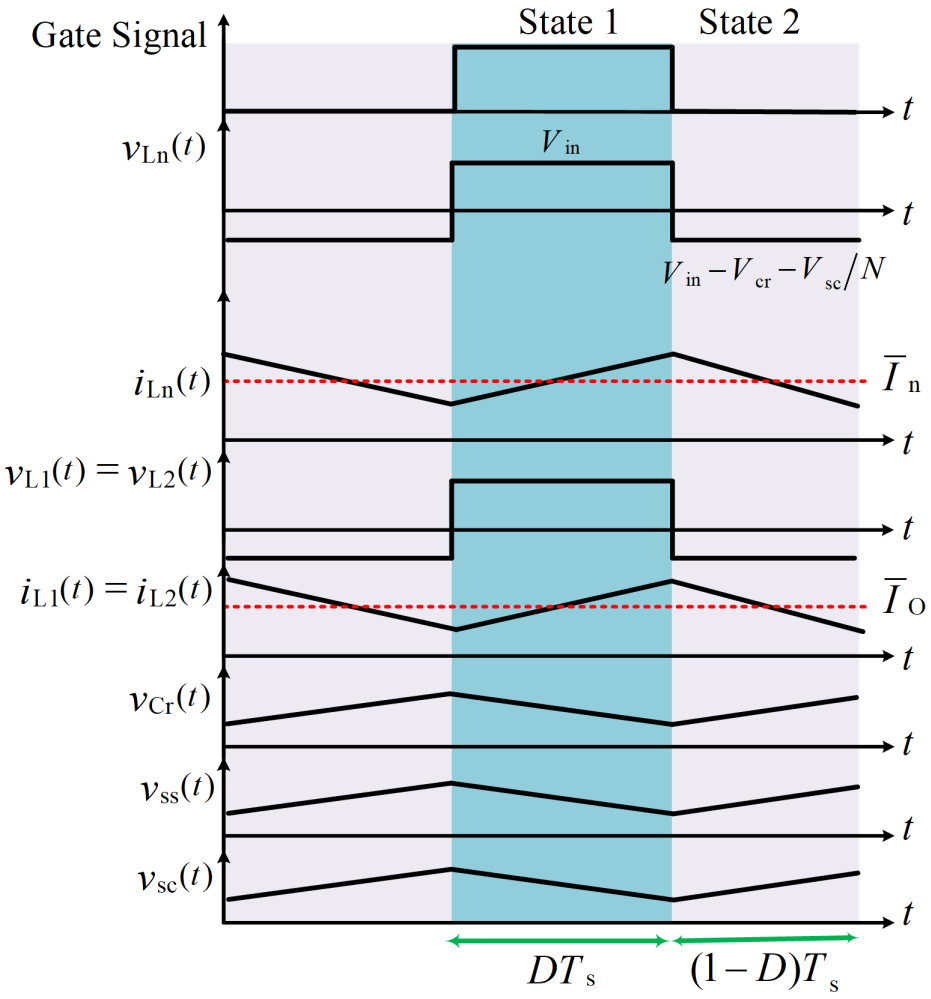


Figure 3.5: Key waveforms of DISC converter.

3.4 Analytical average approach

As discussed in the previous section, the DISC converter that has been presented operates in two different states. The state-space model will be extracted after these states are averaged over a switching interval in the following subsections.

3.4.1 Dynamic model

The state-space model is challenging to develop because the DISC is an 8^{th} order converter; hence, it has not yet been published in the literature . The DISC is a buck-boost converter with three inductors and five capacitors. The state-space averaged model for the DISC converter imitates the average behaviour of the inductor currents and capacitor voltages as the system's state varies. On average, these states change as the system operates with different duty ratios when it is excited.

A state-space average model can be derived by averaging the states of the variables over a switching time. Thus, the proposed DISC can be used with the ON and OFF state equivalent circuits shown in Fig 3.3 and 3.4, which are turned into a set of first-order differential equations by applying simple circuit laws. To simplify the dynamic model of the DISC converter description, it helps to understand the importance of the following aspects:

1. Each switching time interval (switch state) is described by its DISC converter's circuit.

2. The mathematical expression of state variables is written during the ON and OFF switch states.

3. Differential equations are used to characterise the ON and OFF states of each DISC converter circuit.

4. The state variables x are based on inductor currents and capacitor voltages.

5. The derivatives of inductor currents are expressed by using Kirchhoff's voltage law, while the derivatives of capacitor voltages are obtained by applying Kirchhoff's current law.

6. In the state-space equations, the state variables can be replaced with controlled voltage and current sources.

The state space of the DISC converter is analysed and configured out so that the behaviour of the converter can be more fully understood comprehended. In addition, controllers can be designed, stability and transient performance can be demonstrated, and the state space can be used in the process of parameter selection, which will be shown in the next section. The state-space model of the DISC converter can be derived over the switching time by formulating the following first-order differential equations that describe the liner system circuit [147].

$$\dot{x} = Ax + Bu \tag{3.3}$$

$$y = Cx + Bu \tag{3.4}$$

Where A, B, and C are the system, input and output matrices, respectively, the output voltage of PV modules is the input signal $u(t) = V_{in}(t)$, and the output capacitor voltages are $y(t) = V_o(t)$. The state vector $x(t)$ can be chosen as:

$$x(t) = [i_n(t)v_{cr}(t)v_{ss}(t)v_{sc}(t)i_{L1}(t)i_{L2}(t)v_{cs}(t)v_{cn}(t)]$$

The differential equations of these variables are derived over one complete cycle of switching operation t_{on} and t_{off} using Kirchhoff's laws, and yielding differential equations for both possible DISC converter states:

1. **State 1** ($0 \leq \mathrm{t} < Dt_s$)

   This state is formed during the ON circuit, as depicted in Fig 3.3 when the input

switch is turned on but the output switches are not. The differential equations for the state variables are as follows:

$$\frac{di_n}{dt} = \frac{1}{L_n} V_{in} \tag{3.5}$$

$$\frac{dv_{cr}}{dt} = -\frac{N}{C_r} \left(i_{L1} + i_{L2} \right) \tag{3.6}$$

$$\frac{dv_{SS}}{dt} = -\frac{1}{C_S} i_{L1} \tag{3.7}$$

$$\frac{dv_{SC}}{dt} = -\frac{1}{C_C} i_{L2} \tag{3.8}$$

$$\frac{di_{L1}}{dt} = \frac{N}{L_1} V_{cr} + \frac{1}{L_1} V_{SS} \tag{3.9}$$

$$\frac{di_{L2}}{dt} = \frac{N}{L_2} V_{cr} + \frac{1}{L_2} V_{SC} - \frac{1}{L_2} V_{Cn} \tag{3.10}$$

$$\frac{dv_{cp}}{dt} = -\frac{1}{C_p Z} V_{cp} - \frac{1}{C_p Z} V_{cn} \tag{3.11}$$

$$\frac{dv_{cn}}{dt} = \frac{1}{C_n} i_{L2} - \frac{1}{C_n Z} V_{cp} - \frac{1}{C_n Z} V_{cn} \tag{3.12}$$

2. **State 2** $(t_{on} < t < t_s)$

The second state is formed in the OFF circuit, as shown in Fig 3.4. In this state, both of the output switches are on, but the input switch is not. The state space operation becomes complicated and the differential equations cannot be solved without assumptions because of the input current passing through both the Cuk and SEPIC output sides and its path being divided across them. Therefore, these approximate assumptions are made possible as a result of the following observations:

(a) The average currents of the capacitors and the two states (state 1 plus state 2) over one full switching cycle are both zero, so the average currents of the inductors i_{L1} and i_{L2} are the same, as shown in the sub-circuit in Fig 3.6a.

(b) The current flowing in the inductor L_1 which is i_{L1} is equal to the output current i_O. In addition, the current flowing into C_p is so close to and almost equals the current in C_S, as seen in Fig 3.6b. Then, their equivalent series capacitance can be calculated from:

$$C_{eq} = \frac{C_s * C_p}{C_s + C_p} \tag{3.13}$$

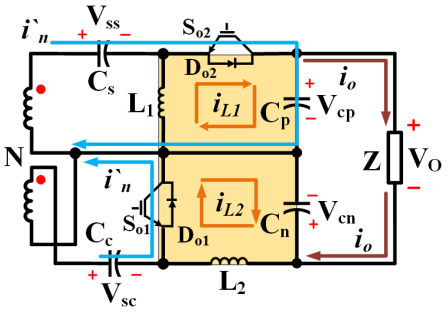
(c) Accordingly, the input current i_n is divided based on the impedance values of the capacitors on the output sides of the DISC converter. Therefore, as shown in Fig 3.6c, the ratio ρ that defines the total parallel connection of equivalent capacitors C_{eq} and Cuk capacitors C_c is available in the following formula:

$$\rho = \frac{C_c}{C_{eq}} \tag{3.14}$$

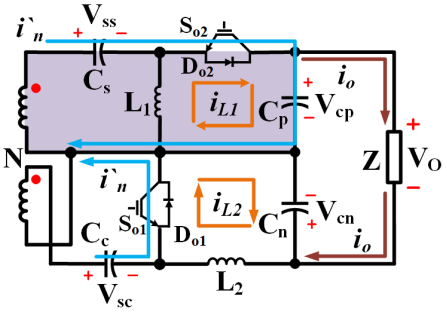
Thus, it is possible to express the currents that are flowing through the capacitors of SEPIC C_S and Cuk C_C thanks to the simplifications that have been made.

$$i_{ss} = \frac{i_n}{N(1+\rho)} \tag{3.15}$$

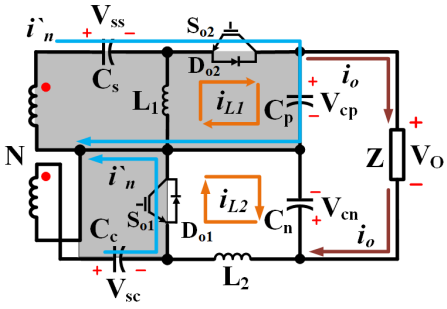
$$i_{sc} = \frac{i_n \rho}{N(1+\rho)} \tag{3.16}$$



(a) Sub-circuit current flow.



(b) Series capacitors loop.



(c) Current splitting.

Figure 3.6: Observations made in state2.

As described earlier, these observations and assumptions are required to simplify the differential equations that are used during *State 2* for the DISC converter. Herein, the differential equations can be derived as follows:

$$\begin{aligned} \frac{di_n}{dt} &= \frac{1}{L_n}V_{in} - \frac{1}{L_n}V_{cr} - \frac{1}{NL_n}V_{ss} - \frac{1}{NL_n}V_{cp} \\ \frac{di_n}{dt} &= \frac{1}{L_n}V_{in} - \frac{1}{L_n}V_{cr} - \frac{1}{NL_n}V_{sc} \end{aligned} \tag{3.17}$$

$$\frac{dv_{cr}}{dt} = \frac{1}{C_r}i_n \tag{3.18}$$

$$\frac{dv_{ss}}{dt} = \frac{1}{C_s} * \frac{1}{N(1+\rho)} i_n \tag{3.19}$$

$$\frac{dv_{cc}}{dt} = \frac{1}{C_c} * \frac{\rho}{N(1+\rho)} i_n \tag{3.20}$$

$$\frac{di_{L1}}{dt} = -\frac{1}{L_1} V_{cp} \tag{3.21}$$

$$\frac{di_{L2}}{dt} = -\frac{1}{L_2} V_{cn} \tag{3.22}$$

$$\frac{dv_{cp}}{dt} = \frac{1}{C_p} * \frac{1}{N(1+\rho)} i_n \tag{3.23}$$

$$\frac{dv_{cn}}{dt} = \frac{1}{C_n} i_{L2} - \frac{1}{C_n Z} V_{cp} - \frac{1}{C_n Z} V_{cn} \tag{3.24}$$

3.4.2 Modelling of DISC converter

The averaged model of two states can be obtained by finding deviations around steady-state operating points, which often depends on the duty ratio of the converter to obtain the necessary transfer functions. Consequently, the state-space representation for the model of **state 1** can be arranged, and the system matrices can be defined as follows:

$$\begin{bmatrix} \dot{i_{in}} \\ \dot{v_{cr}} \\ \dot{v_{SS}} \\ \dot{v_{CC}} \\ \dot{i_{L1}} \\ \dot{i_{L2}} \\ \dot{v_{cp}} \\ \dot{v_{cn}} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{-N}{C_r} & \frac{-N}{C_r} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{-1}{C_S} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{C_C} & 0 & 0 \\ 0 & \frac{N}{L_1} & \frac{1}{L_1} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{N}{L_2} & 0 & \frac{1}{L_2} & 0 & 0 & 0 & \frac{-1}{L_2} \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{-1}{C_pZ} & \frac{-1}{C_pZ} \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{C_n} & \frac{-1}{C_nZ} & \frac{-1}{C_nZ} \end{bmatrix} \begin{bmatrix} i_{in} \\ v_{cr} \\ v_{SS} \\ v_{CC} \\ i_{L1} \\ i_{L2} \\ v_{cp} \\ v_{cn} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_n} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} V_{in} \tag{3.25}$$

$$V_O = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & -1 & -1 \end{bmatrix} \begin{bmatrix} i_{in} \\ v_{cr} \\ v_{SS} \\ v_{CC} \\ i_{L1} \\ i_{L2} \\ v_{cp} \\ v_{cn} \end{bmatrix} \tag{3.26}$$

Similar steps are repeated for the **state 2** model. In this instance, the input switch is off, and the output switches are hence on. This results in a change in the system's

dynamics, which is reflected in new equations for the state space:

$$\begin{bmatrix} \dot{i_{in}} \\ \dot{v_{cr}} \\ \dot{v_{SS}} \\ \dot{v_{CC}} \\ \dot{i_{L1}} \\ \dot{i_{L2}} \\ \dot{v_{cp}} \\ \dot{v_{cn}} \end{bmatrix} = \begin{bmatrix} 0 & \frac{-1}{L_n} & 0 & \frac{-1}{L_n} & 0 & 0 & 0 & 0 \\ \frac{1}{C_r} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \frac{C_p}{N*(C_C C_p + C_C C_S + C_p C_S)} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \frac{C_p + C_S}{N*(C_C C_p + C_C C_S + C_p C_S)} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{L_1} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_2} \\ \frac{C_S}{N*(C_C C_p + C_C C_S + C_p C_S)} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{C_n} & \frac{-1}{C_n Z} & \frac{-1}{C_n Z} \end{bmatrix} \begin{bmatrix} i_{in} \\ v_{cr} \\ v_{SS} \\ v_{CC} \\ i_{L1} \\ i_{L2} \\ v_{cp} \\ v_{cn} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_n} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} V_{in} \tag{3.27}$$

$$V_O = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & -1 & -1 \end{bmatrix} \begin{bmatrix} i_{in} \\ v_{cr} \\ v_{SS} \\ v_{CC} \\ i_{L1} \\ i_{L2} \\ v_{cp} \\ v_{cn} \end{bmatrix} \tag{3.28}$$

The corresponding average model is derived by merging the matrices of states 1 and 2 using the state space averaging technique, which takes into account the relative contribution of each state of operation to the total duty cycle D. Therefore, the state space averaged model can be formulated as follows:

$$A_{avg} = DA_{\text{state1}} + (1-D)A_{\text{state2}}$$

$$B_{avg} = DB_{\text{state1}} + (1-D)B_{\text{state2}}$$

$$C_{avg} = DC_{\text{state1}} + (1-D)C_{\text{state2}}$$

Thus, the two state-space representations are averaged over the two states during the switching period t_s, yielding the following averaged state-space matrices. Where:

$A_{\text{avg}} =$

$$\begin{pmatrix} 0 & D{-}1/L_n & 0 & D{-}1/L_nN & 0 & 0 & 0 & 0 \\ -(D{-}1)/C_r & 0 & 0 & 0 & -DN/C_r & -DN/C_r & 0 & 0 \\ -C_p(D{-}1)/(N{*}(C_CC_p{+}C_CC_S{+}C_pC_S)) & 0 & 0 & 0 & -D/C_S & 0 & 0 & 0 \\ -(D{-}1)C_p{+}C_S/(N{*}(C_CC_p{+}C_CC_S{+}C_pC_S)) & 0 & 0 & 0 & 0 & -D/C_C & 0 & 0 \\ 0 & DN/L_1 & D/L_1 & 0 & 0 & 0 & D{-}1/L_1 & 0 \\ 0 & DN/L_2 & 0 & D/L_2 & 0 & 0 & 0 & -1/L_2 \\ -C_S(D{-}1)/(N{*}(C_CC_p{+}C_CC_S{+}C_pC_S)) & 0 & 0 & 0 & 0 & 0 & -D/C_pZ & -D/C_pZ \\ 0 & 0 & 0 & 0 & 0 & 1/C_n & -1/C_nZ & -1/C_nZ \end{pmatrix}$$

$B_{\text{avg}} =$

$$\begin{pmatrix} 1/L_n & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{pmatrix}^T$$

$C_{\text{avg}} =$

$$\begin{pmatrix} 0 & 0 & 0 & 0 & 0 & 0 & -1 & 1 \end{pmatrix}^T$$

It is possible to acquire the S-domain transfer function of the DISC converter, which is also referred to as the line-to-output, and its expression can be determined using the following:

$$G(s) = C_{\text{avg}}(sI - A_{\text{avg}})^{-1}B_{\text{avg}} \tag{3.29}$$

The average model of the DISC converter is a seventh-order transfer function, which

can be described by the following equation. This function has five zeros and seven poles.

$$G_{DISC}(s) = \frac{a_5 s^5 + a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0}{b_7 s^7 + b_6 s^6 + b_5 s^5 + b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_0} \tag{3.30}$$

As shown from Eq3.30, the existence of an uncontrollable state variable is implied by the 7th-order transfer function due to pole-zero cancellation. Where a_5,..a_0, and b_7,..b_0 are the coefficients in the numerator and denominator, respectively, whose values are dependent on the DISC converter parameters. As expected, the steady-state voltage gain ratio of the SM can be given using the following formula:

$$\lim_{s \to 0} G(s) = \frac{V_O}{V_{in}} = \frac{2ND}{1 - D} \tag{3.31}$$

3.5 Design and parameter selection

Following the completion of the dynamic representation of the proposed DISC converter in either of its two operational states, a set of design requirements can be established, including equations that describe the sizes of the passive elements. The DISC converter was analysed in both states to derive equations of the voltages across and currents through the various passive components. The concepts of inductor volt-second balance and capacitor charge balance both hold steady-state operation. This means that the changes in the currents and voltages of the inductors and capacitors during state 1 must be the exact opposite of those observed during state 2. Thus, it is possible to derive formulae for inductances and capacitances as functions of other known parameters by applying equations from one of these states in combination with the inductor and capacitor formulas ($V = L\frac{di}{dt}$ and $I = C\frac{dv}{dt}$).

3.5.1 Input inductor design

As the input side of the converter is connected to a PV module, the ripples in the input current must be reduced as much as possible to maintain the operation at the maximum power point (MPP). The design considers the DISC converter with ideal passive components (i.e., zero equivalent series resistance (ESR)), which allows total efficiency to be calculated under the best-case situation. On the other hand, it is the worst-case scenario for the current ripples through the inductor. This is done to guarantee that the ripples caused by the current will never exceed the maximum permissible level.

In state1, the voltage measured across L_n was defined by Equation 3.5, which can also be rewritten as:

$$L_n = \frac{Dt_s}{V_{in} di_n} \tag{3.32}$$

Where t_s is the total switching period and the maximum ripple in inductor current $\Delta I\%$ can be expressed as a function of the average input current i_n as:

$$di_n = \Delta I\% * i_n \tag{3.33}$$

To simplify, the duty cycle ratio D can be written as a function of known parameters such as the output voltage V_O and the output power P_{out}, so Equation 3.32can be re-arranged as follows:

$$L_n = \frac{V_O V_{in}^2 t_s}{2N\left(V_{in} + V_O\right) P_{out} \Delta \mathrm{I_{in}}\%} \tag{3.34}$$

3.5.2 Output inductors design

Given that the circuit is in state 1, it is possible to derive the parameters of the output inductors. Using Equations 3.9 and 3.10, the values of the output inductors L_1 and L_2 can be determined.

$$L_1 = \frac{(NV_{cr} + V_{SS})\, Dt_s}{di_{L1}} \tag{3.35}$$

$$L_2 = \frac{(NV_{cr} + V_{SC} - V_{cn})\, Dt_s}{di_{L2}} \tag{3.36}$$

It is possible to design L_1 and L_2 from an expression for the voltage across the output inductors in terms of other known parameters. First, if it assumes that the input voltage V_{in} is the same as the sum average voltage across the primary V_{cr} and SEPIC V_{SS} capacitors, it can use the following equation to find the value of L_1:

$$L_1 = \frac{NV_{in}Dt_s}{di_{L1}} \tag{3.37}$$

Similarly, in the calculation L_2, the total average voltage of the primary V_{cr} and the Cuk capacitor V_{SC} is twice the input voltage, whereas the negative output voltage V_{cn} is equal to the input voltage. Hence, the corresponding value of L_2 can be given by:

$$L_2 = \frac{NV_{in}Dt_s}{di_{L2}} \tag{3.38}$$

Then, the output inductors can be designed based on the following substitutions

using known parameters in place of D and $\Delta I\%$ as follows:

$$L_1 = L_2 = \frac{V_{\text{in}}\, V_o^2 t_s}{2\,(V_{\text{in}}\, + V_O)\, P_{\text{out}}\, \Delta I_{L_{1,2}}\%} \tag{3.39}$$

3.5.3 Primary and Secondary Capacitors design

During state 1, the design of the primary capacitor C_r can be derived from Equation 3.6 and is presented as:

$$C_r = \frac{N\,(i_{L1} + i_{L2})\, D t_s}{dV_{cr}} \tag{3.40}$$

Upon closer observation, state1 reveals that the input current i_n is equivalent to the sum of the average currents that are flowing through the primary capacitor. As a result of this, it is possible to rewrite Equation 3.40 as:

$$C_r = \frac{N i_n D t_s}{dV_{cr}} \tag{3.41}$$

The previous equation can be simplified and yields the following calculation for the primary capacitor C_r:

$$C_r = \frac{V_O P_{\text{out}}\, t_S}{2\,(V_{in} + V_O)\, V_{in} \Delta V_{cr}\%} \tag{3.42}$$

Where $\Delta V\%$ is the allowed voltage ripple range used to establish the design formulas for each capacitor. Applying the same strategy of assuming an equation for the currents flowing in the secondary capacitors C_s and C_c in terms of other known parameters, it is possible to substitute i_{L1} and i_{L2}, which have a value that is on average equal to the output current i_o.

$$C_s = C_c = \frac{i_o D t_s}{dV_{ss,cc}} \tag{3.43}$$

As D is a function of both the output voltage V_O and the power P_{out}, selecting secondary capacitors can be accomplished by taking into account the following factors:

$$C_S = C_C = \frac{P_{out} t_s}{2N\left(V_{in} + V_O\right)\Delta V_{SS,SC}\%} \tag{3.44}$$

3.5.4 Design of Output Capacitors

The following formulas can be used to obtain the appropriate sizes for each of the output capacitors:

$$C_p = \frac{i_{cp} D t_s}{dV_{cp}} \tag{3.45}$$

$$C_n = \frac{i_{cn} D t_s}{dV_{cn}} \tag{3.46}$$

The observation reveals that the average current in C_p is equal to i_o, whereas the average current flowing through the negative output capacitor C_n is zero. Thus, it is possible to use a small capacitor at a negative output terminal. Here, the following formulation can be used to describe output capacitors:

$$C_p = \frac{i_o D t_s}{dV_{cp}} \tag{3.47}$$

$$C_n = \frac{D t_s}{dV_{cn}} \tag{3.48}$$

Usually, the converters are designed based on their output power and voltage. Therefore, the calculation is defined in terms of these two quantities. It is possible to

derive the values for C_p and C_n using the following expression:

$$C_p = \frac{P_{\text{out}}\, t_s}{2N\,(V_{\text{in}} + V_O)\,\Delta V_{Cp}\%} \tag{3.49}$$

$$C_n = \frac{V_o t_s}{2N\,(V_{in} + V_O)\,\Delta V_{CN}\%} \tag{3.50}$$

3.6 Simulation Results

The DISC converter has been modelled and investigated in open-loop operation. The system is simulated using MATLAB/Simulink software to study the performance with a passive load. The specifications of the converter are listed in Table3.2.

The simulation has been performed with "ideal" components, which means that the inductors, capacitors, and switches have no resistance. The set of simulation results demonstrates that the proposed DISC has two modes of operation: dc/dc and dc/ac. In addition, these waveforms are presented to validate the different derivations and explanations given so far in this chapter.

3.6.1 dc/dc mode

The DISC converter is operated in the dc/dc mode with a duty cycle of $D = 0.5$. The continuous input current with low ripple guarantees the PV module operates close to its MPP and extracts the maximum available power, as shown in Fig 3.7.

Parameter	Value
Input voltage V_{in}	100v
Grid frequency f_o	50 Hz
Switching frequency f_s	20 KHz
Load resistor	$30\,\Omega$
Inductors	$L_n = 1.5$ mH and $L_1 = L_2 = 1$mH
Primary and secondary capacitors	$C_r = C_S = C_C = 10\mu$ F
Output capacitors	$C_n = 10\mu$ F and $C_p = 50\mu$ F
Transformer turns' ratio	$N = 1$
Input current ripple	$\Delta \mathrm{I_{in}}\% = 10\%$
Output current ripple	$\Delta I_{L_{1,2}}\% = 20\%$
Voltage ripple of primary and secondary capacitors	$\Delta V_{SS,SC}\% = 10\%$
Voltage ripple of output capacitors	$\Delta V_{C_p,C_n}\% = 5\%$

Table 3.2: Circuit parameters of DISC converter.

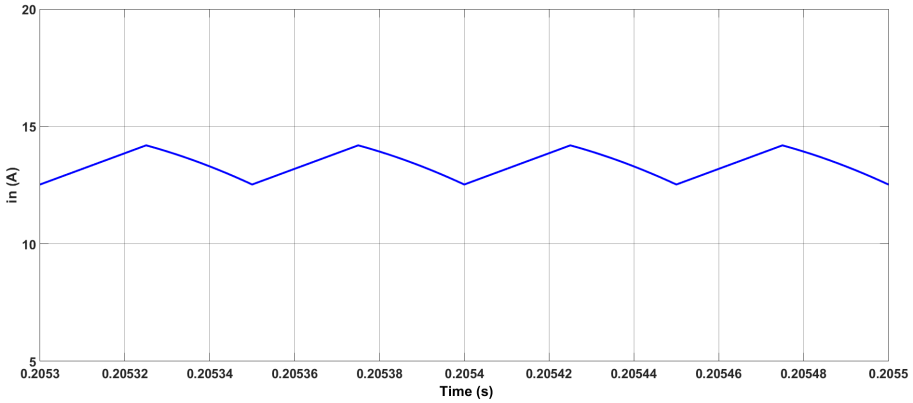


Figure 3.7: Input current dc/dc mode.

Both output inductor currents are presented in Fig 3.8, which are identical, and their average value corresponds to half the average input current. The flow of the secondary currents through the sepic and cuk capacitors is plotted in Fig 3.9, and their average values are both zero.

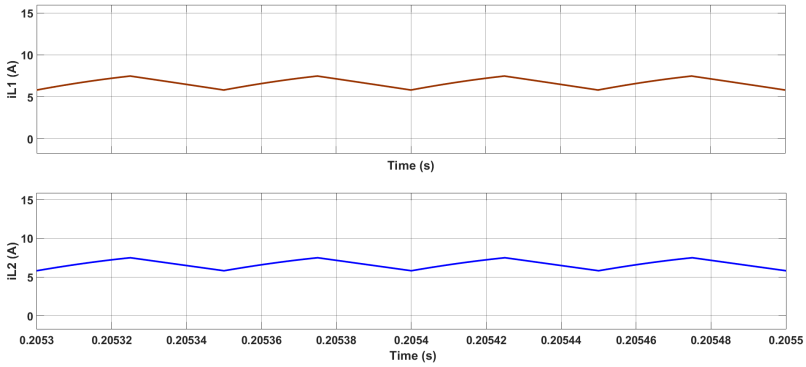


Figure 3.8: Output inductor currents.

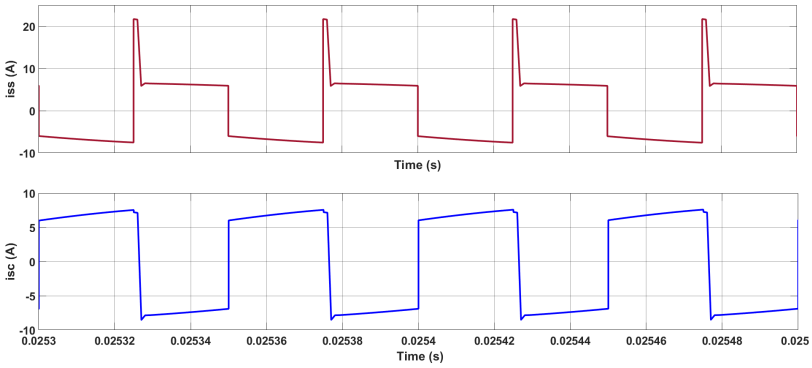


Figure 3.9: Secondary currents.

On the other hand, the voltage measurement over the primary and secondary capacitors is provided in Fig 3.10. The dual-polarity voltage output of the proposed DISC converter is presented in Fig 3.11, where the sepic output is positive and the cuk output is negative. Fig 3.12 shows the waveforms of the output voltage and current respectively.

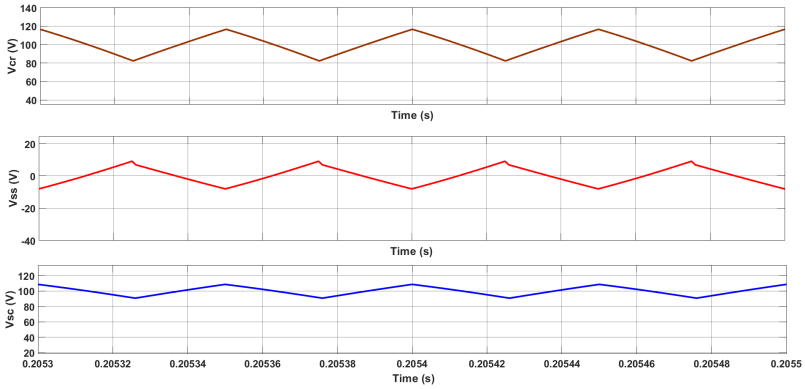


Figure 3.10: Measured transfer capacitor voltage.

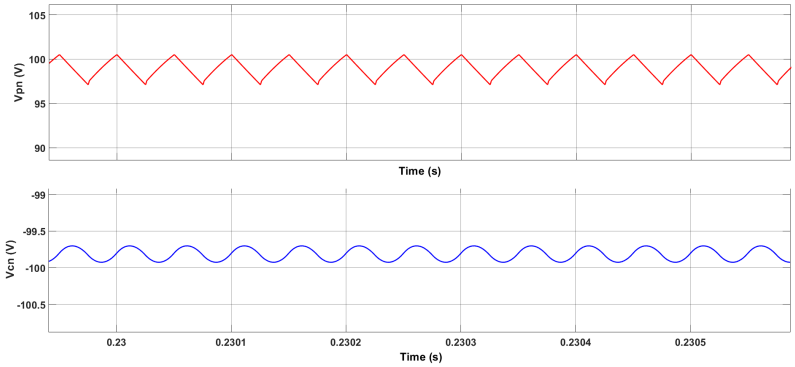


Figure 3.11: Output dual voltage.

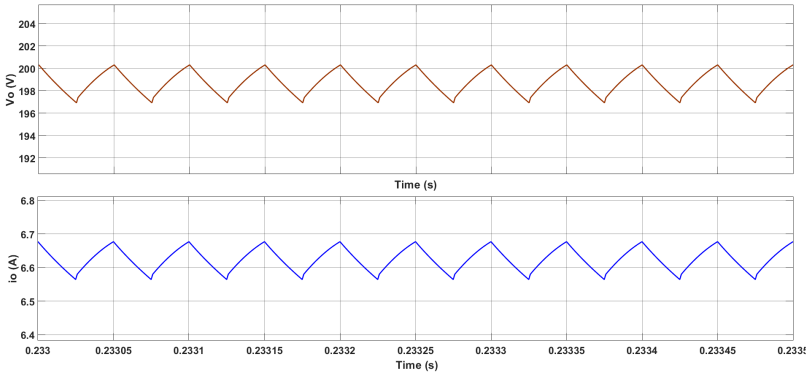


Figure 3.12: Voltage and current output.

Fig 3.13 compares the mathematical model and switching model to validate the state space average model during states 1 and 2.

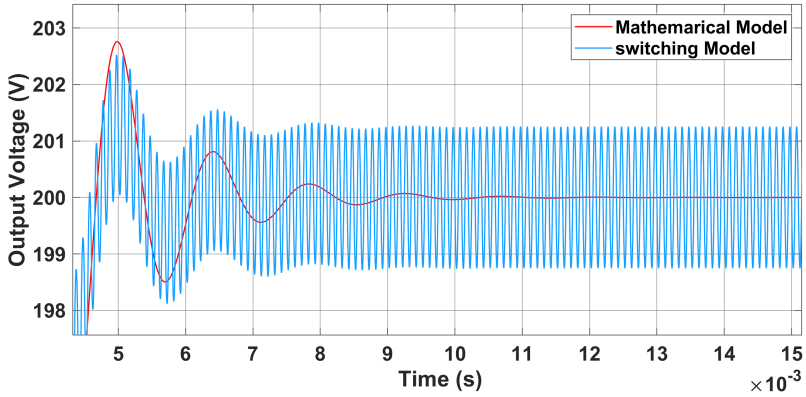


Figure 3.13: DISC converter dynamics from the switching model and state space average model.

3.6.2 DC bias mode

The DISC operates in the DC bias mode by applying the SPWM modulation strategy described in 3.2. Fig 3.14 represents the output voltage and current, and Fig 3.15 shows the duty-cycle ratio that corresponds to the output voltage and current and is responsible for the operation of the converter.

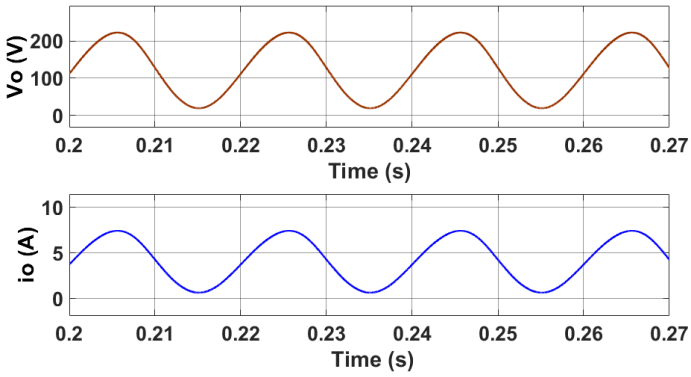


Figure 3.14: Output voltage and current.

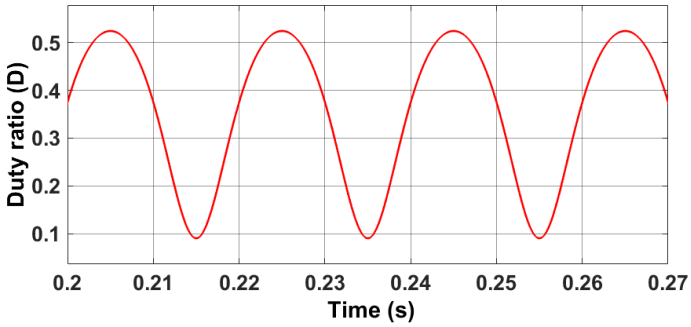


Figure 3.15: Duty-cycle ratio.

The input current with continuous operation is presented in Fig 3.16, which is desirable for MPPT controllers in PV systems. As can be seen in Fig 3.17, the currents flowing through the two output inductors i_{L1} and i_{L2} are similar, and each has a magnitude that is exactly half that of the input current. Currents are flowing through the capacitors of SEPIC and Cuk, which are estimated based on the ratio ρ, as found in Fig 3.18.

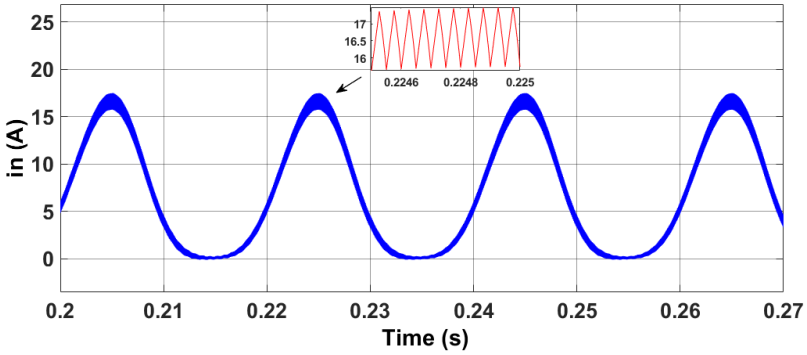


Figure 3.16: Input current.

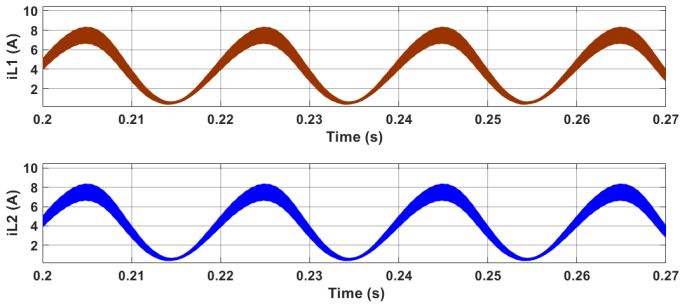


Figure 3.17: Currents flowing through output inductors.

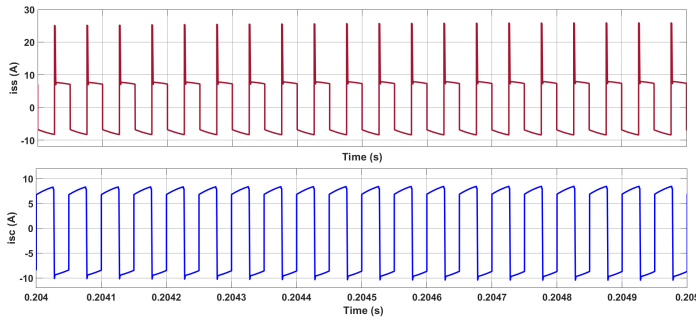


Figure 3.18: Currents flowing through Sepic and Cuk capacitors.

Voltages measured across all three transfer capacitors (i.e., C_r,C_s, and C_c) are shown in Fig 3.19 together and mostly follow each other. It is important to note that the average voltage across the primary capacitor C_r equals the input voltage, whereas the average voltage across the Sepic capacitor C_s is zero equal to the average voltage across the transformer therefore, a small capacitor can be employed. The average voltage of the Cuk capacitor C_c corresponds to the input voltage. The dual output of the DISC converter is shown in Fig 3.20, and it is shown as being positive at the Sepic output terminal and negative at the Cuk output terminal.

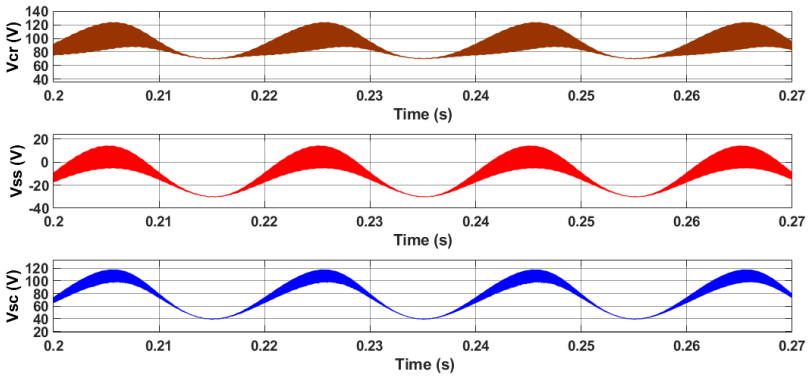


Figure 3.19: The voltage across the transfer capacitors.

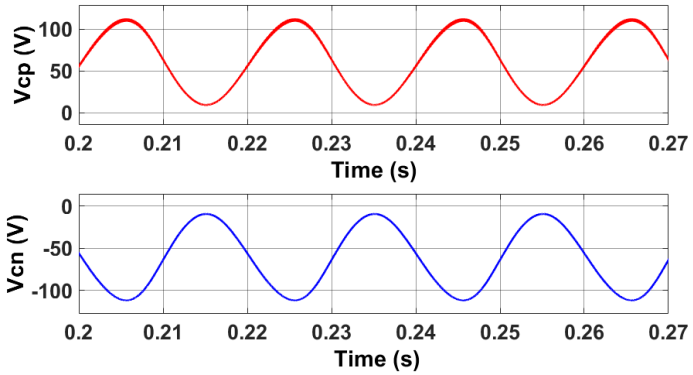


Figure 3.20: The dual output voltage.

3.7 Chapter Conclusion

This chapter introduced the DISC converter and discussed its performance. The chapter began with the novel DISC structure, which included an HFT with one primary winding and dual secondary windings for galvanic isolation and voltage boosting. It is a promising solution for PV systems with remarkable features such as high gain and the capability of providing both step-up and step-down voltages. In addition, it has a continuous input current to allow the use of a small film

capacitor instead of a bulky electrolytic capacitor. The modulation technique used to generate gate signals for switches was developed. Then, the operation of the DISC converter was analysed, along with a description of the input-to-output energy transfer process for each of the two states. Moreover, a mathematical analysis and a state-space model of the DISC's operation are derived and examined to shed light on the DISC's operational features. Following the theoretical investigation of the converter, the procedure for designing the DISC was described. Based on the performance requirements, equations were derived for sizing each of the converter's passive components. In conclusion, simulation results were presented to validate the proposed DISC operation in dc/dc and dc/ac modes, as well as their associated theoretical analysis.

Chapter 4

A Three-Phase Modular Inverter (TPMI) Topology

The configurations of LSPV plants have undergone significant development in recent years. As more PV generation plants are connected to the grid and the use of electric vehicles and associated energy storage systems increase, it is crucial to improve the energy conversion of PV sources. Therefore, many research efforts have been directed to various inverter topologies that can manage additional power through power scaling without increasing the complexity of the LSPV design. In this regard, modular isolated inverter topologies can perform this role effectively. The most important aspect of the modular isolated inverter is their operation comprised between MLCs and string inverters, as discussed in several scholarly publications [32], [50], [108].

In this context, the modular isolated inverters based on power converters as their SMs stand out as a possible solution to improve the performance of LSPV systems. [33], [121]. Because of their unique structure, they can meet several requirements listed in Chapter 2 for LSPV power converters. They are single-stage power circuits

with many possible topologies. Multiple converters can be connected in parallel or series on the input, output, or both sides. With such a system, decentralised control is possible, where each SM converter can have individualized control objectives [148]. In addition, they offer the benefits of allowing the installation of an independent MPPT controller for every input port, galvanic isolation, and bidirectional energy flow in PV applications. [34].

This chapter aims to introduce a novel TPMI based on the DISC converter for a grid-tied system. The inverter will operate at high power of LSPV systems and will be connected to the utility grid in the United Kingdom at 230 VAC and 50 Hz. The TPMI structure provides a high output voltage with low-voltage rating SMs, and each SM can perform independent MPPT control. The DISC SM has desirable characteristics for LSPV applications because it can provide a high step-up ratio, galvanic isolation, low input current ripple, and a wide range of input voltages. The specifications, analysis, and design of the TPMI topology are the main focus of Chapter 4. This chapter provides a comprehensive description of TPMI by focusing on its main modulation method, its operation, and its control strategy for delivering high power to the grid. MATLAB/Simulink results are used to validate the performance and functionality of the TPMI using simulation models. Then, experimental verifications on a downscaled prototype controlled by the TMS32028335 DSP are presented.

4.1 Topology Structure

A simplified block diagram of a PV system connected to the grid based on TPMI is shown in Fig 4.1. The proposed TPMI is formed by several symmetrical SMs based

on the DISC converter, as presented in Chapter 3, where it is possible to increase or decrease the power levels by connecting or disconnecting the basic SM units. The simplest version of TPMI has two DISC SMs for each phase that is responsible for power processing.

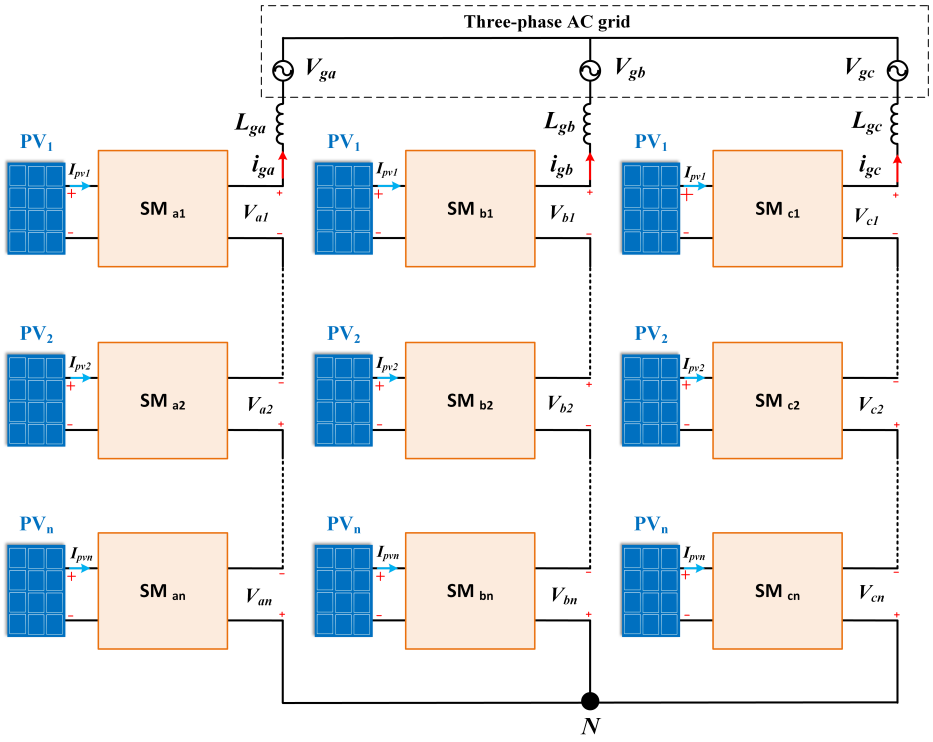


Figure 4.1: Modular a grid-connected TPMI topology.

The SMs of the TPMI are connected independently at the input and connected in series at the output to conform to the MVAC grid requirements. This form of connection is known as an input-independent and output-series (IIOS) connection, and it can be considered a way of achieving a high voltage conversion ratio. As the proposed inverter is designed for grid-connected applications, it interfaces with the grid via three-phase line inductors (L_{ga}, L_{gb}, and L_{gc}) with internal resistances (r_{ga}, r_{gb}, and r_{gc}). Compared to the conventional LSPV configurations, the TPMI structure

offers some impressive advantages, which can be summarised as follows:

(i) The uniform operation of TMPI allows modularity with plug-and-play functionality and can be easily expanded and scaled to higher power levels by just adding more SMs. Consequently, the inverter can be directly connected to the MVAC grid without a bulky LFT.

(ii) The modular structure of the TPMI ensures that even if a single PV module fails, the entire output power will not be lost. In addition, it possesses fault-blocking capabilities in the event of a dc or ac power breakdown. So, it is possible to forward or replace SMs if they fail for any reason, which can significantly increase the PV system's reliability.

(iii) The modularity of the inverter's device structure allows the use of low-state resistance active switches, which decreases conduction loss and increases reliability.

(iv) Each DISC SM is connected to a PV module with its MPPT controller; consequently, with its distributed MPPT operation, it is possible to yield the maximum possible energy under both uniform and non-uniform partial shading environments.

(v) A HFT can be embedded in the SM to provide galvanic isolation and reduce leakage current, common mode voltage (CMV), and electromagnetic interference (EMI). Due to its high switching frequency, it can be compact. Additionally, it can readily contribute to input voltage boosting or bucking.

(vi) DISC-based SMs have a continuous input current; therefore, it is possible to

filter the input PV system using a compact film capacitor instead of a bulky electrolytic capacitor, which results in a longer inverter life.

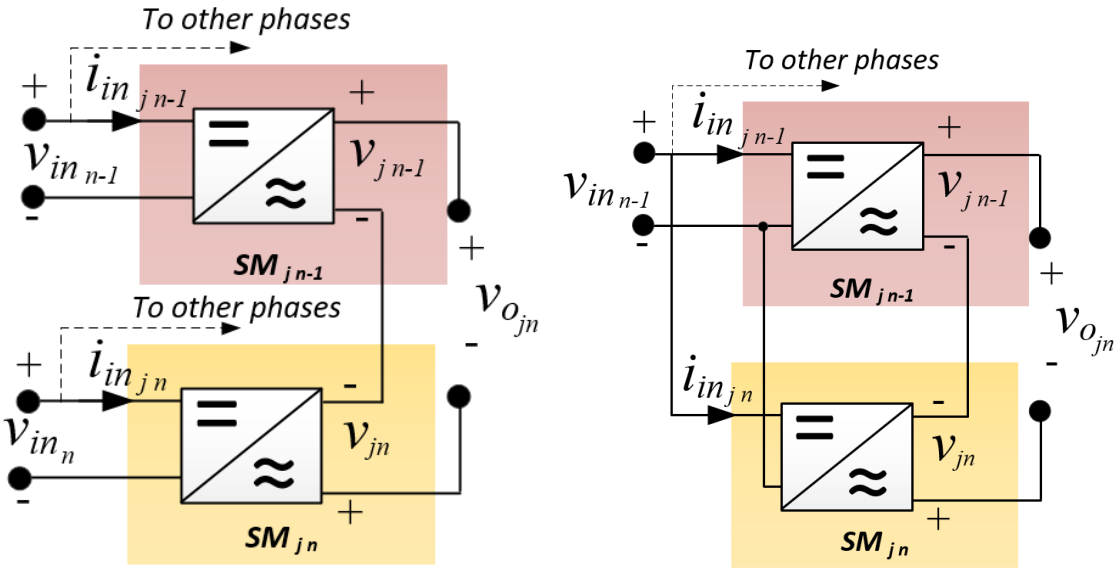
(vii) Simple DSP control boards can be used to implement the control technique, which can reduce the complexity and cost of the inverter.

4.2 Modulation Strategy

There are two possible connections between the SMs in phase j and the PV modules, as shown in Fig 4.2. In the first method, separate PV modules are connected to each SM to reduce the current of each PV module. In the second method, the same PV module is connected to the successive SMs to ease the input connection but at the expense of increased input current. The output ac voltage and current from the SMs will be the same in both connections. In phase j, the output voltages of SM_{n-1} and SM_n can be represented as:

$$\begin{aligned} v_{jn-1}(t) &= \frac{1}{2}V_{jn-1}\sin(\omega t) + V_{dcjn-1} \\ v_{jn}(t) &= \frac{1}{2}V_{jn}\sin(\omega t + \pi) + V_{dc\ jn} \end{aligned} \tag{4.1}$$

Both V_{jn-1} and V_{jn} are AC output voltages, whereas V_{dcjn-1} and $V_{dc\ jn}$ are common DC offsets for the connection of SM_{n-1} and SM_n.



(a) Different PV modules. (b) Same PV modules.

Figure 4.2: Connecting the successive SMs in phase j with the PV modules.

The DC offsets and magnitudes of the AC components are equal at the connection of two successive SMs. Then, their DC offsets were cancelled out by each other, and their total output voltage is:

$$v_{ojn}(t) = v_{jn-1}(t) - v_{jn}(t) = V_{jn}\sin(\omega t) \tag{4.2}$$

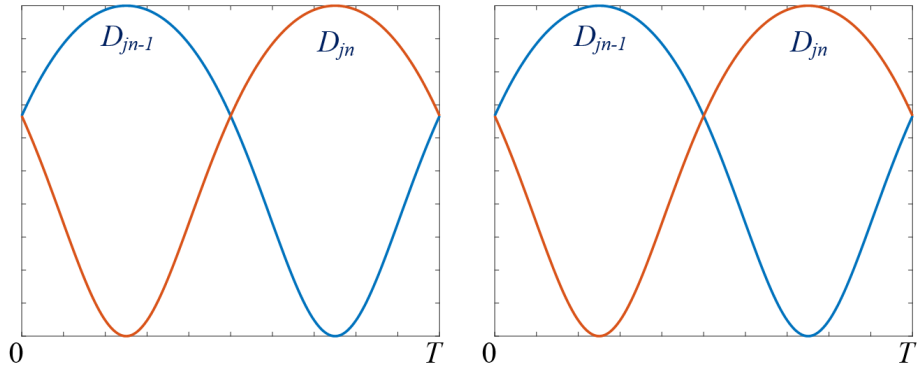
The duty-cycle ratios for successive SMs, which generate an AC output voltage with a common DC offset, are calculated as follows:

$$\begin{aligned} D_{jn-1}(t) &= \frac{v_{jn-1}}{v_{jn-1} + 2NV_{inn-1}} \\ D_{jn}(t) &= \frac{v_{jn}}{v_{jn} + 2NV_{inn}} \end{aligned} \tag{4.3}$$

The SM input currents for both connections can be expressed as follows:

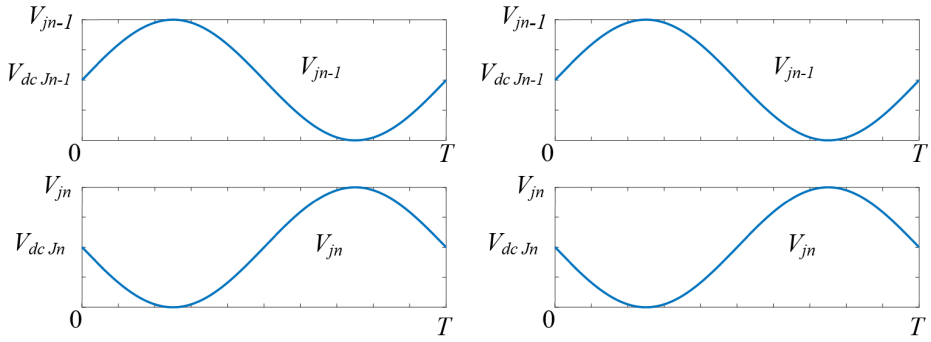
$$\begin{aligned} i_{injn-1}(t) &= 2N\frac{D_{jn-1}}{1-D_{jn-1}}i_{gj} \\ i_{injn}(t) &= -2N\frac{D_{jn}}{1-D_{jn}}i_{gj} \end{aligned} \tag{4.4}$$

The figures below show the waveforms of the duty-cycle ratios, voltages, and currents for the first and second connections of SMs.



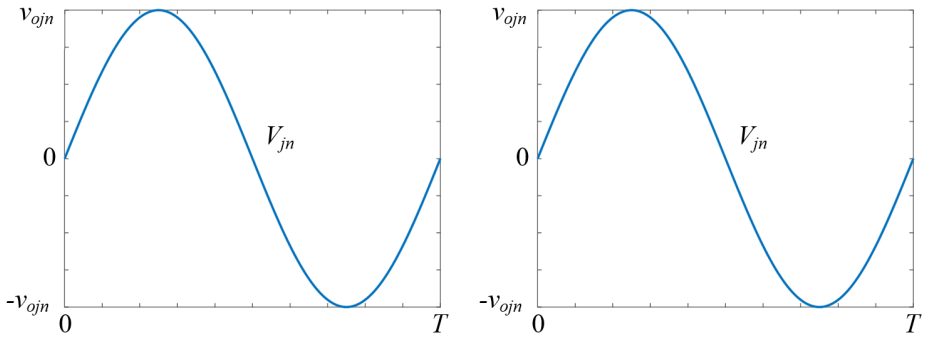
(a) First connection. (b) Second connection.

Figure 4.3: Duty cycles.



(a) First connection. (b) Second connection.

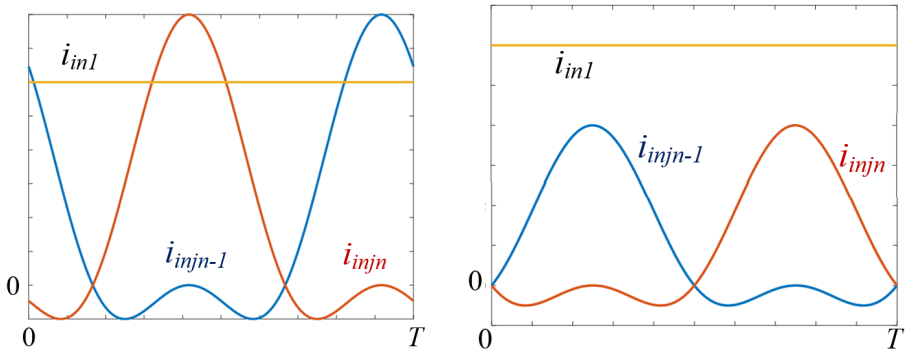
Figure 4.4: Two successive SM voltages.



(a) First connection. (b) Second connection.

Figure 4.5: The output voltage at the common point.

It is worth noting that the total input current from the PV modules to provide the three phases will be doubled in the second connection shown in Fig 4.6, as each PV module will feed six SMs (i.e., two SMs in each phase) in this case.



(a) First connection. (b) Second connection.

Figure 4.6: The input currents

4.3 Modular DC/AC Operation

The TPMI-based system is presented in Fig 4.1, where the output voltages of the series n SMs (V_{o1} to V_{on}) are summed to provide the total per-phase output voltage

at the point of common coupling (PCC), which can be expressed as follows:

$$V_{PCC} = V_{o1}\sin(\omega t + \theta_1) + V_{o2}\sin(\omega t + \theta_2) + V_{on}\sin(\omega t + \theta_n) = \sum_{i=1}^{n} v_{oi} = V_o \sin(\omega t + \theta) \tag{4.5}$$

As demonstrated in Equation4.5,V_o and θ are the magnitude of the output voltage of the SMs and the phase-shift angle, respectively. The output voltages of the SMs have the same magnitude and phase angle values as the following:

$$\begin{aligned} V_{o1} = V_{o2} = ... = V_{on} \\ \theta_1 = \theta_2 = ... = \theta_n \end{aligned} \tag{4.6}$$

Assuming the normal operation when the active power is distributed evenly among the SMs, the grid current of each phase can be represented as follows:

$$i_g(t) = \frac{n\left[V_o \sin(\omega t + \theta)\right] - V_g \sin(\omega t)]}{Z_g} \tag{4.7}$$

Where V_g is the peak value of the ac grid voltage. Here n and Z_g denote the number of DISC SMs present in each phase and the grid impedance. This operation is balanced and identical, as all three phases produce the same voltages and currents. The only difference is the addition of a 120-degree phase shift to each phase. Thus, the three-phase voltages and currents can be written as

$$\begin{aligned} v_{oj}(t) &= V_o \sin(\omega t + \varphi_j) \\ i_{oj}(t) &= I_o \sin(\omega t + \varphi_j - \gamma) \end{aligned} \tag{4.8}$$

In these equations, j and I_o represent phase a, b, or c, and the peak value of TPMI output current, respectively, while γ indicates the phase-shift angle of the output currents and $\varphi_j = \{0, -2/3\pi, 2/3\pi\}$.

On the other hand, the power of one DISC SM per phase can be written as follows:

$$P_{SM} = V_{in} I_{in} \approx \frac{3 V_o I_o \cos(\theta - \gamma)}{4} \tag{4.9}$$

In addition, the total output power of the TPMI system can be determined by disregarding the power loss in the cable resistance as follows:

$$P_{total} = \frac{3n V_o I_o \cos(\theta - \gamma)}{4} \tag{4.10}$$

If the targeted operating point is known from the MPPT calculations at the optimal points (V_{in}, I_{in}, and P_{SM}), as shown in Fig 4.7, then the TPMI reference voltages and currents can be determined using equations 4.7,4.9, and 4.10.

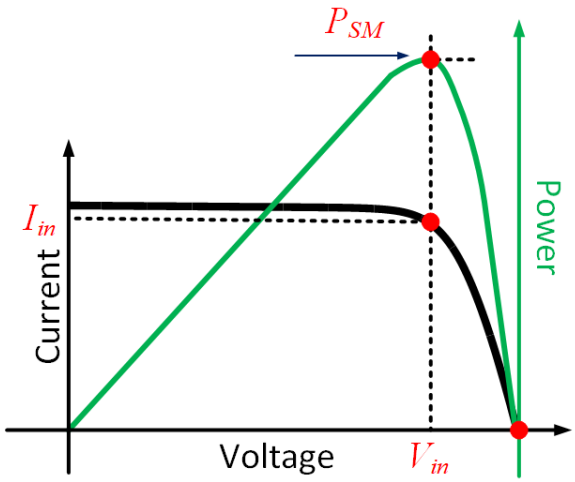


Figure 4.7: Operational points on the PV curves.

4.4 Control architecture

This section will discuss the control system employed in the proposed TPMI topology when operating as an inverter and transferring energy from PV modules to the utility grid. In this architecture, two levels of control are designed to regulate the grid's voltage and current. The first part is referred to as a system-level controller and is responsible for generating the total voltage from all series SMs [149]. This control loop is designed to be slower than the second SM-level controller, which is the part that is responsible for fine-tuning the voltage of each SM individually [150]. The commands of both controllers will lead to an improvement in the dynamic response of the TPMI system.[32].

It is worth noting that the MPPT control itself is not in the scope of this Ph.D. thesis. In this study, it was assumed that the MPPT approach works and can find the reference values of the SM output voltages. In the following subsection, further

details about the aforementioned controller schemes will be discussed.

4.4.1 System-level control

This control system assumes that all passive components are equal and operate under normal conditions. As shown in Fig 4.8, the TPMI system can be considered as a single central converter that is controlled by a uniform duty-cycle ratio D_{ov} and the same gate drive signals.

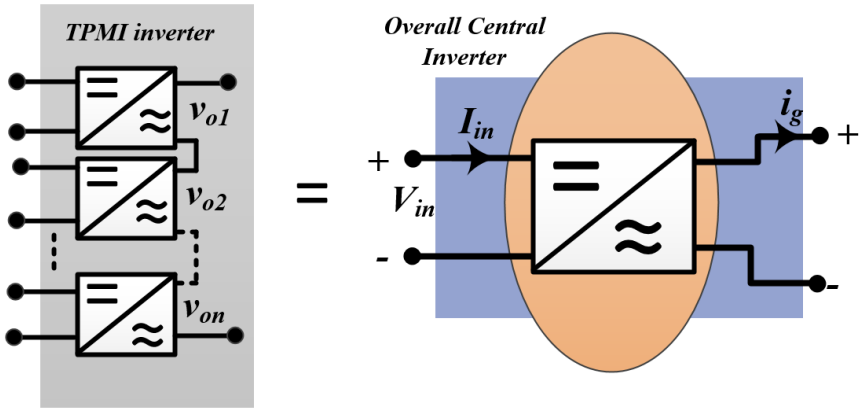


Figure 4.8: Modular series-connected inverter simplification.

In this particular instance, the equivalent circuit of the overall central inverter can be derived by using the assumptions outlined in Table4.1.

TPMI Parameter	Equivalent	Value
Input inductor L_n	L_{nov}	$L_{nov} = L_n$* n
Sepic inductor L_1	L_{1ov}	$L_{1ov} = L_1$* n
Cuk Inductor L_2	L_{2ov}	$L_{2ov} = L_2$* n
Input capacitor C_r	C_{rov}	$C_{rov} = C_r$ / n
Sepic capacitor C_S	C_{Sov}	$C_{Sov} = C_S$ / n
Cuk capacitor C_C	C_{Cov}	$C_{Cov} = C_C$ / n
Positive rail capacitor C_p	C_{pov}	$C_{pov} = C_p$ / n
Negative rail capacitor C_n	C_{nov}	$C_{nov} = C_n$ / n

Table 4.1: Equivalent values of overall inverter passive components.

The overall transfer function can be derived by substituting the equivalent parameters from Table4.1 into Eq.3.30 and is represented as follows:

$$G_{ov}(s) = \frac{a_5 s^5 + a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0}{b_7 s^7 + b_6 s^6 + b_5 s^5 + b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_0} \tag{4.11}$$

The control at the system level is composed of two different control loops, which are both explained in the following subsections:

4.4.1.1 Open-loop controller

The open loop is used to determine the value of the central duty-cycle ratio D_{ff}, which can be computed from the power equation and is fed forward to all SMs as illustrated in Fig 4.9. As discussed previously, the total voltage delivered per phase is obtained from Eq.4.5, while the grid voltage and current can be written as:

$$\begin{aligned} v_g &= V_g \sin(\omega t) \\ i_g &= I_g \sin(\omega t - \gamma) \end{aligned} \tag{4.12}$$

If the three-phase TPMI supplies the active power P to the AC grid with a power factor of $\cos\varphi$, then the magnitude of the output voltage V_o, the phase shift θ, and the magnitude of the output current I_g per phase can be expressed as follows:

$$I_g = \frac{2P}{3V_g \cos(\varphi)} \tag{4.13}$$

$$\begin{aligned} \theta &= \tan^{-1}\left[\frac{r_g I_g \sin(\varphi) + \omega L_g I_g \cos(\varphi)}{V_g + r_g I_g \cos(\varphi) - \omega L_g I_g \sin(\varphi)}\right] \\ V_o &= \left[\frac{V_g + r_g I_g \cos(\varphi) - \omega L_g I_g \sin(\varphi)}{\cos(\theta)}\right] \end{aligned} \tag{4.14}$$

After these variables have been determined, the following formula can be used to compute the feed-forward duty-cycle ratio D_{ff}:

$$D_{ff} = \frac{v_o(t) + V_o}{v_o + V_o + 2nNV_{in}} \tag{4.15}$$

Then, D_{ff} is supplied to each SM in phases a, b, and c, respectively, in order to generate the output voltage v_o.

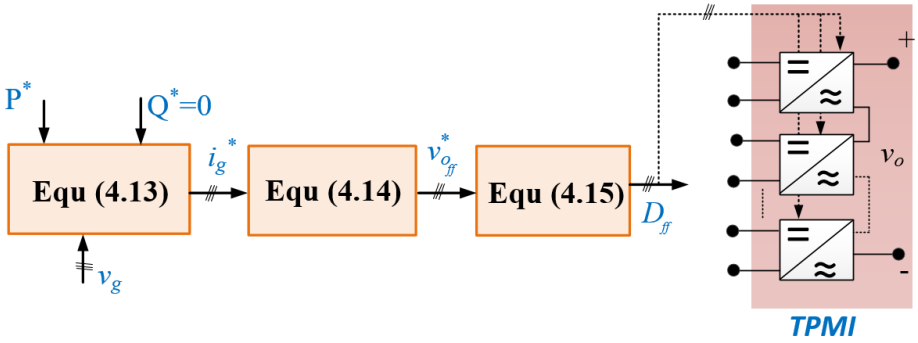


Figure 4.9: System-level control with an open-loop.

4.4.1.2 Closed-loop controller

As aforementioned, the previous control loop was used to operate the TPMI, with this control being responsible for generating the output voltages and, consequently, the output grid current. However, If the values of the passive elements, parasitic resistances, or input voltage differ, the estimated duty-cycle ratio D_{ff} will produce an error in the output grid current.To eliminate this error, an additional controller (i.e., a closed-loop) can be added by its duty-cycle ratio D_{cl}, as shown in Fig 4.10. Thus, a proportional resonant (PR) controller is introduced in the closed loop system. The PR controller controls the output voltage or current directly, without additional frame transformations. The resonant component of the controller offers an infinite gain at the desired frequency, which is tuned to the frequency of interest; thus, the waveforms will be controlled with zero steady-state error[151]. The transfer function of the PR controller in the continuous s-domain can be written as follows:

$$G_{PR}(s) = k_p + \frac{k_r s}{s^2 + \omega^2} \tag{4.16}$$

Here, k_p and k_r represent the proportional and resonant gains of the PR controller

and ω represents the grid angular frequency, which can be tuned at grid frequency ($\omega = 2\pi f_o$)[152].

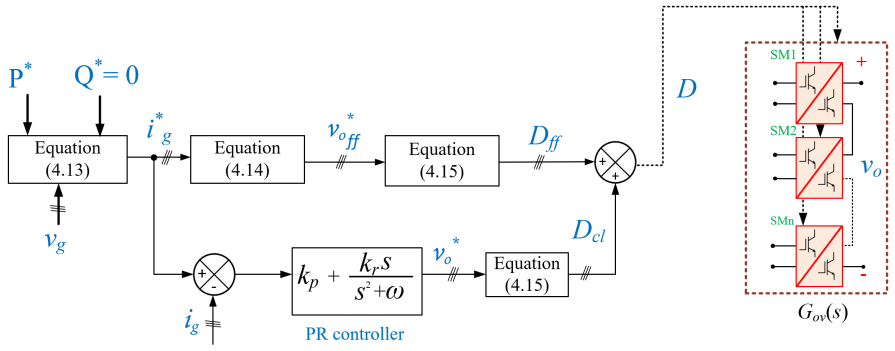
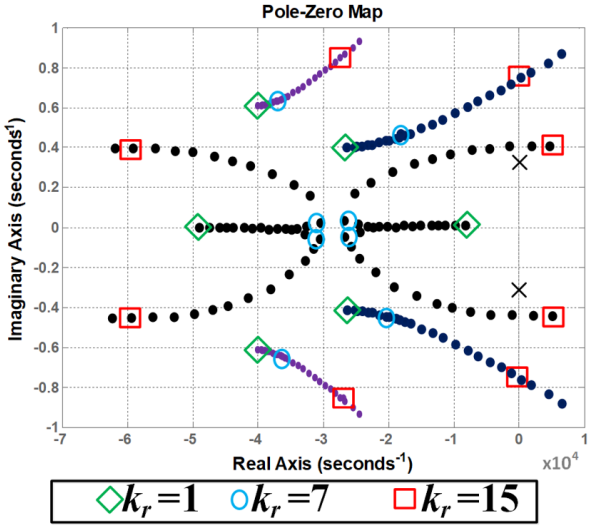


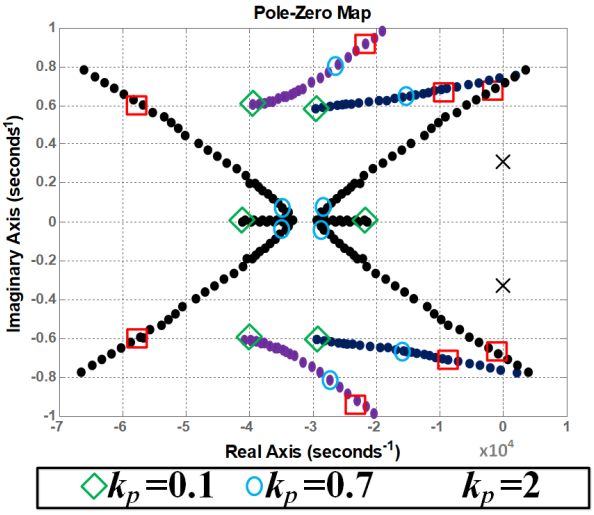
Figure 4.10: System-level control with closed-loop.

To simplify the selection of the PR controller gains k_p and k_r, an average duty-cycle ratio value of $D = 0.5$ is chosen. Additionally, the interactive SISOTOOL toolbox in MATLAB/SIMULINK® is used to pick suitable values for the PR controller gains by plotting the closed-loop system's root loci in two different steps. In the first step, the proportional gain k_p is held at a fixed value of 0.5, while the resonant gain k_r is increased in the range of [1:15]. Second, the value of k_r is held constant at 5, while the range of k_p is shifted from [0.1:2].

Fig 4.11 illustrates the resultant root loci. Gain values are adjusted within these ranges to maintain the stability of the system, maximise the controller's bandwidth, and reduce overshoot. Thus, when $k_p = 0.7$ and $k_r = 7$, the system achieves an acceptable level of performance in terms of bandwidth and stability.



(a) k_p= 0.5 and k_r = [1:15].



(b) k_r= 5 and k_p =[0.1:2].

Figure 4.11: Pole-Zero maps of the system-level controller.

4.4.2 SM-level control

If the SMs are not identical, another control scheme will need to be designed at the SM level to compensate for minor differences in the values of the passive elements

or the operating conditions. Essentially, the SM-level control is designed to contain two different loops, which are the open loop and the closed loop. Since the MPPT algorithms are not the focus of this work, it will be assumed that the MPPT controller is already operational and generates the reference point for each SM. This is because the MPPT algorithms have not been specifically considered. Therefore, the outputs of the MPPT controllers will be the starting point for the control system. More details about both loops are shown in the next subsection.

4.4.2.1 Open-loop

The open loop SM controller shown in Fig 4.12 generates the small-signal duty-cycle ratios for the SMs based on their respective power shares. As all SMs in any phase share the same output current, the output voltages of SM number k (i.e., v_{ok}) will be dependent on the ratio of the power generated by this SM (i.e., p_k) to the total power generated by the full system (i.e., P). As mentioned earlier, the k^{th} SM power reference (i.e., p_{k*}) should come from the MPPT controller, which monitors the operational conditions and knows the power-voltage curves of the PV modules. Thus, the SM voltage output voltage (v_{ok}) is calculated from:

$$v_{ok} = \frac{p_k}{P} v_o \tag{4.17}$$

If the desired output voltage of each SM is known, the feed-forward duty-cycle ratio of k^{th} SM can be obtained as follows:

$$d_{ffk} = \frac{v_{ok}(t) + V_k}{v_{ok} + V_k + 2N v_{ink}} \tag{4.18}$$

Here, V_k is the ac peak value of the SM voltage.

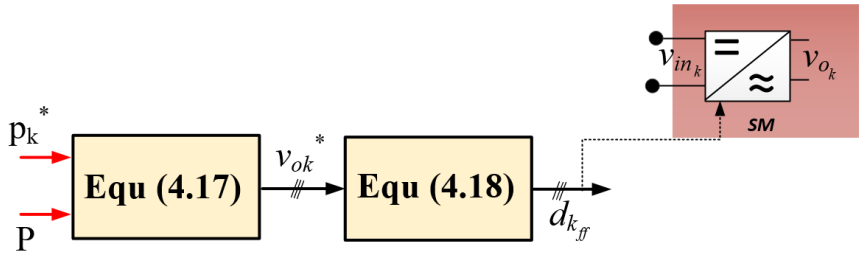


Figure 4.12: SM-level control with an open-loop.

4.4.2.2 Closed-loop

The closed-loop controller that is shown in Fig 4.13 will fix any errors that were made in the open-loop calculations by adding the closed-loop PR controller to the path. The overall controller's technique, which was described earlier when applying the SISOTOOL toolbox, is used in the process of selecting the controller gains.

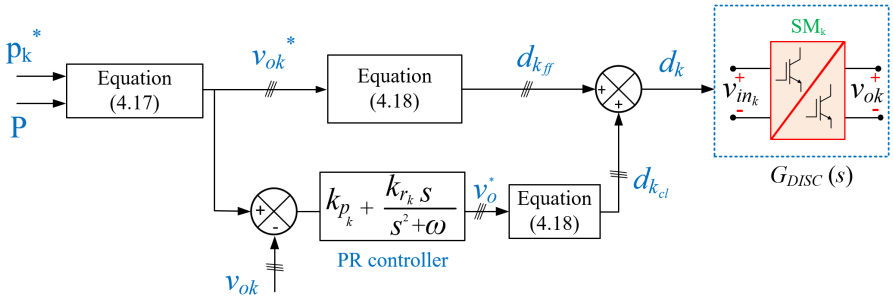


Figure 4.13: SM-level control with closed-loop.

In the computer simulation results in the next section, it will be assumed that all SMs are the same, and since they all have the same values for the passive components, they also all have the same controller gains. Therefore, it has been determined that these gain values, $k_{pk} = 1.2$ and $k_{rk} = 10$, will result in proper system operation.

4.5 Simulation Results

This section presents the results of MATLAB/Simulink models of the TPMI topology when implemented in the LSPV plant, which is connected to the MVAC grid. In these studies, each PV array consisted of 25 AX500W-96M PV modules, where the PV module is rated at 500 W at MPP voltage. These modules were connected in five series and five parallel to meet the voltage and current levels needed to produce 1 MW using 80 PV arrys.

The control approach discussed in the previous section is applied to maintain TPMI stability and guarantee accurate tracking of the output voltages and currents. On the other hand, the MPPT technique is set up in MATLAB/Simulink as a look-up table that generates the new reference current values for the system and SM-level controllers, as shown in Fig 4.14. Thus, the responsibility of the TPMI controller will start after the MPPT to control and track the reference currents.

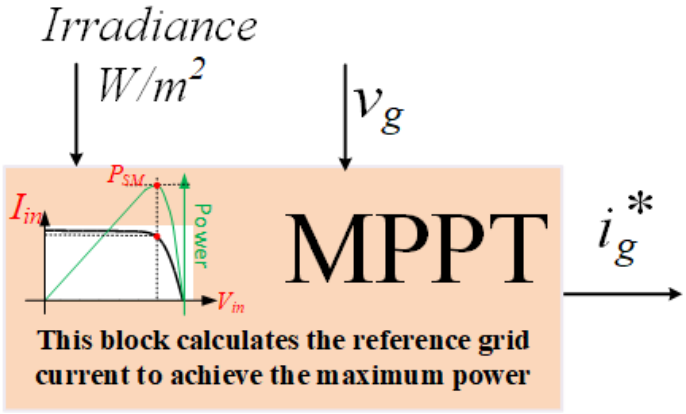


Figure 4.14: MPPT look-up table in the simulations.

Parameter	Value
Number of SMs (n)	80
Selected PV modules	AX500W-96M
Number of PV array	80
PV array	5 parallel $\times$ 5 series
Maximum power, voltage, current operation	500W,48.63V,10.28A
Transformer turns ratio	2
Rated power of the TPMI	1 MW
MVAC grid voltage	13.47 kV
Grid impedance	$L_g = 1$ mH, $r_g = 0.5$
Grid frequency	$f_o = 50$ Hz
SM Switching frequency	20 kHz
SM inductors	$L_n = 1.5$ mH and $L_1 = L_2 = 1$mH
SM Capacitors	$C_r = C_S = C_C = 10\mu$ F
Output capacitors	$C_n = 10\mu$ F and $C_p = 50\mu$ F

Table 4.2: Circuit parameters of the TPMI.

Two case studies are carried out for different TPMI operations, depending on the changing power of the PV modules. These cases are described by various weather conditions associated with different irradiation levels and a constant temperature at 25°C. The first study considers the dynamic response and the capability of the TPMI topology and the control algorithm to deal with sudden changes in solar irradiation. In the second case study, the irradiation level of half of the PV modules is reduced by 50%; thus, the TPMI and power responses are studied in the context of partial shading conditions. Table4.2 has a list of the simulation parameters used in these

studies. The two case studies will be presented in the following subsections.

4.5.1 Case study I: Uniform levels of irradiance

The performance of the TPMI system is evaluated by changing the irradiance level for all PV modules. The first irradiation value, which was 1000 W/m^2 and introduced uniformly for PV modules, resulted in a gradual increase in TPMI's power from zero until it reached its maximum value of 1 MW at t = 0.1 s. At this period, the operation point on the PV curves moves from its initial operating point (p_1) to its maximum possible value (p_2), as illustrated in Fig 4.15.

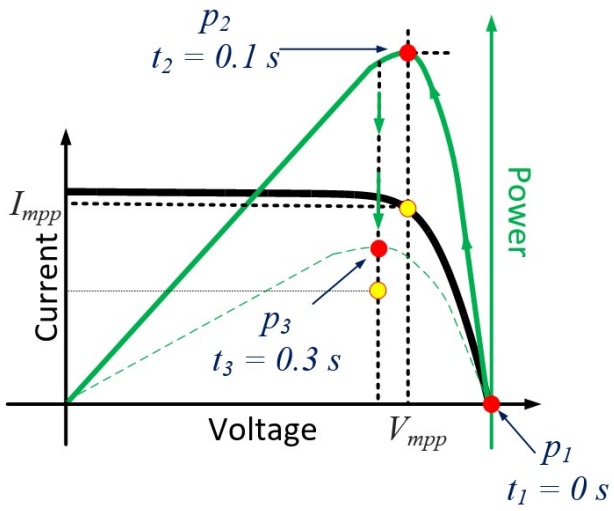


Figure 4.15: Operational points on the PV curves.

At t = 0.3 s, the irradiance level in all PV modules dropped from 1000 W/m^2 to 500 W/m^2. Therefore, the power produced by the TPMI decreased to 0.5 MW. As a consequence, the controller will adjust the phase angle to regulate the output power. This can be accomplished by reducing the AC currents fed into the grid while keeping the output voltages synchronised with the grid. On the other hand, the operational

point will move from its maximum value of (p_2) to the lower point of (p_3).

As demonstrated in Fig 4.16, the irradiation was at the rated level value until t = 0.3, when it decreased by half. Fig 4.17 shows the output power of the TPMI from the 80 PV arrays reaches 1 MW before falling to 50% at t = 0.3s.

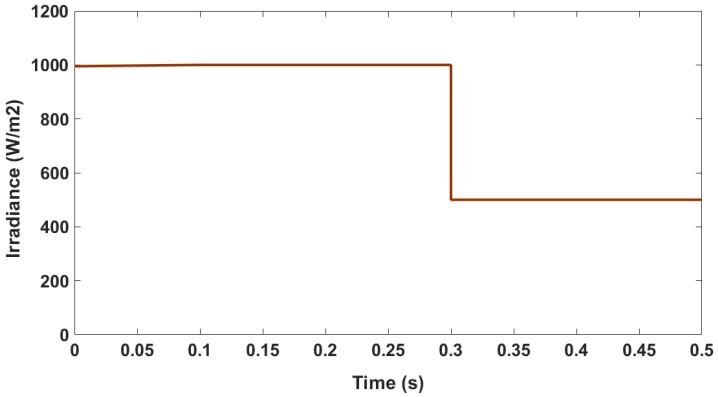


Figure 4.16: Irradiation Level.

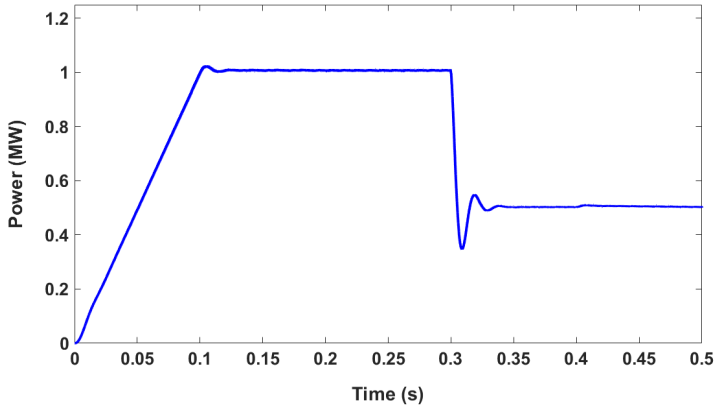


Figure 4.17: Output power of TPMI.

Fig 4.18 presents the three-phase output voltage of the TPMI at PCC with the MVAC grid and the output current of the TPMI injected into the grid when the power factor is controlled at unity. The phase angle is reduced at 0.3 sec because the output

power is reduced. Moreover, the phase angle change depends on the value of the grid inductance L_g. Therefore the angle is changed by a small value of L_g (only 0.2 deg).

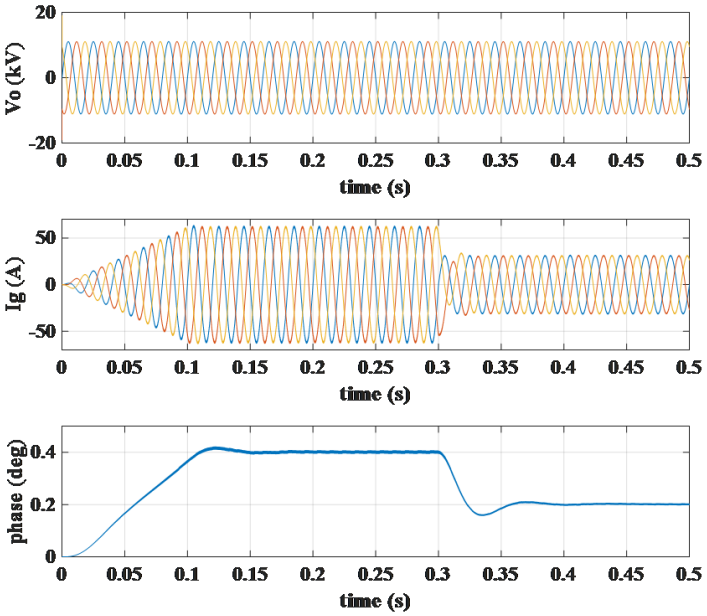
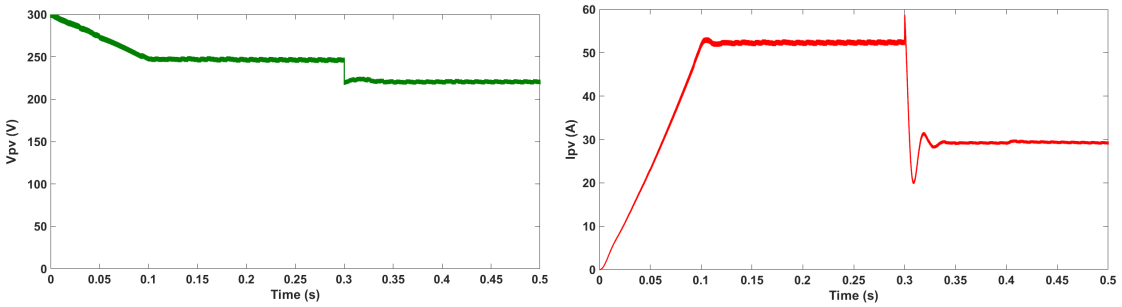


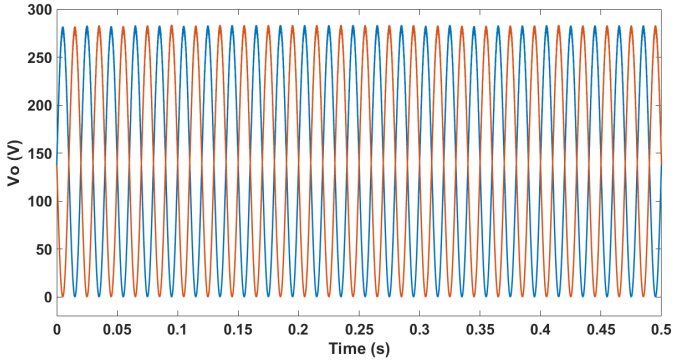
Figure 4.18: the voltage and current output with phase angle response.

Fig 4.19 shows the dynamic responses at the individual system's level, the first PV array's voltage and the current. The output voltages of two successive SMs and their duty-cycle ratios in phase a are shown in Fig 4.20.

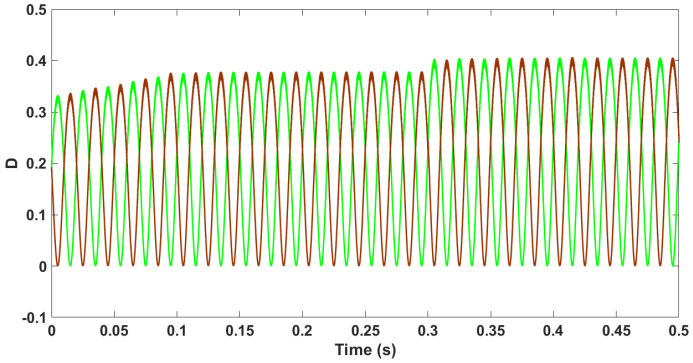


(a) PV array'voltage. (b) PV array' current.

Figure 4.19: The first PV array's voltage and current.



(a) SM voltages.



(b) Duty cycle.

Figure 4.20: Two successive SMs and their duty-cycle ratios.

4.5.2 Case study II: Partial Shading Conditions

In this study scenario, the irradiation level changed from 1000W/m^2 to 500W/m^2 at t = 0.3 s for half of the PV modules, while the irradiation level was kept at 1000W/m^2 for the other half of the PV modules. As shown in Fig 4.21, the total power provided by TPMI is decreased by 25% at t = 0.3 s because half of the PV modules were shaded.

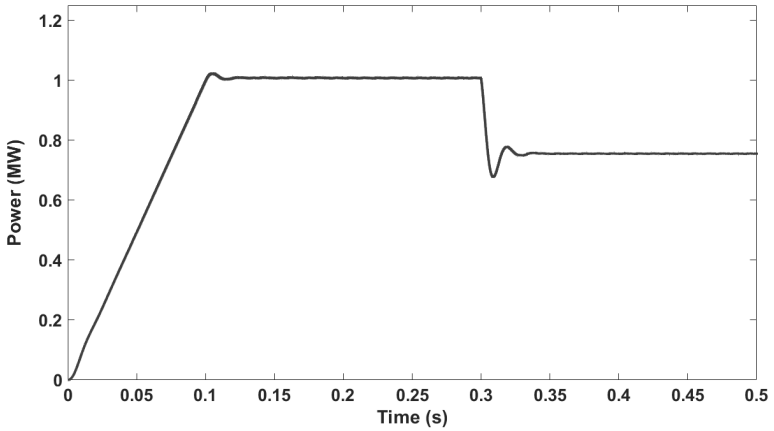


Figure 4.21: Power of TMPI under partial shading condition.

The waveforms of voltages and currents are seen in Fig 4.22, which indicates the magnitude of grid voltage has not changed, whereas the current injected into the grid is reduced by 25% due to the phase angle has shifted slightly to accommodate the new power output.

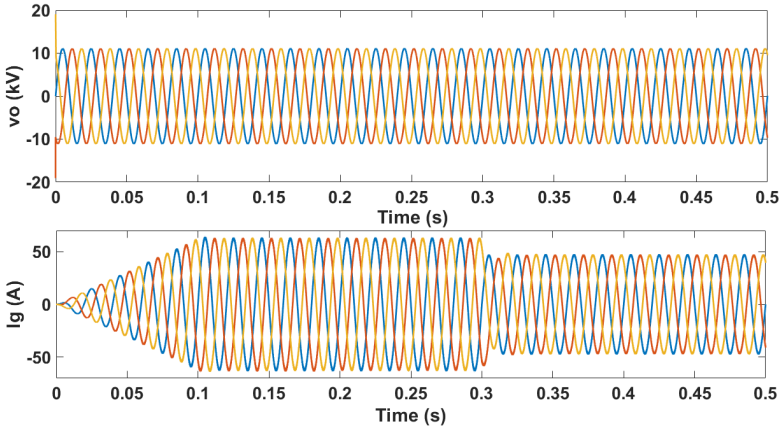


Figure 4.22: Voltage and current responses.

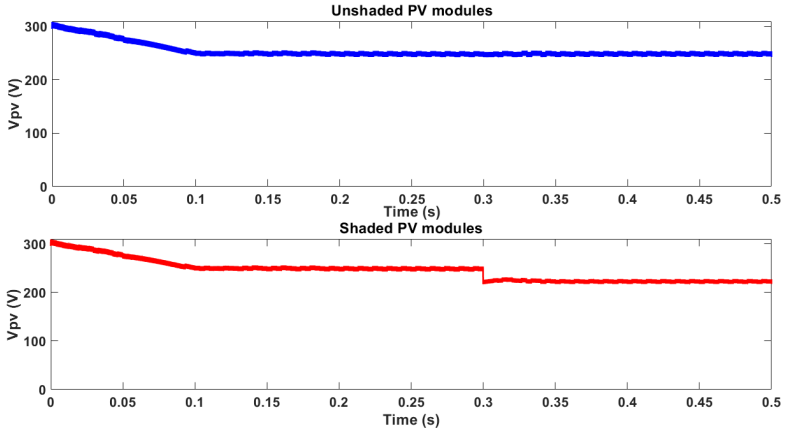


Figure 4.23: Voltage of PV modules without and with shading.

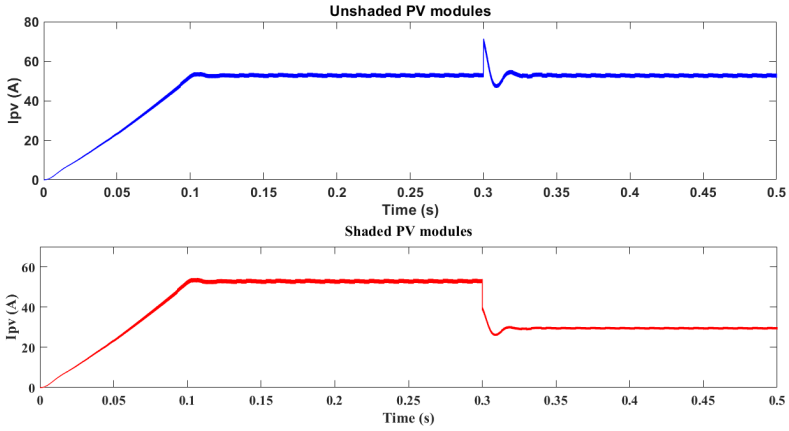
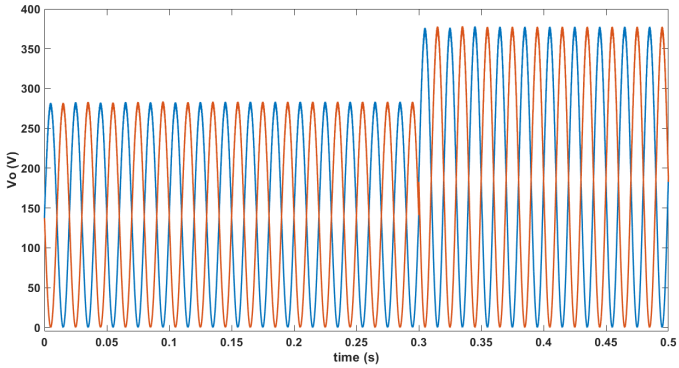


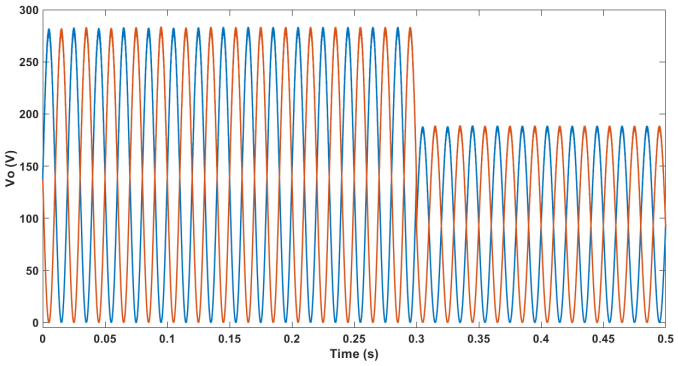
Figure 4.24: current of PV modules without and with shading.

The voltage and current of the PV modules under shaded and unshaded operation circumstances, respectively, are shown in Figs 4.23 and 4.24. The PV modules were not in the shading; their initial voltage began with open-circuit voltage due to the operation point on the PV curves set at point (p_1). As the operation point moved to its maximum point (p_2), these modules operated at the maximum voltage. On the other hand, the shaded PV modules had different PV curves due to the reduction of irradiance occurring at t = 0.3; hence, their operation point moved to a lower maximum point (i.e., (p_3)) as their voltage decreased. Similarly, the current response operated at an open circuit voltage with a zero value and then reached its maximum value. This means that the operation point for unshaded PV modules was (p_2), whereas the operation point for shaded PV modules was (p_2) due to the decreased irradiation level.

The output voltage of the two shaded and un-shaded SMs can be seen in Fig 4.25. Unshaded SMs increase their output voltages in order to compensate and match the grid voltage, whereas shaded SMs were already affected by the shading time of 0.3 s and their voltages were reduced.



(a) Unshaded SM voltage.



(b) Shaded SM voltage.

Figure 4.25: Voltage of shaded and unshaded SMs.

4.6 Experimental structure and results

In this section, the experimental tests are conducted on a scaled-down prototype of TPMI connected to the local utility grid. The proposed TPMI has been developed based on four SMs per phase to validate and confirm the simulations and theoretical studies of its performance and associated control strategy, as shown in Fig 4.26. Moreover, the DC voltage supplies have been used to mimic the PV modules in their operating conditions.

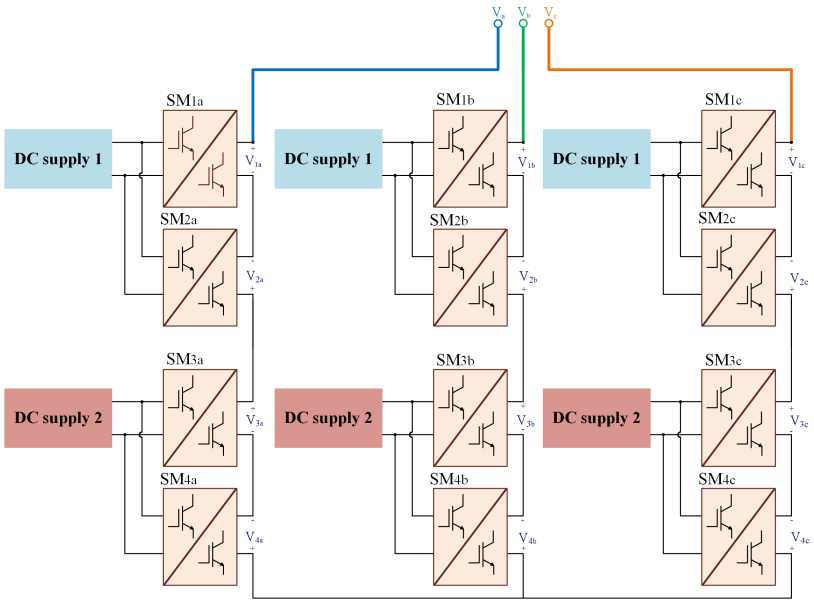


Figure 4.26: The experimental SM connections.

At the beginning of the procedure of preparing TPMI to be connected to the grid, a description of the hardware platform and associated components, such as the control board and measurement sensors, is provided. This is followed by three different experimental results that were conducted using the hardware prototype to determine the fundamental operational principles and the feasibility of the TPMI.

4.6.1 Hardware structure

An experimental setup of a scaled-down prototype dc-ac grid-connected TPMI inverter is developed, as shown in Fig 4.27, where the TMS32028335 DSP control board is used to implement the control strategy. To illustrate the modular structure of TPMI, a zoomed-in view at phase B reveals that all four SMs are identical. The following is an explanation of the different various components that are needed for bench setup.

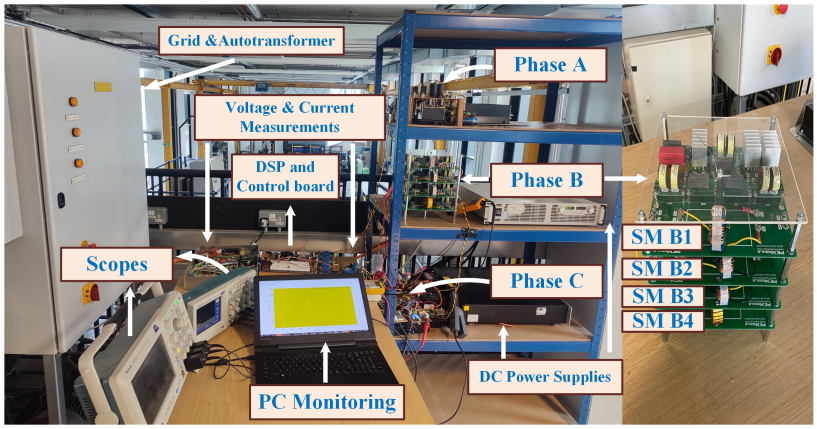


Figure 4.27: Experimental setup of TPMI.

4.6.1.1 Digital Signal Processor

The TMS320F28335 is a digital signal processor (DSP) belonging to the TMS320C28X family of floating-point DSP controllers, which is made by Texas Instruments (TI), as seen in Fig 4.28. This DSP features high precision, low power consumption, low cost, high performance, sufficient storage memory, compatible and rapid analog-to-digital conversion, and simple programming packages. The TMS320F28335 has a high-speed processing speed of 150 MHz, a 32-bit floating-point processing unit, up to 18 PWM outputs, and 12-bit, 16-channel analog-to-digital converters (ADCs)[153]

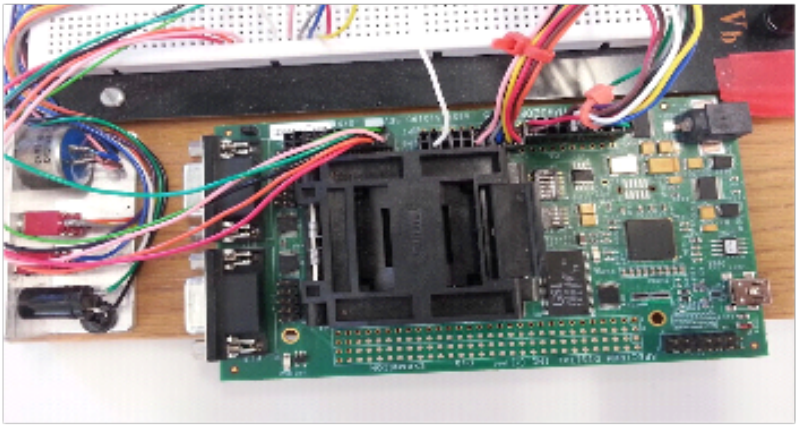


Figure 4.28: TMS320F28335 DSP board.

The main responsibility of the TMS320F28335 DSP is to generate the pulse width modulation (PWM) signal for the gate drive circuits that operate the active switches of the TPMI inverter. This DSP does not need any extra interfacing circuit because its output port is compatible with the gate drive input voltages and currents. In addition, the TMS320F28335 DSP allows real-time monitoring and control by delivering data to the RAM's addressed memory and displaying it using the Code Composer Studio software because measurement sensors are designed to have voltages and currents within the DSP's read range.

The TMS320F28335 DSP can be programmed with either C, C++, or MATLAB/Simulink. The support package turns Simulink block diagrams into C code and makes it possible to download embedded code to the hardware board. Moreover, the DSP supports the CAN protocol and is hence compatible with CANalyzer boxes. CANalyzer Vector-XL can transfer all C code variables to the host PC via the CAN communication protocol.

Practically, the PR controller can be discretized and implemented using accessible DSP technology without the need for algebraic loops. The generalised discrete

equivalent of the PR controller can be easily derived usingthe bilinear pre-normalized transform (Tustin) by expressing the following[154]:

$$s = \frac{2}{t_s}\frac{z-1}{z+1} \tag{4.19}$$

The PR controller in the discrete z-domain is represented by Eq4.19, which is substituted into Eq4.16 and yields the transfer functions listed below:

$$G_{PR}(Z) = \frac{k_r \cdot \frac{2}{t_s}\frac{(z-1)}{(z+1)}}{\frac{4}{t_s^2}\frac{(z-1)^2}{(z+1)^2} + \omega^2} \tag{4.20}$$

The following transfer function is derived from the relation $G_{PR}(Z)$:

$$G_{PR}(Z) = 2 \cdot t_s \cdot k_r \frac{(1 - z^{-2})}{(4 + \omega^2 \cdot t_s^2) + (2 \cdot \omega^2 \cdot t_s - 8)\, z^{-1} + (4 + \omega^2 \cdot t_s^2)\, z^{-2}} \tag{4.21}$$

The equation 4.21 can be rearranged as follows:

$$G_{PR}(Z) = \frac{a_0\,(1 - z^{-2})}{b_0 + b_1 z^{-1} + b_2 z^{-2}} \tag{4.22}$$

Where

$$\begin{cases} a_0 = 2 \cdot t_s \cdot k_r \\ b_0 = (4 + \omega^2 \cdot t_s^2) \\ b_1 = (2 \cdot \omega^2 \cdot t_s^2 - 8) \\ b_2 = (4 + \omega^2 \cdot t_s^2) \end{cases} \tag{4.23}$$

The PR controller in the z domain can be reformulated in terms of the error e (z) and

the controller output y (z) as follows:

$$G_{PR}(z) = \frac{y(z)}{e(z)} = k_p + \frac{a_0\left(1 - z^{-2}\right)}{b_0 + b_1 z^{-1} + b_2 z^{-2}} \tag{4.24}$$

The following expression is the difference equation for the PR controller required for DSP implementation:

$$y(n) = \left[a_0 \cdot \left(e(n) - e(n-2) - b_1 \cdot y(n-1) - b_2 \cdot y(n-2)\right)/b_0\right] + k_p e(n) \tag{4.25}$$

Where $y(n)$ represents the present output control action, $y(n-1)$ represents the previous output control action, $e(n)$ shows the present error, and $e(n-1)$ represents the previous error.

4.6.1.2 Gate drive circuits

In this experiment, the gate drive circuits are employed to buffer the PWM switching signals generated by the DSP before sending them to the switches, as shown in Fig 4.29. The gate drive circuits are required to amplify the DSP output current so it can reach the switch gate current because the DSP can only make a few milliamps, which is not enough to turn on the switch. The gate drive circuits feature high safety isolation that allows for galvanic isolation between the DSP ground and the switches' common points.

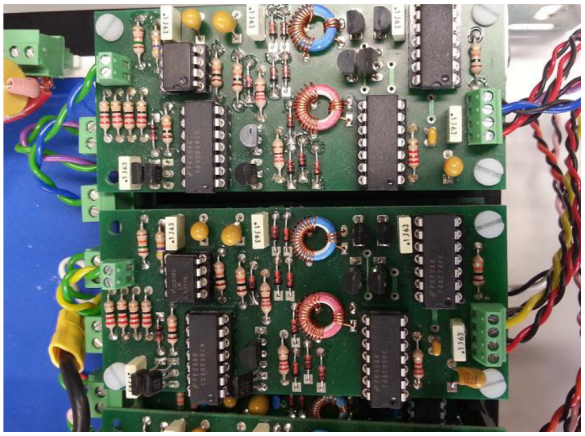


Figure 4.29: Gate drive circuits.

4.6.1.3 Voltage and current measurements

The TPMI inverter is connected to the utility grid, so accurate measurements should be taken from different parts of the integrating process, such as the current via the grid inductors and voltages at PCC, in order to provide the proper control task. This section will describe the measurement circuits for current and voltage.

(A) Voltage measurements

The voltage measurement board is shown in Fig 4.30 and is used to measure the voltages when the TPMI inverter is connected to the local grid. This board can scale the input voltage and add a dc-bias, so the output voltage is compatible with the ADC of the DSP. The LEM25-P sensors are chosen because of their 10–500 V measurement range and high-frequency bandwidth. The LEM25-P can measure ac and dc signals using the Hall effect.

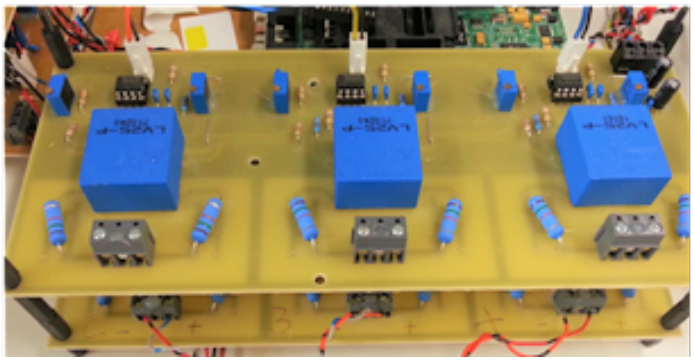


Figure 4.30: Voltage measurement board.

(B) Current measurements

The current measurement board is implemented to measure the inverter output currents, which are then delivered to the DSP for feedback control. The LEM LA55-P sensing devices are selected to construct the current sensing boards, as shown in Fig 4.31. These sensors provide galvanic isolation since they are based on the Hall Effect. These sensors feature a wide measuring range from 0-50 A with a maximum bandwidth of 200 kHz.

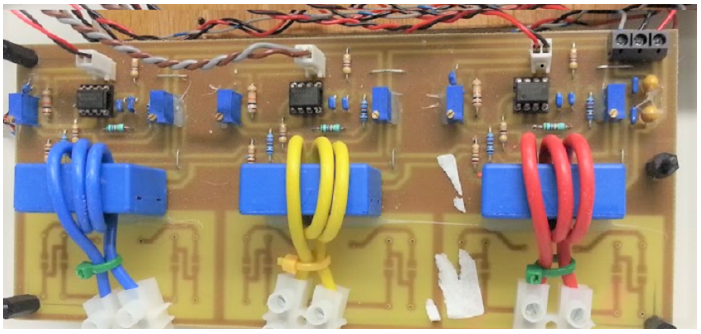


Figure 4.31: Current measurement board.

4.6.1.4 Auto-transformer

Autotransformer is used to connect the low-voltage scaled-down of TPMI to the local AC grid. Fig 4.32 presents an autotransformer with three phases, which features the following: Type: RAVISTAT, Serial Number: 1212/11684, Input: 415 volts, 3-phase, 50 or 60 Hz; output: 0–415 volts and 10 amperes per line.

Figure 4.32: Transformer with three phases.

4.6.1.5 DC power supplies

The DC power supplies have simplified the PV modules to simulate their operation in experimental tests. Thus, two different power supplies are used, one for the top two SMs and the other for the lower two, as shown in the connection in Fig 4.26. These power supplies, Sorensen SG A80/65 and Keysight N8761A, are shown in Fig 4.33.

(a) First DC power supply.

(b) Second DC power supply.

Figure 4.33: DC power supplies used in experiments.

4.6.2 Experimental results

Fig 4.27 shows the experimental setup for the proposed TPMI three-phase implementation with four SMs per phase, and Fig 4.26 is a block schematic of the connection between the SMs. In this work, each SM is rated at 250 W, so the total TPMI system's maximum power is rated at 3 kW. The output of the system is connected to the local grid, and its rated power is injected into the AC grid to validate the performance of the three-phase TPMI topology.

The procedure of connecting and synchronising the three phases of TPMI to the local grid is shown in Fig 4.34 to provide a clear explanation of the operation. The proposed TPMI is initially connected to the grid via an autotransformer, which gradually increases the output voltage of the TPMI. Then, the voltage sensors measure the voltage at the PCC, where the autotransformer is connected, and these measurements are converted to the digital format by the analog-to-digital converters (ADCs) for use by the DSP controller. In the following step, the DSP controls the switches of the TPMI to provide the same voltage as the PCC. Thus, the current is always zero,

and there is no power flow into the grid. The next step is to increase the voltage manually by turning the dial on the auto-transformer until the maximum voltage is reached. In the final step, the circuit breaker (CB) is disconnected and the system is fully connected to the grid.

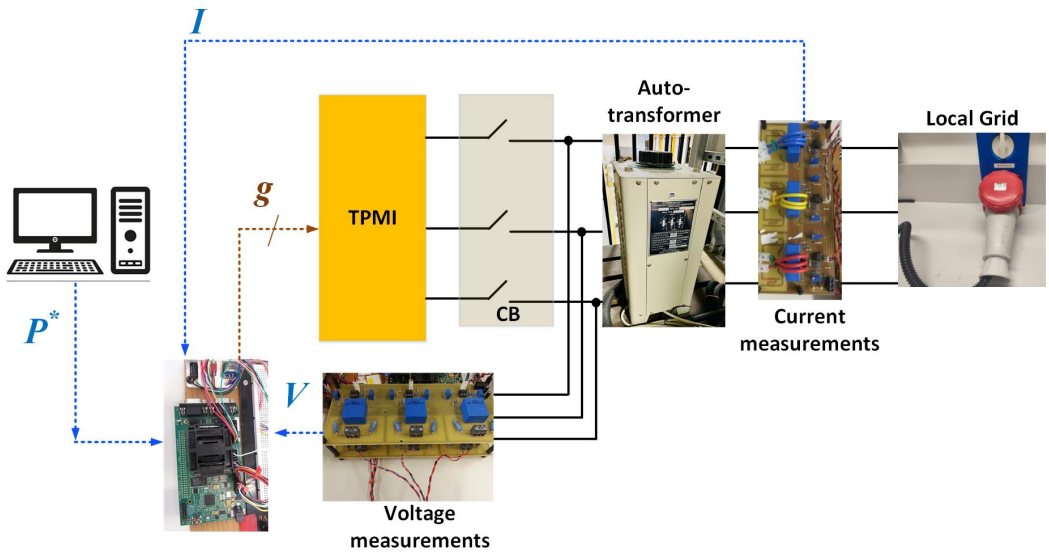


Figure 4.34: Practical steps for grid connection.

In this section, the TPMI has been tested at an output power of 3 kW for three different power supply levels to verify the simulation studies and the analytical derivations. In the first experiment, the proposed TPMI is validated with full-rated input power supplies (i.e., standard conditions). Then, an investigation was conducted under uniform shading conditions by lowering the rated power of both of the power supplies. followed by an experiment with partial shading based on reducing the rated power of one power supply while operating another at full-rated power. Table4.3 provides a list of the parameters for all experimental cases.

Parameter	Value
Number of SMs	$n = 4$
Input Voltage	$V_{in} = 48\ V_{dc}$
Input Current	$i_{in} = 16\ A$
SM rated power	P_{SM}= 250
Rated output power	P_o= 3 kW
Grid voltage	400 V_{ac}
Grid impedance	$L_g = 1$ mH, $r_g = 0.5$
Grid frequency	$f_o = 50$ Hz
Switching frequency	f_s= 20 kHz
Transformer turns' ratio	$N = 2$
SM inductors	$L_n = 1$ mH and $L_1 = L_2 = 1$mH
SM Capacitors	$C_r = C_S = C_C = 10\mu F$

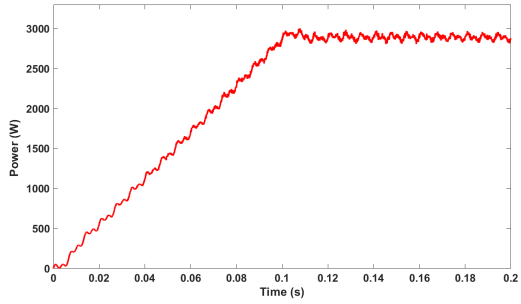
Table 4.3: Parameters of experimental prototype

4.6.2.1 Experiment I: Standard conditions

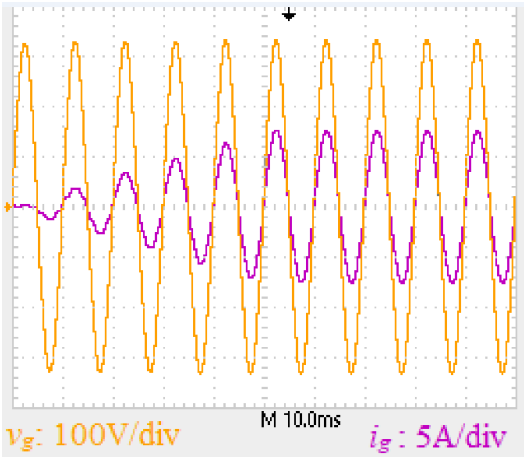
This experiment demonstrates that the DC power supplies were set to their rated input voltage and supplied power for all SMs. As shown in Fig 4.15, the scenario that began with TPMI is operating at its maximum power point (p_2). Therefore, it is capable of gradually delivering its full power of 3 kW into the grid,as shown in Fig 4.35a. This power is computed based on the voltage and current measurements made by the sensor boards. Then, these values are delivered to the DSP, which is connected to the PC's code composer program, and the required software is used to

plot the power. The power is calculated as follows:

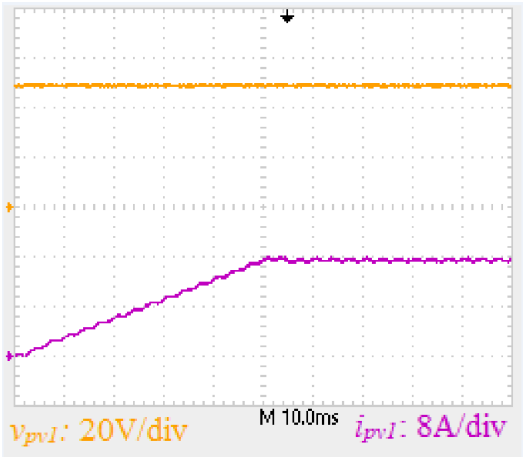
$$P = V_a i_a + V_b i_b + V_c i_c \tag{4.26}$$



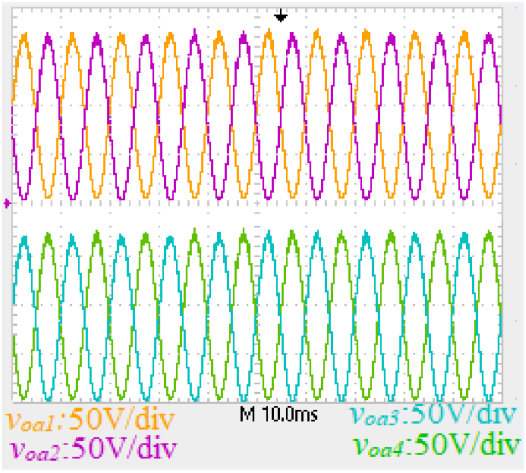
(a) Output power.



(b) Grid voltage and current.



(c) PV voltage and current.



(d) SMs voltage.

Figure 4.35: Normal-condition results.

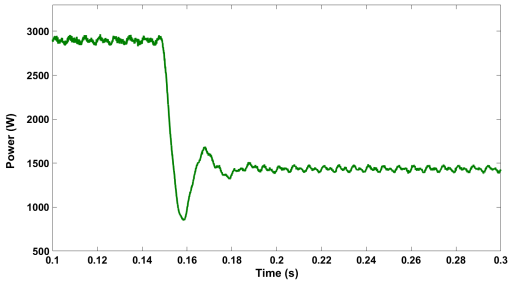
The single-phase grid voltage and current are shown in Fig 4.35b, where the grid current follows the variations in output power P_o, hence it increases and reaches its highest value at t = 0.1 s. Fig 4.35c presents the input voltage and current waveforms

of the first PV module, which supplies the first SM. It can be noted that the output power will increase until it reaches its rated value according to the input current is increased. On the other hand, the four SMs in phase a have identical output voltages, and their summed voltage is synchronised with the grid voltage, as illustrated in Fig 4.35d.

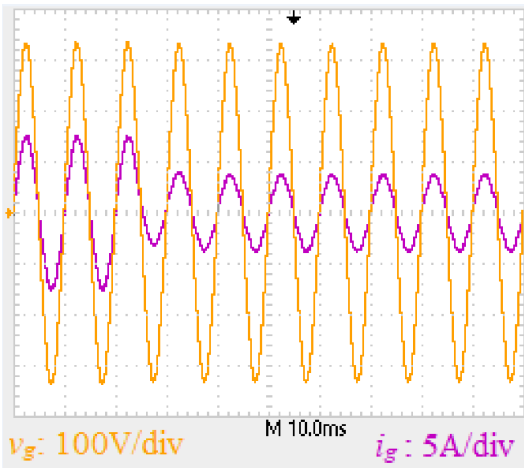
4.6.2.2 Experiment II: Uniform shading conditions

Here, the results of the experiments are used to verify part of the computer simulations done in Case study 4.5.1. Both power supplies are reduced by generating 50% of their rated power to demonstrate the TMPI system's performance under uniform shading conditions. As the power from the DC supplies is changed, the code programmed in the TI DSP understands that there is partial shading and moves to new reference values of the controller according to the values from the PV curves (lookup tables), as shown in Fig 4.14.

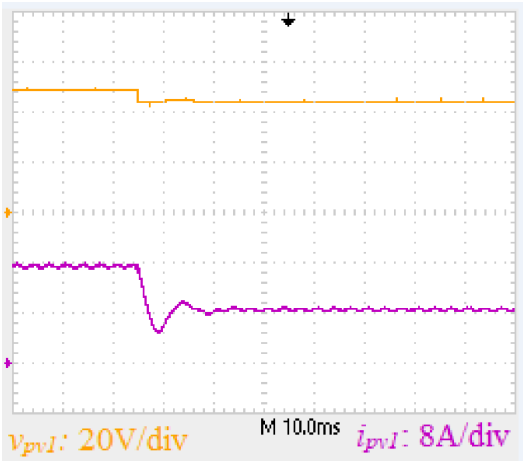
In this case, the operational point has been moved from the maximum point to the bottom one. Fig 4.36a shows that the new input power of DC supplies resulted in a significant shift in the total output power, triggering a reduction of around half the total power. The current injected into the grid is reduced by 50% due to a shift in the phase angle, which can be seen in Fig 4.36b. The input voltage and current waveforms that fed the first SM are shown in Fig 4.36c, respectively. Furthermore, the voltages of the SMs were maintained at a fixed value, and their total voltage was synchronised with the grid voltage; only the phase angle was changed by a small value, as shown in Fig4.36d.



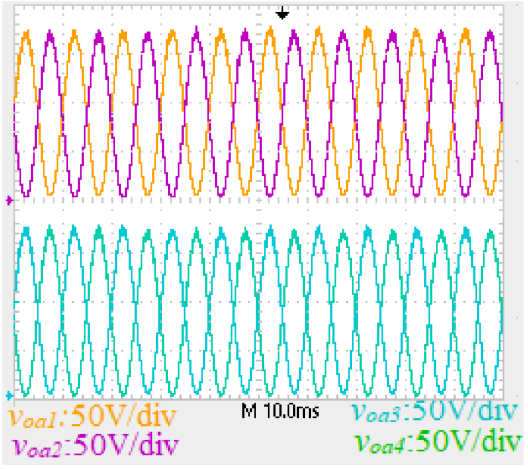
(a) Output power.



(b) Grid voltage and current.



(c) PV voltage and current.



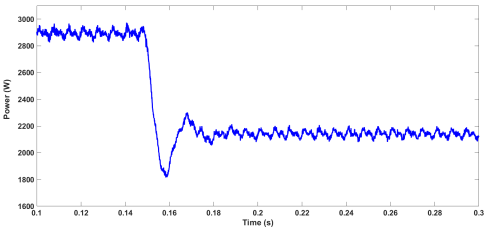
(d) SMs voltage.

Figure 4.36: Uniform shading conditions.

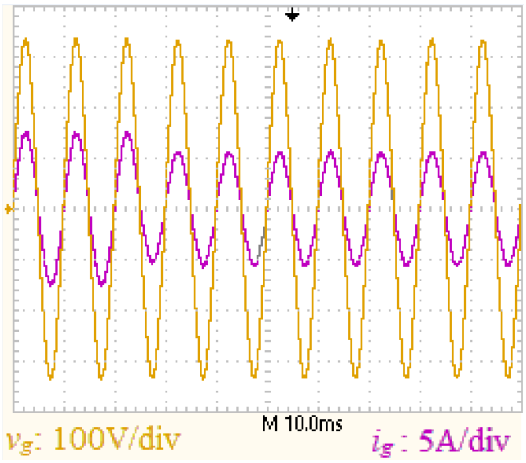
4.6.2.3 Experiment III: Partial shading conditions

In this experiment, the bottom power supply generated 50% of its rated power while the top power supply continued to provide 100% of its rated power to further illustrate the performance of the system under partial shading conditions. Consequently, the total maximum available power of the system is 75% of the value compared to standard operating conditions, and this is controlled by setting the reference value of the output

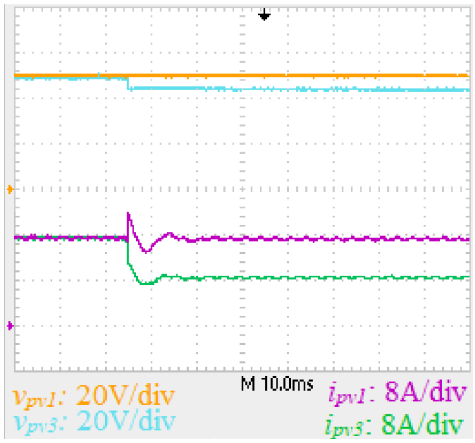
grid current to 75% of its rated value.



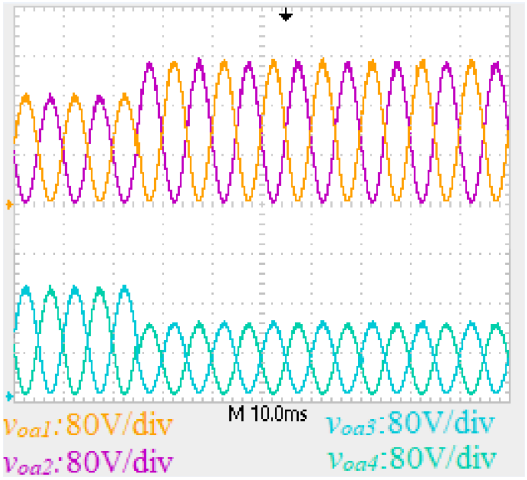
(a) Output power.



(b) Grid voltage and current.



(c) PV voltage and current.



(d) SMs voltage.

Figure 4.37: Partial shading conditions.

At t = 0.16 s, the total output power will be reduced to 75% of the value under normal conditions because of the shading of the bottom power supply, as seen in Fig 4.37a. Fig 4.37b shows the waveforms of phase grid voltage and current when grid current has dropped to 75% because of partial shading. The supply voltages and currents for the unshaded top power supply and the shaded bottom one can be shown in Fig 4.37c.

The output voltages of the four SMs in phase a are depicted in Fig 4.37d. Before the time of partial shading, the output voltages of the SMs were identical. Then, the voltages of the unshaded SMs were increased to compensate for the voltage reduction, while the voltages of the shaded SMs were dropped by the same proportion.

4.7 Comparison and Evaluation

The proposed TPMI inverter is compared to state-of-the-art current source topologies in terms of topology, conversion ratios, number of components, and power efficiency. A comparison of the performance of several works of literature in which all topologies were tested under normal operating conditions with the same number of SMs or power cells [32], [33], [150]. In Table4.4, These topologies are categorised based on their SMs, resulting in five distinct types.

Topology	conversion ratios	Inductors / Capacitors	power efficiency
Cuk	$\frac{ND}{1-D}$	2 / 3	97.5%
P5	$\frac{ND}{1-D}$	3 / 4	96%
DISC	$\frac{2ND}{1-D}$	3 / 5	94%
Sepic	$\frac{ND}{1-D}$	2 / 2	93.5%
F5	$\frac{ND}{1-D}$	2 / 3	92%

Table 4.4: Comparison of the proposed SM with comparable topologies.

The proposed TPMI based on DISC SMs provides a high conversion ratio in comparison to the existing four SM buck-boost converters. This feature allows the DISC converter to handle high input voltage variations with the same duty cycle

range, or alternatively, it enables the converter to regulate the same input voltage variation with a narrower duty cycle range, which allows the use of smaller input inductors. However, The DISC converter consists of a number of passive components, which can increase its weight and dimensions. In addition, the DISC SM is derived from an eighth-order converter, increasing the complexity of the control system.

The efficiency of the selected topologies is recorded for different ranges of the output power and input voltage values, as shown in Fig 4.38. The following expression represents the calculation of efficiency based on power efficiency (η):

$$\eta = \frac{P_o}{P_n} = \frac{V_o * i_o}{V_{in} * i_{in}} \tag{4.27}$$

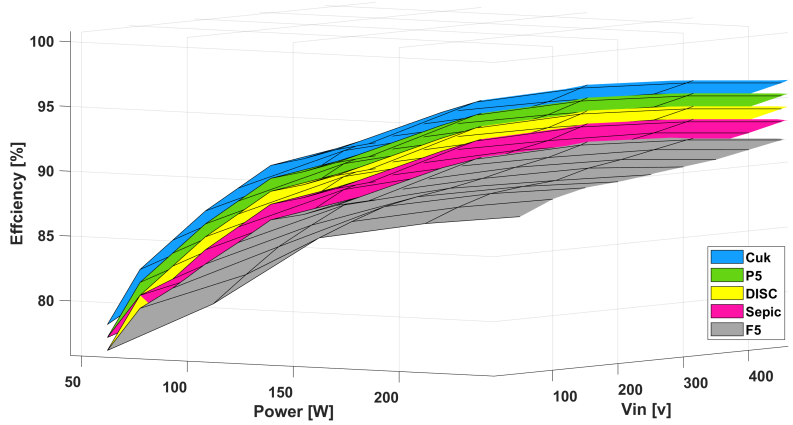


Figure 4.38: Efficiency evaluations for selected inverter topologies.

The cuk SM topology achieves the highest efficiency; consequently, it is preferable to maximise the PV system's power harvest. The efficiency of the proposed DISC topology is within an acceptable range due to the high voltage stress and ESR losses. The F5 inverter has the lowest efficiency compared to other topologies because a larger

transformer magnetic core is required to temporarily store and then discharge energy.

4.8 Chapter Conclusion

This chapter introduced new TPMI systems suitable for LSPV systems to improve the energy conversion of PV power. The TPMI has several advantages over the conventional centralised system, such as modularity, scalability, fault tolerance, continuous input current, the capability of providing both voltages step-up and step-down, and better performance during shading conditions because of the use of distributed MPPT controllers. The control strategies have been investigated, created, and presented. The proposed inverter is controlled by two control loops at both the system and SM levels. The operation of the inverter has been simulated using MATLAB/Simulink under standard, equal shading, and partial shading circumstances to confirm that the controller can extract the maximum available power from the PV modules. Then, the results are verified and confirmed by a scaled-down experimental prototype of 3kW with four SMs and a TMS320F28335 DSP controller.

Chapter 5

Proposed TMPI: modified SM structure and modulation process.

The previous chapter analysed the TPMI and discussed its applicability for high-power PV applications. This chapter is extended to form a new version of the TPMI to improve its overall performance and efficiency at high frequencies. The TPMI structure is modified based on its DISC SMs, where replace the output switches with diodes and add a bypass switch operating at grid frequency. Compared to conventional DISC SMs that operate with two output switches at high frequencies, the modified structure of the DISC SMs provides the advantage of having a single output switch with a small internal resistance because of their operation at grid frequency. Thus, the conduction and switching losses can be decreased. In addition, the modulation principle is set to operate for only a half-cycle to reduce the semiconductor and copper losses.

The following section details the modification of the TPMI to use its new structure of DISC SMs. A discussion of the modulation approach for switches and the

fundamentals of modified SM operations will be described. A simple proportional-resonant (PR) controller is presented to control the output current. The results of the simulation studies conducted on the new TPMI structure using MATLAB-SIMULINK are presented. A laboratory prototype has been created, and experimental findings are provided to confirm the concept.

5.1 Circuit structure

Fig5.1 presents the TPMI system that can draw power from PV modules and feed it into the MV grid. The converter SMs can be configured with series or parallel input connections and series output connections, allowing grid-connected PV systems to operate without a step-up LFT. Because the target is the grid connection, the TPMI inverter is connected to the grid via grid inductors with internal resistances.

Here, unlike the conventional DISC-SM converters, three passive diodes and a single unidirectional power switch are employed. As shown in Fig5.2, the modified DISC SM topology replaces the output switches of the converters with diodes and adds an active switch and diode to the AC output side. The redesigned DISC SM structure employs diodes D_{o1} and D_{o2} to remove the output switches and offer a suitable path for the SM current. The output terminal of the DISC is equipped with an external diode to provide a flowing current path and prevent short-circuiting. Moreover, the outer switch S_o is responsible for bypassing the reverse current from the grid. This structure of DISC SM gets rid of the high-frequency output switches, so it can provide reduced switching and conduction losses, increased efficiency, and enhanced system reliability.

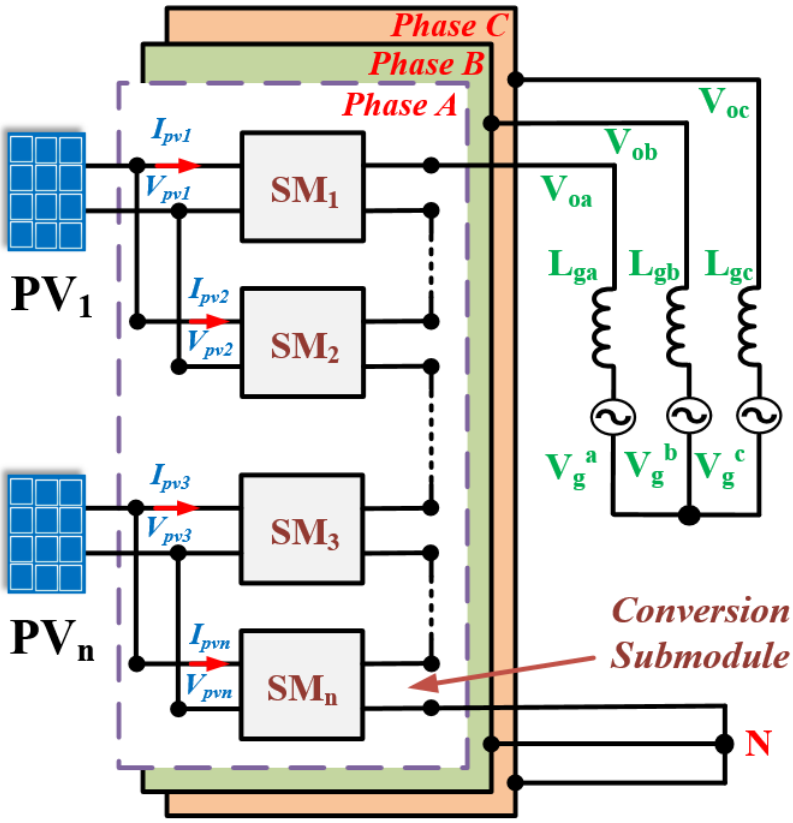


Figure 5.1: TPMI PV conversion system.

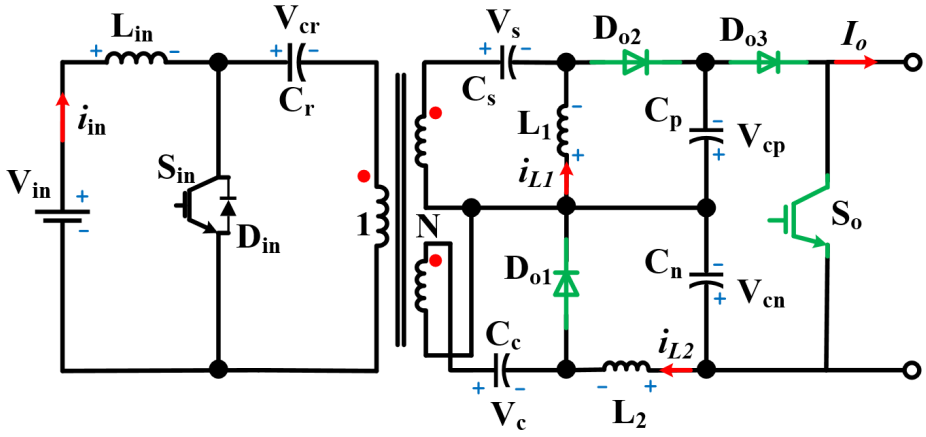


Figure 5.2: The redesigned structure of DISC SM conversion.

5.2 Modulation strategy

The modified structure of TMPI will be controlled and operated using a new modulation technique called half-cycle modulation (HCM). The operation of HCM is dependent on the switches being activated for only half of the cycle. This can result in a reduction of the switching and conduction losses of the power devices. To clarify the modulation principle, two successive SMs operate in turns, and each SM outputs a voltage with a half-sinusoidal waveform. As shown in Fig 5.3, both SMs are fed by the same PV module, where each SM operates for half a cycle without the need for a dc offset on the output voltage side. Therefore, the difference between the outputs of the two SMs generates a pure sinusoidal ac voltage at the output.

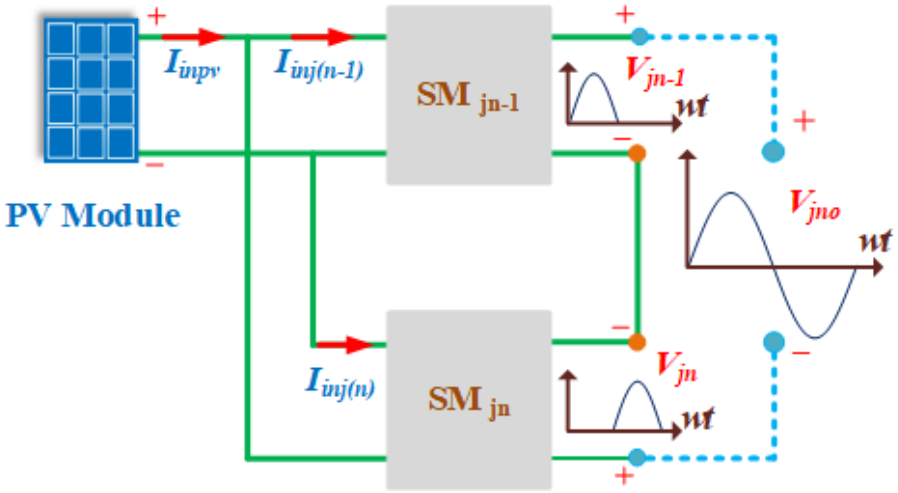


Figure 5.3: HCM principle.

The output voltage of each SM can be described by the following equations.

$$V_{jn-1} = \begin{cases} V_{n-1}\sin(\omega t) & 0 \geq \omega t \geq \pi \\ 0 & \pi > \omega t \geq 2\pi \end{cases} \tag{5.1}$$

$$V_{jn} = \begin{cases} 0 & 0 \geq \omega t \geq \pi \\ V_n \sin(\omega t + \pi) & \pi > \omega t \geq 2\pi \end{cases} \tag{5.2}$$

Because the magnitudes of the ac voltages V_{n-1} and V_n are equal, the output voltage produced by both SMs is a sinusoidal ac voltage that is obtained as follows:

$$V_{jno} = V_n \sin(\omega t) \tag{5.3}$$

As the switches operated in the half cycle, it is expected that this modulation technique will have lower losses and be more efficient than the modulation strategy discussed in Chapter 4. In addition, each SM contains an input switch S_{in} that operates solely at high frequency, whereas the output switch S_o operates at grid frequency. As shown in Figs 5.4 and 5.5, both switch patterns are active for only a half-cycle, resulting in a reduction in overall switching losses.

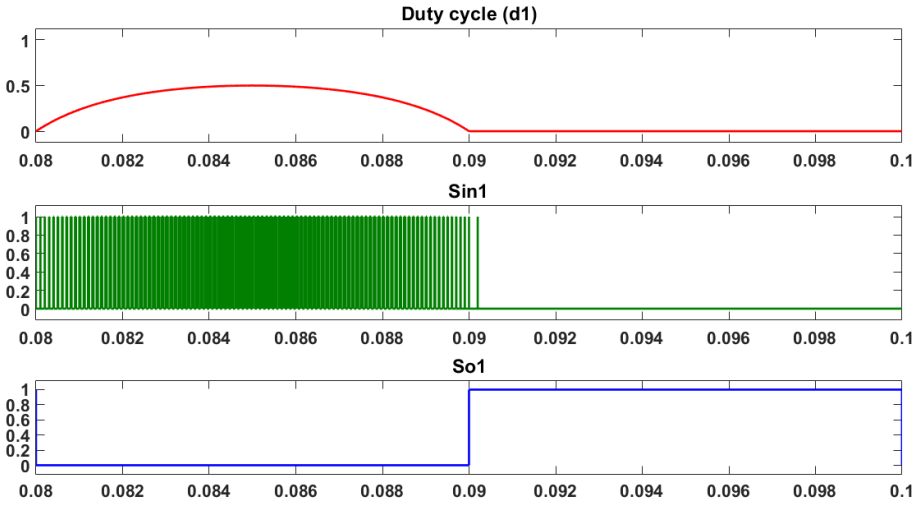


Figure 5.4: First SM switches pulses.

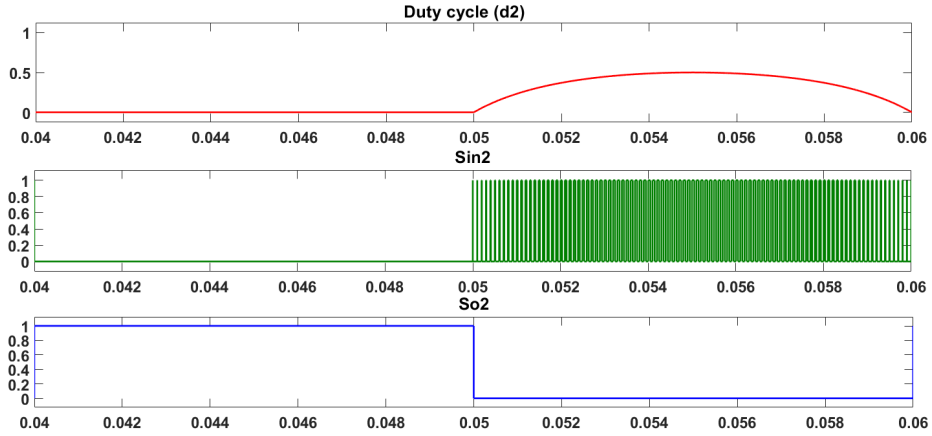


Figure 5.5: Second SM switches pulses.

5.3 SM Operation

The operational states of this modified design of DISC SM topology are the same as the classic DISC SM; the only difference is that the employed diodes and a switch add a new path for the output current to flow in the freewheeling period. The following sections describe the details of each operation state:

5.3.1 State 1 (ON cycle)

In this state, S_{in} is on while S_o is off, and the input inductor is shorted to ground, which increases its current and stored energy, as shown in Fig 5.6. Since the S_{in} is grounded, the positive terminals of the primary capacitor (C_r), SEPIC capacitor (C_s), and Cuk capacitor (C_c) on their right-hand side terminals have a negative potential relative to ground. Therefore, the voltage on the left is greater than the voltage on the right, causing both D_{o1} and D_{o2} to be in reverse-biased conditions. Meanwhile, the energy stored in the C_r and C_s and C_c is released into the inductors L_1 and

L_2. Consequently, their currents i_{L1} and i_{L2} increase simultaneously while the output capacitors C_p and C_n discharge their energy to the output load via D_{o3}.

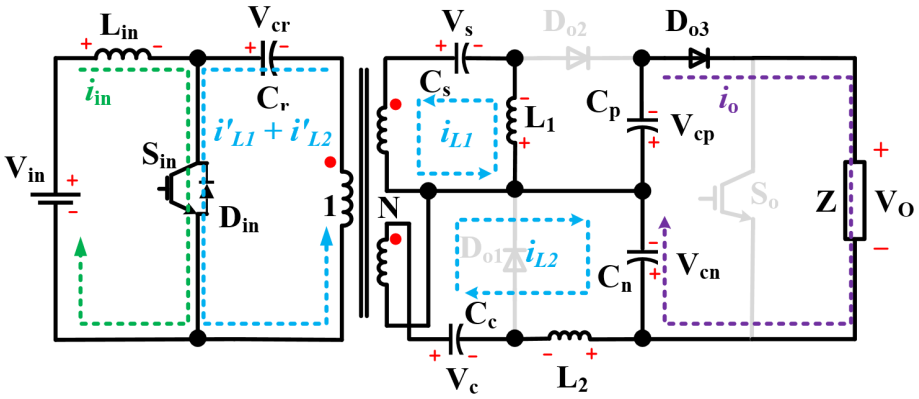


Figure 5.6: State ON cycle.

5.3.2 State 2 (OFF cycle)

As illustrated in Fig 5.7, both switches S_{in} and S_o are off. This causes the input current to flow into the primary capacitor and subsequently through the newly forward-biased diodes to the Sepic and cuk capacitors. Thus, these capacitors charge, and an immediate increase in voltage is observed in each of them.

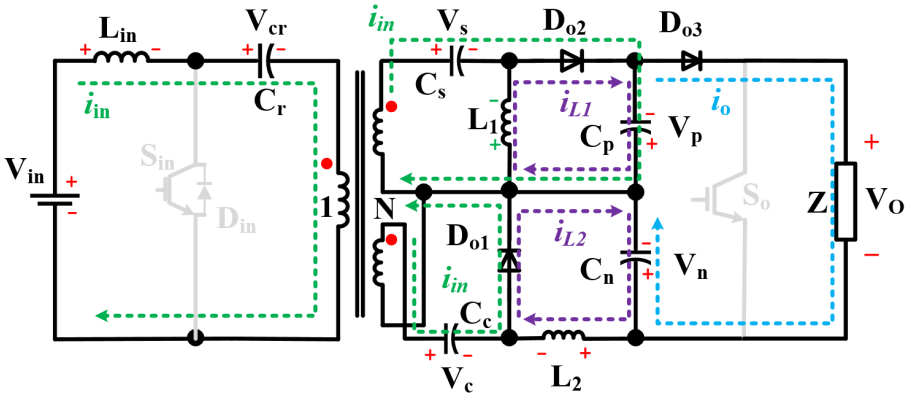


Figure 5.7: State OFF cycle.

As the diodes D_{o1} and D_{o2} begin to conduct, the upper inductor L_1 discharges and transfers energy to C_p and the output load via the diode D_{o3}, whereas the bottom inductor L_2 discharges and releases energy to C_n and the output load.

5.3.3 State 3 (Shutdown)

Only S_o is on, while S_{in} and all other diodes are off, as shown in Fig 5.8. Consequently, the switch S_o is responsible for bypassing the output's current i_o. This mode of operation will continue until the beginning of the next switching period.

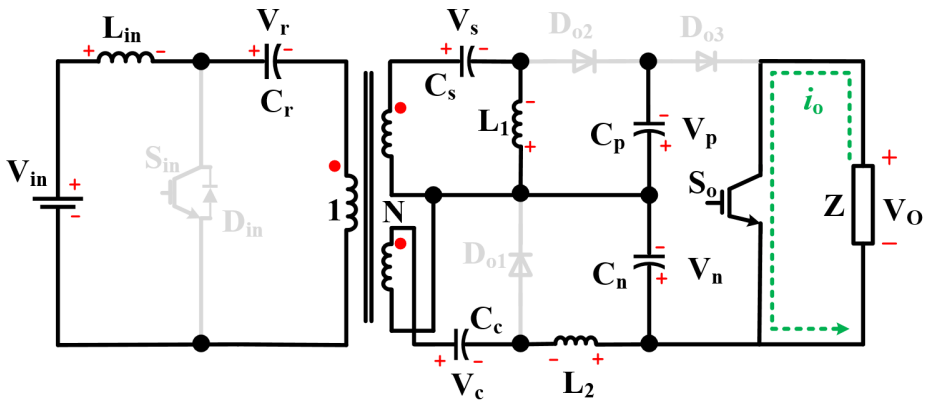


Figure 5.8: State shutdown cycle.

5.4 Control Technique

The control system approach applied to operate the modified TPMI is the same as the control strategy presented in Chapter 4. Fig 5.9 shows the schematic diagram of the PR controller tuned at the grid frequency $\omega_o = 2\pi f$. This controller is responsible for regulating the output current. Notably, this control system assumes that all PV modules function under identical irradiance and weather circumstances. If partial shading is present, a further controller at the SM level will be required to ensure that

the power is distributed across all of the SMs based on their different maximum power points.

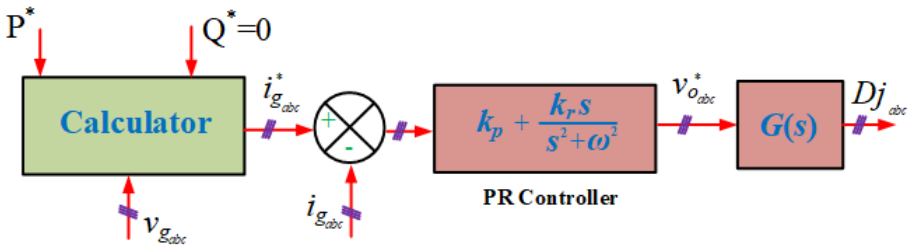


Figure 5.9: Controller system.

5.5 Simulation Results

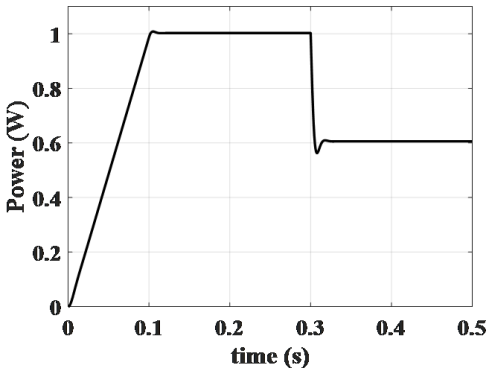
To test the theoretical study and evaluate the performance of the proposed TPMI with its new structure of DISC SM in the LSPV grid-tied inverter, a 1 MW simulation model is created by MATLAB/SIMULINK software and the parameters provided in Table5.1. In this work, each SM is connected to a PV array formed of 3 series x 10 parallel PV modules.

In the simulation study, the response of TPMI to various levels of irradiation will be demonstrated. In Fig 5.10a, it can be shown that the total power delivered to the grid increased from zero to the maximum value of 1 MW at t=0.1. The total power experienced a significant change as the degree of irradiation decreased. At the time t = 0.3, the total power dropped to 60% as a consequence of the new irradiation level. Fig 5.10b displays the output of the three-phase voltages and grid currents. The output voltage waveforms remain synchronised with the grid, but the grid current has dropped to 60% of its rated value as a result of the phase angle adjustment.

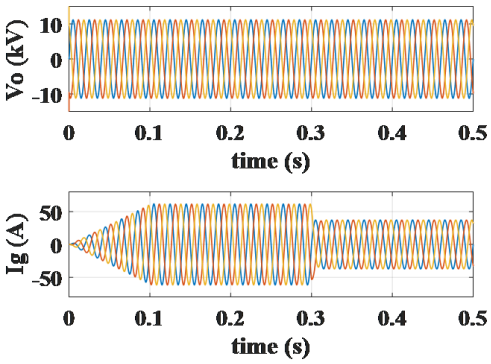
Parameter	Value
Number of SMs (n)	80
Selected PV modules	Grape Solar GS-S-420-KR3
Number of PV array	80
Maximum power, voltage, current operation	420W, 48.73V, 8.62A
Transformer turns ratio	2
Rated power of the TPMI	1 MW
SM Switching frequency	20 kHz
SM inductors	L_n = 1.5 mH and L_1= L_2 = 1mH
SM Capacitors	$C_r = C_S = C_C = 10\mu$ F
Output capacitors	$C_n = 10\mu$ F and $C_p = 50\mu$ F
Grid voltage	13.47 kV
Grid impedance	L_g = 1 mH, r_g = 0.5
Grid frequency	f_o = 50 HZ

Table 5.1: Simulation parameters.

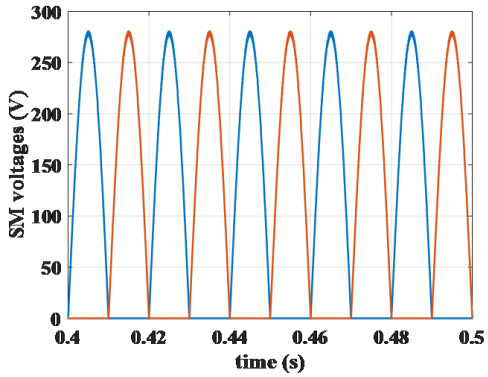
Fig 5.10c presents the output voltage of the top two SMs in phase a, where each SM operates for one half-cycle. The amplitude of these voltages has not changed, but the phase angle has been slightly altered to accommodate the change in power. The input currents for the first two SMs in phase a on the top graph and the total PV module current for the first SMs in phases a, b, and c on the bottom graph are plotted together in Fig 5.10d. Although each of the SMs in the phases has a current that pulses at 100 Hz, the total current pulled from the PV modules remains constant. This means that the PV modules can operate at their maximum power point.



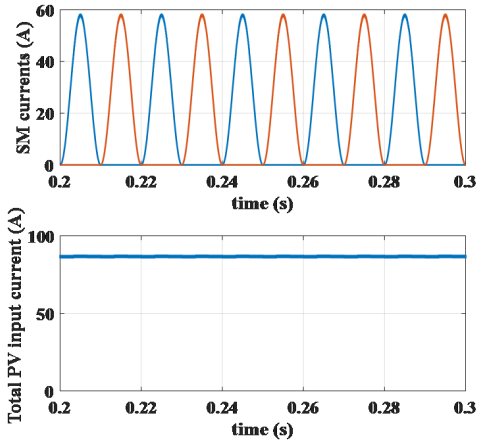
(a) Total output power.



(b) Three-phase voltage and current.



(c) First two SMs' voltage output.



(d) Currents at the input.

Figure 5.10: Simulation results of the TPMI during DC/AC inversion from PV modules to grid.

5.6 Experimental Results

A proof-of-concept hardware prototype is developed and tested using the same passive element parameters mentioned in the computer simulation section. The TPMI is formed from twelve SMs (four SMs per phase) and is used to provide a total of 3 kW of power, with each SM being rated for 250 W. The hardware setup was conducted

using the scaled-down prototype presented in Chapter 4 and employed the same characteristics and concepts provided in Sections 4.6 and 4.6.2. Remember that the PV modules are emulated by two DC voltage sources to mimic the PV modules in the associated states of operation, as shown in Fig 5.11.

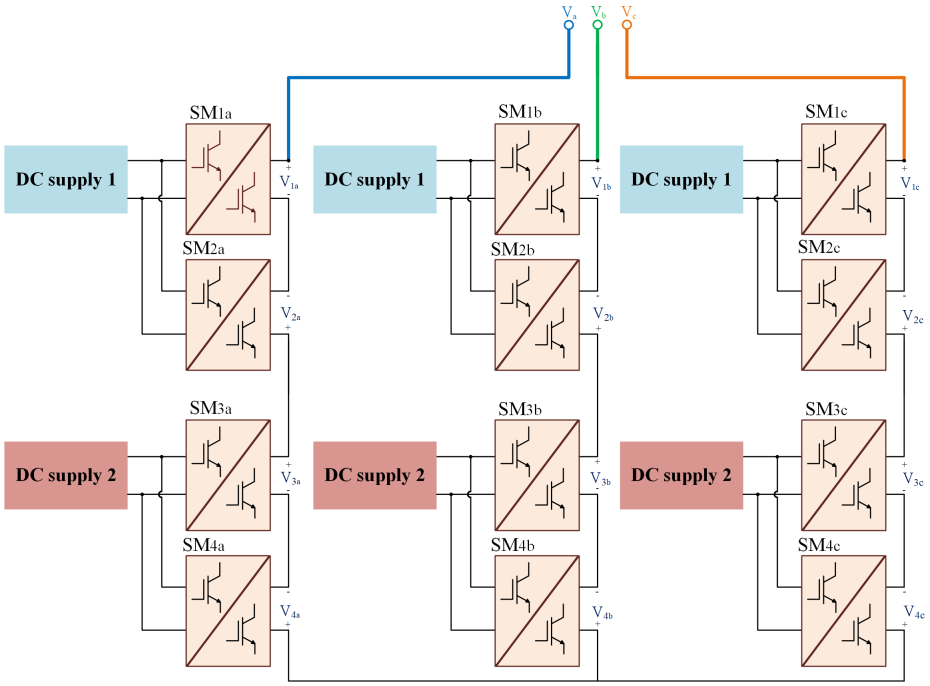
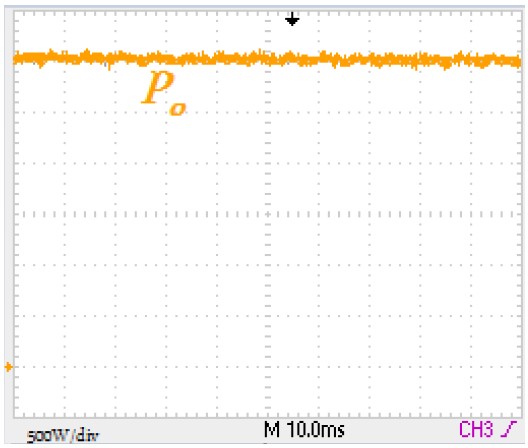


Figure 5.11: The electrical connection of the SMs to the two power supplies.

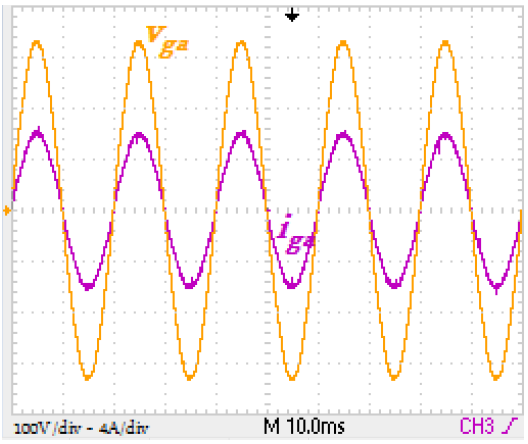
Two different experimental cases were conducted to determine the fundamental operating principles and viability of the TPMI, which is connected to the local grid. In the first scenario, both dc sources begin with their normal maximum power in order to test the performance of TPMI with its modified SMs structure and its capability to transfer power from suppliers to the AC grid. In the second scenario, an experiment with partial shading is conducted by decreasing the rated power of one dc source while another remains at its full rated power.

5.6.1 Normal power operation

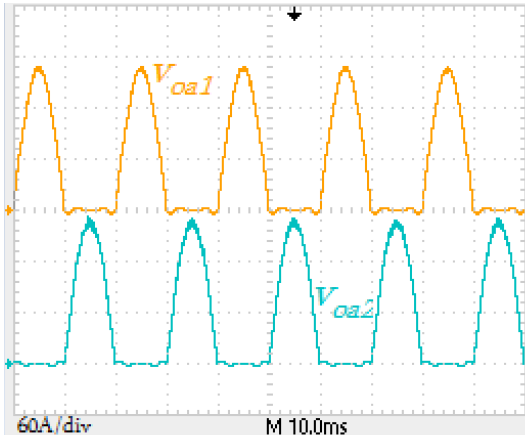
Both of the DC sources are being used at their rated power levels (i.e, 48 V and 16 A). The purpose is to validate TPMI's ability to deliver higher power levels with the revised structure of SMs. The measured power delivered to the grid by the TPMI inverter is illustrated in Fig 5.12a. In addition, the total output voltage and current of phase a are shown in Fig 5.12b.



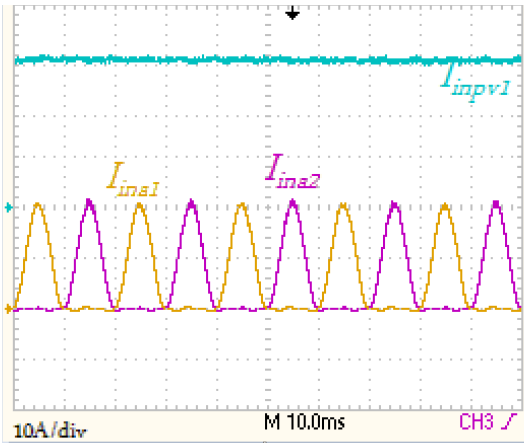
(a) Total TPMI power .



(b) Single-phase grid voltage and current.



(c) The output voltage of two successive SMs.



(d) PV modules input currents.

Figure 5.12: DC-to-AC inversion results from DC sources connected to the grid.

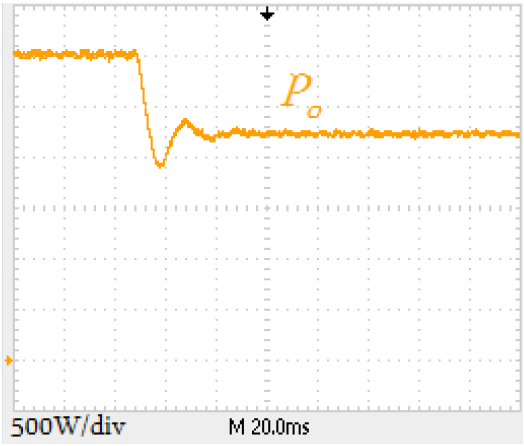
The output voltages generated by the first two SMs in phase a can be seen in Fig 5.12c, where the output switches S_o are responsible for controlling the operation of each SM for a half-cycle. The waveforms of two SMs at the bottom of the connection are not illustrated because they have the same response. The input currents of the two successive SMs in phase a, and the total input (PV) current delivered to the three-phase SMs, are shown in Fig 5.12d. These currents are measured from the first DC source.

5.6.2 Partial shading operation

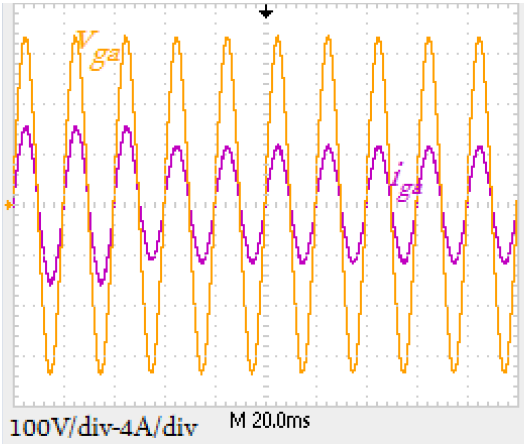
Partial shading is one of the common challenges faced by PV systems. An experiment has been conducted to validate the operation of the TPMI system when some PV modules were partially shaded. According to the schematic diagram in Fig 5.11, it will be assumed that the bottom source is shaded by producing half of its rated power, whereas the top source will continue to provide its full rating. As shown in Fig 5.13a, the shading of the lower supply causes the total TPMI power to be reduced by 25% compared to its value under the normal condition at t = 100 ms. The grid voltage and current for phase a are shown in Fig 5.13b, where the current decreases to 75% during partial shading.

The output voltages of the SMs in phase a are shown in Fig 5.13c. Before the moment of partial shading, the SMs' output voltages were identical. Then, the voltages of the unshaded SMs (i.e., 1 and 2) were increased, while the voltages of the shaded SMs (i.e., 3 and 4) were dropped by the same ratio. The sum of the SMs' voltage is required to synchronise with the grid, therefore the unshaded SMs increase their voltage to compensate for the drop in voltage of the shaded SMs. Lastly, Fig 5.13d presents the

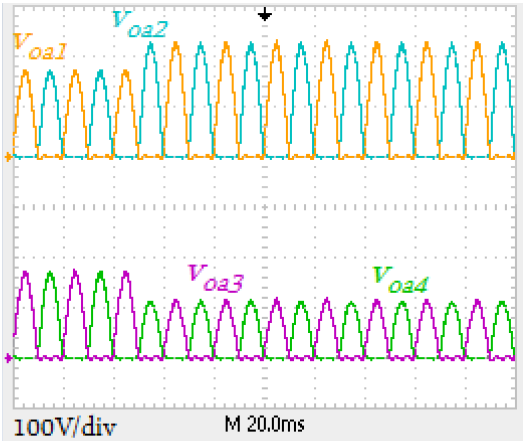
voltages and currents for both the unshaded and shaded power supply sources.



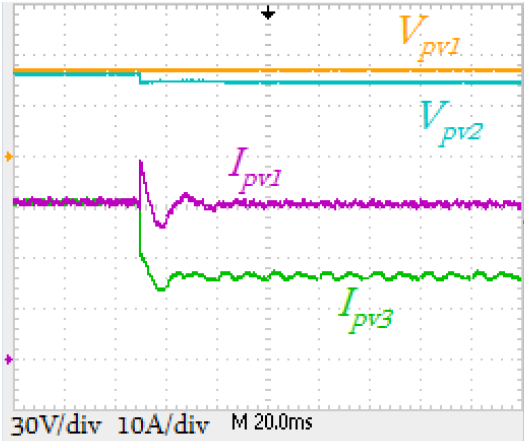
(a) Total TPMI power .



(b) Single-phase grid voltage and current.



(c) Output voltage of SMs in phase a.



(d) Power supplies' voltages and currents.

Figure 5.13: Experimental results during partial shading.

5.7 Comparison and Discussion

The modified structure of DISC and the classic one are compared according to modulation techniques, switch and diode counts, and power efficiency, as summarised in Table5.2. The modified DISC is operated using the HCM technique; consequently, the semiconductor losses are lower compared to SPWM. Another exciting benefit of

the modified DISC is that it uses two active switches, one of which is operated at grid frequency to reduce switching losses. In addition, it utilised a single gate driver, which reduced the size of the inverter and made it more compact.

Topology	Modulation Scheme	Switches / Diodes	power efficiency
Modified DISC SM	HCM	2 / 3	95.5%
Classic DISC SM	SPWM	3 / 3	94%

Table 5.2: Comparison of the modified DISC and the classic DISC topologies.

On the other hand, the efficiency of the modified DISC reaches 95.5% at 500 W, which is higher than the classic DISC structure, as shown in Fig 5.14.

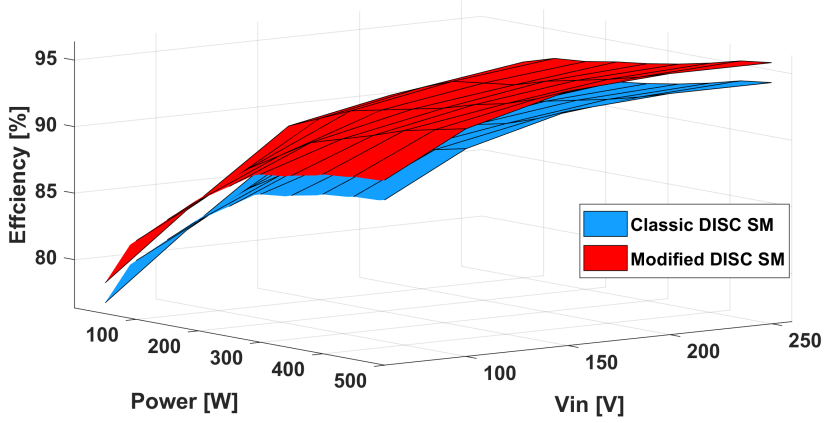


Figure 5.14: The efficiency comparison curve with DISC topologies for varying the power rating and the input voltage.

5.8 Chapter Conclusion

The fifth chapter proposes a new structure for TPMI based on its modified DISC SMs. A detailed description of the DISC structure and an explanation of the modulation

strategy for the proposed TPMI inverter are described and thoroughly discussed. Following this theoretical analysis, the DISC SM's operation was described. In addition, the PR controller is designed to be the main approach for regulating the output voltage and current. The simulation models are presented to demonstrate the operation and validate the theoretical analysis. The normal operation and partial shading conditions of a scaled-down experimental prototype were investigated and presented. Finally, the results were acquired from this experimental prototype, and these results confirmed the data from both the simulation and the theory.

Chapter 6

Conclusions and future work.

This chapter's overview of the work completed for this thesis places a particular focus on the significant contributions made by this thesis and how these contributions satisfy the objectives stated in the introduction. The key results and their implications are highlighted, along with the limits of the research conducted. Finally, the chapter concludes with recommendations for future research to increase the scope of this investigation and overcome its shortcomings.

6.1 Summary of work

This Ph.D. thesis was considered and focused on describing, validating, and analyzing the TPMI topology based on the DISC converter for the LSPV application. Many of its features make it suited for integrating the LSPV system with the utility grid, which has been the subject of this thesis:

- The TPMI is a structure comprised of stacked SMs that are linked together to increase the voltage at their terminals for a higher power rating and to provide

a direct connection to the grid without LFT.

- Fully modular architecture with a high level of redundancy to provide straightforward maintenance, installation, transportation, and rearrangement.
- TPMI has a single-stage power conversion that performs MPPT and regulates both input and output voltages in a single stage of power processing.
- A HFT can be placed within the SM to provide galvanic isolation. This prevents leakage of current and allows the input voltage to be stepped up or down.
- Its continuous input nature with low ripple guarantees that PV modules operate close to their MPP, hence maximising their energy harvesting.
- Because each PV module is independently connected to its SM, the distributed MPPT operation of the TPMI makes it possible to generate the maximum available power in partial shading conditions that are either uniform or non-uniform.

In Chapter 2, the most common MLC topologies employed in high-power PV applications are analysed and reviewed in detail. The classification was associated with MLC topologies, and each class was evaluated for the many advantages and drawbacks to determine the suitability of each converter topology for connecting the LSPV system to the grid. According to this analysis, the CHB and MMC types can be appropriate topologies for LSPV applications because they provide modularity, dependability, high power levels, and grid support. However, the CHB- and MMC-based topologies need further development to offer the required galvanic isolation, have superior SMs balancing, and operate distributed MPPT capabilities.

Alternatively, modular inverter structures that use power converters as their SMs are promising for interfacing PV systems into grids because they combine the merits of modularity, galvanic isolation, and bidirectional power flow to obtain higher voltages and boost overall efficiency. It investigated both the advantage of power converter-based modular inverters and the requirements of PV systems. Consequently, it inspired and directed the development of the proposed TPMI structure, which satisfies the fundamental criteria of PV applications in terms of insulation limits and partial shading operation. This Ph.D. thesis describes a configuration created in response to the aforementioned issues and concepts.

Chapter 3 began by describing the specifications of the fundamental SMs of the TPMI inverter and then focusing on the novelty of the DISC converter's structure, modulation, operation, steady-state average model, and the parameters of its eight passive components. The design of the DISC converter is a combination of SEPIC and CUK converters. It has a variable output range and continuous currents with low ripples on both the input and output sides. Its structure can embed compact a HFT to provide galvanic isolation and boost output voltage, which is advantageous for PV systems. The operation of the DISC converter was presented in CCM to define the energy transfer paths that flow from the input supply to the output side in each of the switch's "on" and "off" states. A novel average state-space model is addressed as part of the design process for the DISC converter, starting from mathematical analysis and obtaining the size of the DISC converter's passive components. The operation of the converter was then performed by obtaining simulation results. The results demonstrate that the theoretical equations accurately describe the DISC converter, allowing the proposed converter to be designed and implemented.

In Chapter 4, a novel TPMI topology was designed for high-power PV grid integration. The DISC-based converters are employed as its SMs. Firstly, the modulation technique and its connections to the SMs are presented. A step-by-step procedure is described for generating the output ac voltage and current for each SM. The operation of the DC/AC mode in which PV modules feed power into the AC grid is described in detail. Additionally, a control approach is based on two key parts: system control and SM-level control, which were introduced to determine the TPMI system performance. In system control, series-connected SMs are considered as a single central inverter, and the mismatches among the SMs' parameters are neglected. In this case, the uniform duty cycle and the same gate drive signal were fed to the single central inverter. At the SM level of control, each SM has its own controller so that it can compensate for slight differences in the values of the various parameters and keep an equal distribution of voltage and current among the SMs. The PR controller was used to tune at the grid frequency and add the closed-loop duty-cycle ratio because of its superior steady-state operation. The performance of the TPMI was validated using MATLAB/Simulink under normal, uniformed, and partial shading conditions to demonstrate that the inverter can deliver 13.47 kV of voltage into the AC grid. A scaled-down version of a 3 kW hardware prototype was built with a description of the test bench design. Several experiments were done to test the proposed inverter's performance in different weather conditions and its control strategy.

In Chapter 5, a new structure for TPMI was developed by making modifications to its DISC SMs. In contrast to the conventional DISC SM, which uses two output switches at high frequency and can increase conduction and switching losses, the new structure of DISC SMs has just one output switch that operates at grid frequency and has a

modest internal resistance. The DISC SM structure is modified by placing an active switch and two diodes on the output side. By replacing the two active switches in the classic structure of DISC SMs with diodes, the switching losses and complexity of the operation are both reduced. Moreover, the output side of DISC is included an additional external diode, which provides a current route and avoids a potential short circuit. The modulation methodology is discussed and its output voltage waveform of SMs is described. The major advantage of the modulation scheme is its capability to operate for only half of the cycle and no dc offset of SMs, which considerably reduces the switching and conduction losses of power devices. The operation principles for the new structure of DISC SM converters were defined for the on, off, and shutdown states. Once again, simulations carried out using MATLAB/Simulink and experimental results obtained with a scaled-down prototype validate the feasibility and operation of the TPMI with its newly redesigned structure of DISC SMs.

6.2 Research's key contributions

The research described in this thesis has made significant contributions to the field of power electronics in modular isolated inverters based on power converters, particularly for single-stage conversion, and three-phase inverter topologies used in high-power PV applications. More specifically, the key contributions of this thesis can be summarised and listed as follows:

- A comprehensive review of MLCs, including their circuit structure, the advantages they offer in LSPV systems, and the drawbacks they present. The classification depends on the common modular PV inverters used in high-power

PV plants to assist academic and industrial readers in identifying a suitable DC-AC inverter for their applications. (Chapter 2).

- The DISC, a new power converter, is proposed and used as submodules (SMs) in the TPMI inverter. It has a low ripple current at the input, a high power factor, and buck-boost capabilities; hence, the output voltage can be higher or lower than the input voltage. The proposed DISC SM is isolated by an HFT with one primary winding and two secondary windings for galvanic isolation and voltage amplification. This work also presents a novel mathematical model, state space representation, and its associations with the design processes of passive parameters for the DISC converter. The analyses help tune the control scheme for this kind of converter. The DISC SM topology was studied in the MATLAB simulation platform. (Chapter 3).

- Design a novel configuration of TPMI topology within the context of the LSPV grid-connected system that provides galvanic isolation and harvests the maximum available energy from the PV modules. The new modular inverter is superior to the traditional power converters for LSPV systems because TPMI is a descendant of both Sepic and Cuk in which the total input current is continuous, thus the inverter does not require a bulky electrolytic capacitor to operate. Consequently,the system's reliability is enhanced, and the MPPT operates at a constant voltage and current with minimal high-frequency ripples, which maximises the power harvesting from the PV modules. Additionally, the system control and SM level control were both provided as components of the control approach for TPMI. Although the control scheme is tailored for the TPMI, the concept can be extended to other inverters. Simulation studies and

experimental research have demonstrated the TPMI's dynamic properties. In grid-connected mode, the characteristics and capabilities of the TPMI under normal conditions, complete shading, and partial shading of PV modules have been investigated. Again, although these results were conducted on the selected TPMI, they help understand the benefits of using modular isolated inverters based on power converters in the context of the LSPV system. (Chapter 4).

- A redesign of the SM DISC structure for the TPMI is presented to reduce the number of switches operating at high frequency and conduction losses. The new structure is based on replacing the two output switches in the classic DISC SM with diodes and adding a new outer switch that operates at a frequency of 50/60 Hz to provide a current path when the output current is negative. Simulation and experiment results are discussed to illustrate the advantages and application possibilities of the TPMI with its redesigned DISC submodule structure. (Chapter 5).

6.3 Limitations of research

The MPPT technique was the main limitation of this investigation. Both the simulation and the experimental testing make use of a straightforward look-up table to facilitate the simplification of the MPPT controllers. As the purpose of this thesis is to investigate the innovative aspects of the suggested inverter, the design approach had a very tight focus on emphasising its distinguishing features. It is expected that taking additional key objectives into account, such as the MPPT controller, will greatly increase the input power provided by PV modules and then the system efficiency.

The point of grid connection was another limitation. The high grid impedance caused by the weak grid made it more challenging to tune the closed-loop control system. Moreover, the university campus where the experimental bench is kept has several other experimental studies, such as grid-tie converters and machines that can introduce low-order harmonics to the grid, which distort the voltage.
Lastly, the DC power supplies are employed to simulate PV modules in the corresponding modes of operation due to the limited budget available for this study.

6.4 Future work

There are various future aspects to build upon the research project described in this thesis. This section concludes with several recommendations for addressing the restrictions previously described as well as suggesting new ideas that can be implemented for the continued development of the proposed inverter.

6.4.1 Loss identification and efficiency improvement

The design of the LSPV plant is limited by the size and weight of the inverter, which are heavily determined by the operating frequency. Although a high switching frequency can efficiently reduce the size, this will bring some undesired features, such as increased core and winding losses and increased switching losses. Therefore, power losses are a key consideration. In the future, it could be possible to develop an analytical and mathematical model for inverter losses, which would lead to a design aimed at optimising efficiency. Interestingly, further research could look into areas such as core losses for transformers and inductors, switching and diode device losses,

thermal performance, and packaging.

6.4.2 Soft switching techniques

The size of TPMI can be reduced by operating the system at a high frequency, but at the expense of increased switching losses and reduced efficiency. Soft-switching has been used in other modular inverters to operate with lower switching losses and higher performance and efficiency. Therefore, future work could look into soft-switching to further increase the proposed inverter's efficiency.

6.4.3 MPPT algorithms

Within the scope of this study, The MPPT technique was simplified by a look-up table to operate and locate the SM output voltage reference values and total grid current faster than the system-level control. In MATLAB/Simulink, the MPPT is set as a look-up table that sends these values to the system and SM controllers. In the experimental work, these values were set in the code programmed in the TI DSP, and when the voltages from the DC supplies are changed, the code recognises that there is partial shading and adjusts the reference values of the controller based on the PV curves (look up tables). Consequently, the integration of an MPPT controller into the system controller would be an interesting research area. This would allow the controller to take into consideration both local and global points as well as increase its speed of tracking during solar transitions.

6.4.4 Transformer design

It would be beneficial to study the use of multi-winding transformers in light of the secondary side of the DISC converter is connected to two different converters. This will require additional design consideration, in particular when it becomes necessary to raise the switching frequency of the DISC converter.

6.4.5 Other Applications

In this thesis, the TPMI has only been proposed for LSPV systems. This inverter can be used for other applications, such as electric vehicles, wind generators, and battery charging.

Appendix A

A Dual-Isolated SEPIC/CUK Converter

A.1 Definition of coefficients

The coefficients in the numerator and denominator of the transfer function represented by Equation 3.30 can be defined as follows:

$$a_5 = (C_c*C_n*C_p*C_r*C_s^2*D*L_1*L_2*N*R - C_c*C_n*C_r*C_s^2*L_1*L_2*N*R) \quad \text{(A.1)}$$

$$a_4 = (2*C_c*C_p*C_r*C_s^2*D*L_1*L_2*N - 2*C_c*C_p*C_r*C_s^2*L_1*L_2*N) \quad \text{(A.2)}$$

$$
\begin{aligned}
a_3 = {} & C_c * C_p^2 * C_s^2 * D * L_1 * N^3 + R \\
& + C_c^2 + C_p * C_s^2 * D * L_1 * N^3 * R \\
& + C_c^2 + C_p^2 * C_s * D * L_1 * N^3 * R \\
& - C_c + C_p * C_r * C_s^2 * L_1 * N * R \\
& - C_c + C_p^2 * C_s^2 * D^2 * L_1 * N^3 * R \\
& - C_c^2 + C_p * C_s^2 * D^2 * L_1 * N^3 * R \\
& - C_c^2 + C_p^2 * C_s * D^2 * L_1 * N^3 * R \\
& - C_c + C_p * C_r * C_s^2 * D^2 * L_1 * N * R \\
& - C_c + C_p^2 * C_r * C_s * D^2 * L_1 * N * R \\
& - C_n * C_p * C_r * C_s^2 * D^2 * L_1 * N * R \\
& - C_n * C_p * C_r * C_s^2 * D^3 * L_1 * N * R \\
& - C_c * C_n * C_p * C_s^2 * D^2 * L_1 * N^3 * R \\
& - C_c * C_n * C_p * C_s^2 * D^2 * L_2 * N^3 * R \\
& + C_c * C_n * C_p * C_s^2 * D^3 * L_1 * N^3 * R \\
& + C_c * C_n * C_p * C_s^2 * D^3 * L_2 * N^3 * R \\
& + 2 * C_c * C_n * C_p * C_s^2 * D^3 * L_1 * N^3 * R \\
& + C_c * C_p^2 * C_r * C_s * D * L_1 * N * R \\
& - C_c * C_n * C_p * C_r * C_s * D^2 * L_2 * N * R \\
& + C_c * C_n * C_p * C_r * C_s * D^3 * L_2 * N * R
\end{aligned}
$$

$$
\begin{aligned}
a_2 = {} & 2 * C_c^2 * C_s^2 * D^2 * L_1 * N^3 \\
& - 2 * C_c^2 * C_s^2 * D^3 * L_1 * N^3 \\
& + 2 * C_c^2 * C_p * C_s * D^2 * L_1 * N^3 \\
& - 2 * C_c * C_p * C_s^2 * D^2 * L_2 * N^3 \\
& - 2 * *C_c^2 * C_p * C_s * D^3 * L_1 * N^3 \\
& + 2 * C_c * C_p * C_s^2 * D^3 * L_2 * N^3 \\
& + 2 * C_c * C_r * C_s^2 * D^2 * L_1 * N^3 \\
& - 2 * C_c * C_r * C_s^2 * D^3 * L_1 * N \\
& - 2 * C_p * C_r * C_s^2 * D^2 * L_1 * N \\
& + 2 * C_p * C_r * C_s^2 * D^3 * L_1 * N \\
& + 2 * C_p * C_r * C_s^2 * D^2 * L_1 * N \\
& - 2 * C_c * C_p * C_r * C_s * D^2 * L_2 * N \\
& - 2 * C_c * C_p * C_r * C_s * D^3 * L_1 * N \\
& + 2 * C_c * C_p * C_r * C_s * D^3 * L_2 * N
\end{aligned}
$$

$$
\begin{aligned}
a_1 = &-Z*C_c^2*C_p^2*D^4*N^3 \\
&+Z*C_c^2*C_p^2*C_p^2*D^3*N^3 \\
&-Z*C_c^2*C_p*C_s*D^4*N^3 \\
&+Z*C_c^2*C_p*C_s*D^3*N^3 \\
&-Z*C_C*C_p^2*C_s*D^4*N^3 \\
&+C_c*C_p^2*C_s*D^3*N^3 \\
&-C_r*Z*C_c*C_p^2*D^4*N \\
&+C_r*Z*C_c*C_p^2*D^3*N \\
&+C_n*Z*C_c*C_p*C_s*D^5*N^3 \\
&-C_n*Z*C_c*C_p*C_s*D^4*N^3 \\
&-C_r*Z*C_c*C_p*C_s*D^4*N \\
&+2*C_r*Z*C_c*C_p*C_s*D^3*N \\
&-C_r*Z*C_c*C_p*C_s*D^2*N \\
&+C_n*Z*C_p*C_s^2*D^5*N^3 \\
&-C_n*Z*C_p*C_s^2*D^4*N^3 \\
&+C_n*C_r*Z*C_p*C_s*D^5*N \\
&-C_n*C_r*Z*C_p*C_s*D^4*N
\end{aligned}
$$

$$
\begin{aligned}
a_0 = &-2 * C_c^2 * C_s * D^5 * N^3 \\
&+ 2 * C_c^2 * C_s * D^4 * N^3 \\
&- 2 * C_p * C_c^2 * D^5 * N^3 \\
&+ 2 * C_p * C_c^2 * D^4 * N^3 \\
&- 2 * *C_c * C_s^2 * D^5 * N^3 \\
&+ 2 * C_c * C_s^2 * D^5 * N^3 \\
&- 2 * C_r * C_c * C_s * D^5 * N \\
&+ 2 * C_r * C_c * C_s * D^5 * N \\
&+ 2 * C_p * C_r * C_c * D^5 * N \\
&+ 2 * C_p * C_r * C_c * D^4 * N \\
&+ 2 * C_p * C_s^2 * D^5 * N^3 \\
&- 2 * C_p * C_s^2 * D^4 * N^3 \\
&+ 2 * C_p * C_r * C_s * D^5 * N \\
&- 2 * C_p * C_r * C_s * D^4 * N
\end{aligned}
$$

$$b_7 = C_n * C_r * L_1 * L_2 * L_n * Z \\ C_c^2 * C_p^2 * C_s * N^2 \\ + C_n * C_r * L_1 * L_2 * L_n * Z \\ * C_c^2 * C_p * C_s^2 * N^2 \\ + C_n * C_r * L_1 * L_2 * L_n * Z \\ * C_c * C_p^2 * C_s^2 * N^2$$

$$b_6 = C_r * L_1 * L_2 * L_n * C_c^2 * C_p^2 * C_s * N^2 \\ + C_r * L_1 * L_2 * L_n * C_c^2 * C_p * C_s^2 * N^2 \\ + C_n * C_r * D * L_1 * L_2 * L_n * C_c^2 * C_p * C_s * N^2 \\ + C_r * L_1 * L_2 * L_n * C_c * C_p^2 * C_s^2 * N^2 \\ C_n * C_r * D * L_1 * L_2 * L_n * C_c * C_p * C_s^2 * N^2$$

$$
\begin{aligned}
b_5 = {} & C_c * C_n * C_p^2 * C_s^2 * L_1 * L_2 * N^2 * Z \\
& + C_c^2 * C_n * C_p * C_s^2 * L_1 * L_2 * N^2 * Z \\
& + C_c^2 * C_n * C_p^2 * C_s * L_1 * L_2 * N^2 * Z \\
& + C_c * C_p^2 * C_r * C_s^2 * L_1 * L_n * N^2 * Z \\
& + C_c^2 * C_p * C_r * C_s^2 * L_1 * L_n * N^2 * Z \\
& + C_c^2 * C_p^2 * C_r * C_s * L_1 * L_n * N^2 * Z \\
& + C_c * C_n * C_p * C_r * C_s^2 * L_1 * L_2 * Z \\
& + C_c * C_n * C_p^2 * C_r * C_r * C_s * L_1 * L_2 * Z \\
& - 2 * C_c * C_n * C_p^2 * D * L_1 * L_2 * N^2 * Z \\
& - 2 * C_c^2 * C_n * C_p * C_s^2 * D * L_1 * L_2 * N^2 * Z
\end{aligned}
$$

$$
\begin{aligned}
b_4 = {} & C_c * C_p^2 * C_s^2 * L_1 * L_2 * N^2 \\
& + C_c^2 * C_p * C_s^2 * L_1 * L_2 * N^2 \\
& + C_c^2 * C_p^2 * C_s * L_1 * L_2 * N^2 \\
& + C_c * C_p * C_r * C_s^2 * L_1 * L_2 \\
& + 2 * C_c * C_n * C_r * C_s^2 * D^2 * L_1 * L_2 \\
& + C_c * C_p * C_r * C_s^2 * D^2 * L_1 * L_2 \\
& + C_c * C_p^2 * C_r * C_s * D^2 * L_1 * L_2 \\
& + C_c^2 * C_n * C_s^2 * D * L_1 * L_2 * N^2 \\
& - 2 * C_c * C_p^2 * C_s^2 * D * L_1 * L_2 * N^2 \\
& - 2 * C_c^2 * C_p * C_s^2 * D * L_1 * L_2 * N^2 \\
& - 2 * C_c^2 * C_p^2 * C_s * D * L_1 * L_2 * N^2 \\
& + C_c^2 * C_r * C_s^2 * D * L_1 * L_n * N^2 \\
& + C_c * C_n * C_r * C_s^2 * D * L_1 * L_2 \\
& - 2 * C_c * C_p * C_r * C_s^2 * D * L_1 * L_2 \\
& - 2 * C_c * C_p^2 * C_r * C_s * D * L_1 * L_2
\end{aligned}
$$

$$
\begin{aligned}
b_3 = {} & C_c * C_p^2 * C_s^2 * L_1 * N^2 * Z \\
& + C_c^2 * C_p * C_s^2 * L_1 * N^2 * Z \\
& + C_c * C_p * C_r * C_s^2 * L_1 * Z \\
& + C_c * C_p^2 * C_r * C_s * L_1 * Z \\
& + C_c * C_n * C_p^2 * C_r * D^2 * L_2 * Z \\
& - 2 * C_c * C_n * C_p^2 * C_r * D^3 * L_2 * Z \\
& + C_c * C_n * C_p^2 * C_r * D^4 * L_2 * Z \\
& C_c * C_p * C_r * C_s^2 * D^2 * L_1 * Z \\
& + C_c * C_p^2 * C_r * C_s * D^2 * L_1 * Z \\
& - 2 * C_c * C_p^2 * C_s^2 * D * L_1 * N^2 * Z \\
& - 2 * C_c^2 * C_p * C_s^2 * D * L_1 * N^2 * Z \\
& - 2 * C_c^2 * C_p^2 * C_s * D * L_1 * N^2 * Z \\
& - 2 * C_c * C_p * C_r * C_s^2 * D * L_1 * z
\end{aligned}
$$

$$
\begin{aligned}
b_2 = {} & C_c * C_r * C_s^2 * D * L_1 \\
& - C_p * C_r * C_s^2 * D * L_1 \\
& + C_c^2 * C_p^2 * D^2 * L_2 * N^2 \\
& + C_c^2 * C_p^2 * D^4 * L_2 * N^2 \\
& - 2 * C_c^2 * C_s^2 * D^2 * L_1 * N^2 \\
& + C_c^2 * C_s^2 * D^3 * L_1 * N^2 \\
& + C_c^2 * C_p^2 * D^4 * L_n * N_4 \\
& + 2 * C_c^2 * C_s^2 * D^3 * L_n * N^4 \\
& - C_c^2 * C_s^2 * D^4 * L_n * N * 4 \\
& + C_p^2 * C_s^2 * D^4 * L_n * N_4 \\
& + C_c * C_p^2 * C_r * D^2 * L_2 \\
& - 2 * C_c * C_p^2 * C_r * D^3 * L_2 \\
& C_c * C_p^2 * C_r * D^4 * L_2
\end{aligned}
$$

$$
\begin{aligned}
b_1 = {} & Z * C_c^2 * C_p * 2 * D^4 * N^2 \\
& - 2 * Z * C_c^2 * C_p^2 * D^3 * N^2 \\
& + Z * C_c^2 * C_p^2 * D^2 * N^2 \\
& + R * C_c^2 * C_p * C_s * D^4 * N^2 \\
& - 2 * Z * C_c^2 * C_p * C_s * D^3 * N^2 \\
& + Z * C_c^2 * C_p * C_s * D^2 * N^2 \\
& Z * C_c * C_p^2 * C_s * D^4 * N^2 \\
& - 2 * Z * C_c * C_p^2 * C_s * D^3 * N^2 \\
& + Z * C_c * C_p^2 * C_s * D^2 * N^2 \\
& + C_r * Z * C_c * C_p^2 * D^4
\end{aligned}
$$

$$
\begin{aligned}
b_0 = {} & C_c^2 * C_s * D^5 * N^2 \\
& - 2 * C_c^2 * C_s * D^4 * N^2 \\
& + C_c^2 * C_s * D^3 * N^2 \\
& + C_p * C_c^2 * D^5 * N^2 \\
& - 2 * C_p * C_c^2 * D^4 * N^2 \\
& + C_p * C_c^2 * D^3 * N^2 \\
& + C_c * C_s^2 * D^5 * N^2
\end{aligned}
$$

A.2 Mathematical average model

The mathematical model of the DISC converter's state variables are shown below.

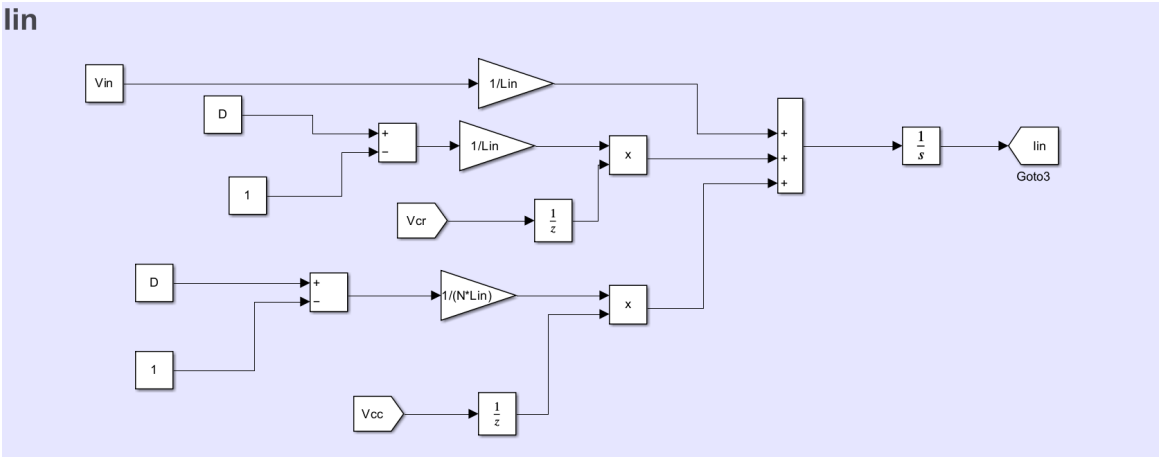


Figure A.1: The input current state variable's derivation.

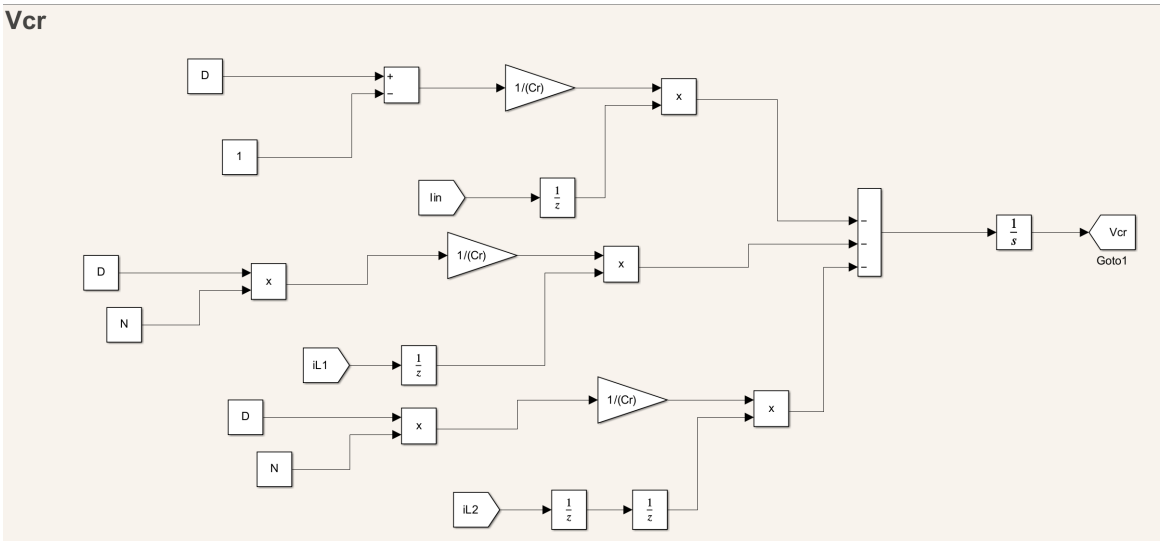


Figure A.2: The primary voltage state variable's derivation.

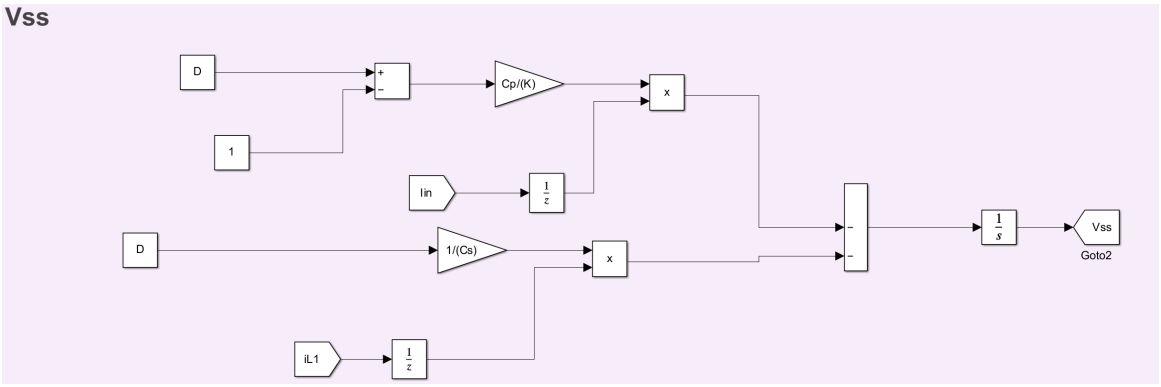


Figure A.3: The sepic voltage state variable's derivation.

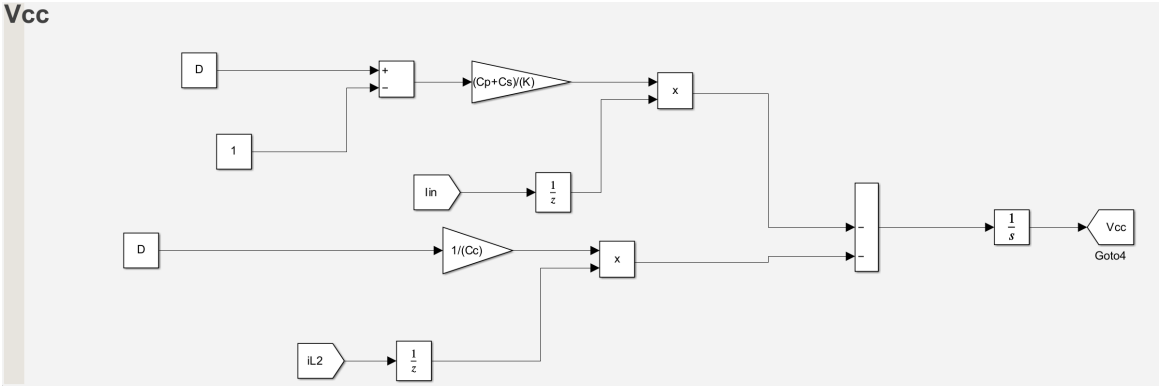


Figure A.4: The Cuk voltage state variable's derivation.

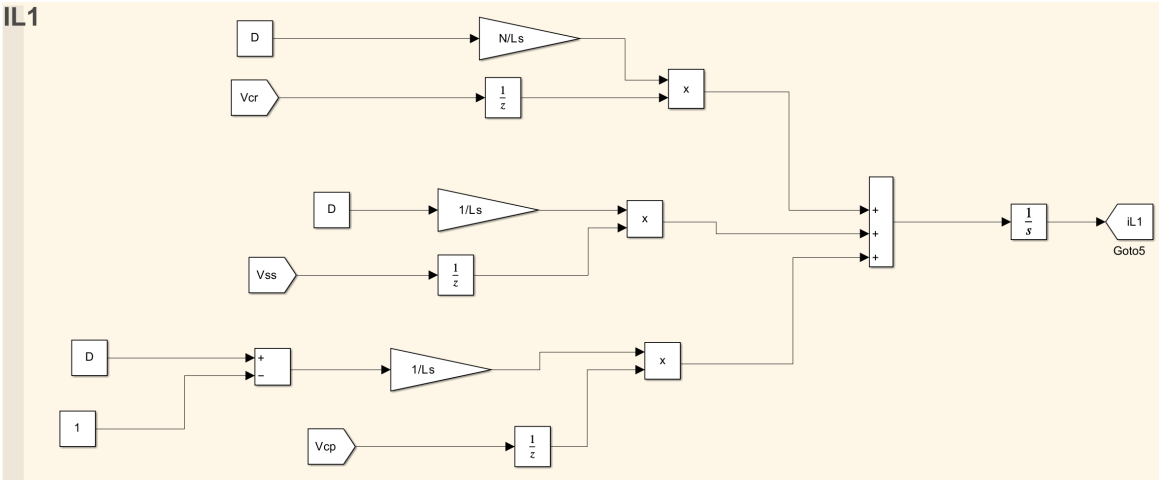


Figure A.5: The primary output current state variables derivation.

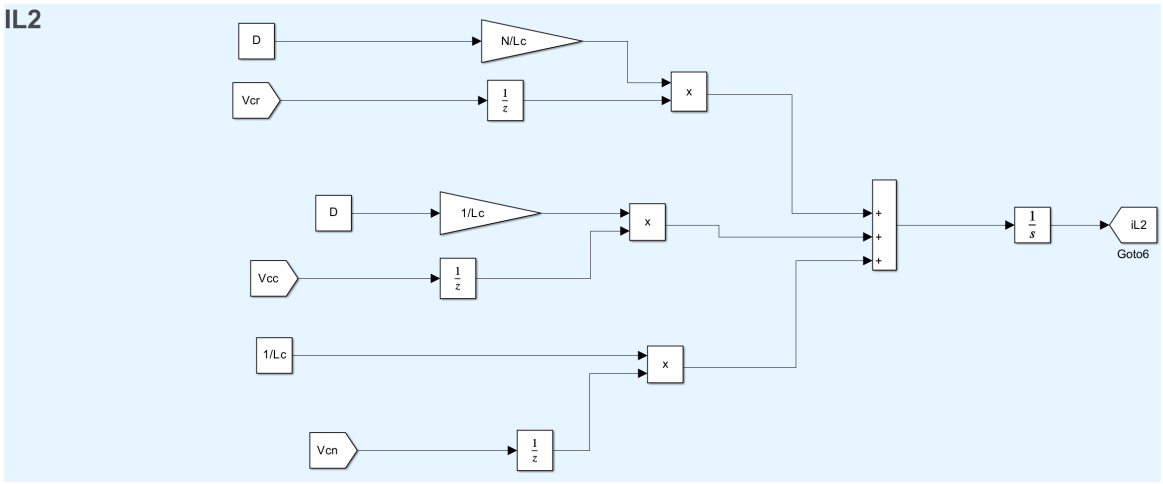


Figure A.6: The secondary output current state variables derivation.

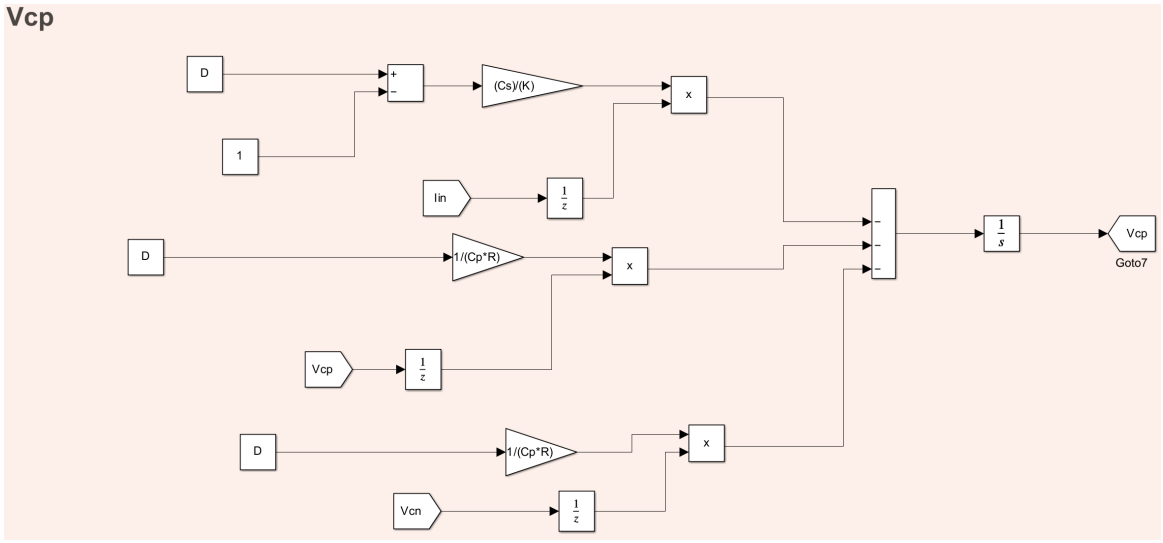


Figure A.7: The positive output voltage state variables derivation.

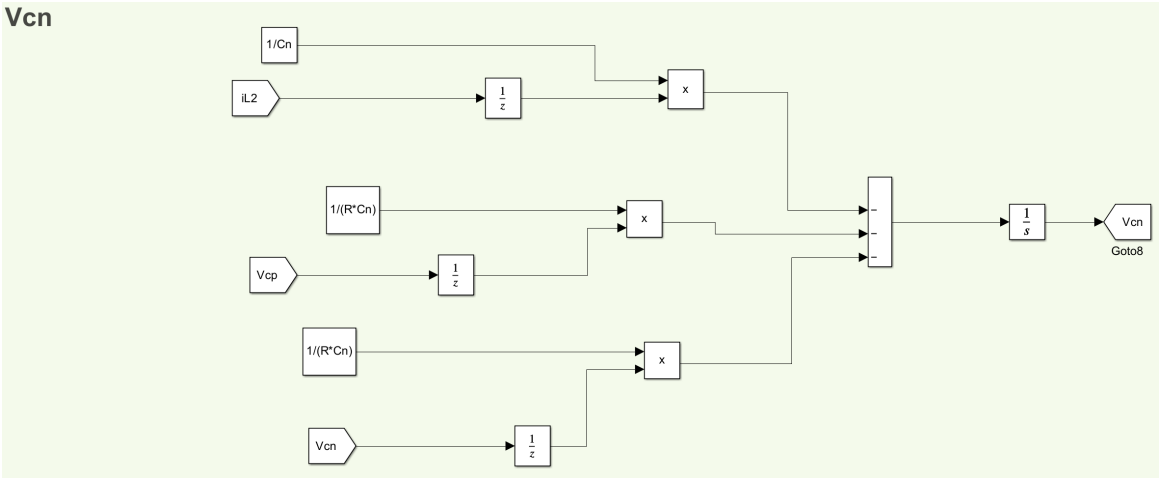


Figure A.8: The negative output voltage state variables derivation.

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