Tunable Electrical Field-Induced Metal-Insulator Phase Separation in $LiCoO_2$ Synaptic Transistor Operating in *Post-Percolation* Region

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Abstract

While mixed ionic-electronic conductors with metal-insulator transition (MIT) are promising candidates for designing neuromorphic computing hardware, the fundamentals of resistive switching in these materials are yet to be well understood. This work studies the switching mechanism of the three-terminal nonvolatile redox transistor (NVRT) containing the $LiCoO_2$ (LCO) channel layer with tunable preferred crystallographic orientation. We used atomic force microscope nanotomography to reconstruct the 3D conductance map of NVRTs, that reveals the applied gate electric-field induces the MIT via reversible phase separation in the LCO channel layer, with the nonequilibrium thermodynamics analytical model providing validation to this mechanism. By operating in the *post-percolation* region, the memory properties can continuously adjust the conductance states of NVRTs. The percolation conductance mechanism via the metallic LCO phase ensures the exceptional linearity and reproducibility of conductance modulation, whereas the field-, rather than current-, induced transition results in the low energy consumption replicating key features of the living neural cells.

Keywords

Synaptic transistor, phase separation, insulator-to-metal transition, $LiCoO_2$

1. Introduction

Resistive memristors (RMs) can process information stored in form of electrical resistance which depends on the history of the electrical stimulation signals. The neuromorphic architectures based on RM units in a crossbar array architecture can therefore enable the one-shot operation of matrix-matrix multiplications [1] and the parallel reading of stored data through 'compute-in-physics' [2], avoiding the shuttling of data between the processing and memory units in the conventional von Neumann chip architectures [3,4]. By taking advantage of multi-level analog states, in-memory computing capability, and parallel processing – all key characteristics of a living brain, integrated chips that use RM units continue to dramatically improve in terms of memory density, data bandwidth and energy efficiency. However, the multi-level analog states have to rely on the linear nature of the tunable conductance/resistance in RM units, which is still a major challenge for the hardware neural network system where highly repeatable operation is necessary.

The linearity of conductance change in RMs stems from their resistive switching mechanisms. RMs fall into different categories according to the switching mechanisms [5], among which the valence change memories (VCMs) and electrochemical metallization memories (ECMs) are the two most investigated ion migration-based electrochemical redox memristors [6,7]. These ion migration-based RMs can mimic the percolation processes [8-10]. The intriguing nature of the percolation model is that in the *post-percolation* region where a scaling relationship holds, the conductivity can be varied through smooth and continuous transitions with small variations in the percolation network [11,12]. This fundamental physical law provides a great opportunity for ion migration-based RMs to deliver good and predictable conductance linearity. However, in conventional VCMs, the migration of oxygen vacancies often required a high electric field to overcome the energy barriers [13]. Meanwhile, in ECMs, the reversible formation and rupture of the conductive filaments rely on the migration of foreign cations (e.g. Cu^{2+}/Ag^{+}) [14], and thereby the uncontrollable formation and rupture of metallic filaments in ECMs deteriorate the resistive switching performance [15-16]. As most electrochemical redox memristors rely on the complex filament formation process within the switching layer (or in the interface), the uncertainty of migration ion species makes the switching performance difficult to predict [6]. These hinder the reversibility, accuracy, and symmetry of the

transition, that are detrimental to the performance of neuromorphic devices, where analog switching with finely adjustable resistive states is desirable.

Lithium-ion migration-based memristors have recently become emerging RMs. Lithium-ion has the smallest size among all metal cations, which has made it a perfect charge carrier for energy storage devices such as lithium-ion batteries. Compared to other metal cations or oxygen anion migration that creates a switching filament [17], much lower energies are required to drive Li ions' intercalation into battery materials. Additionally, one of the most striking outcomes of lithium intercalation/de-intercalation within transition-metal-oxide crystal lattices is that the resultant metal-insulator transition (MIT) [18] can change its conductivity by several orders of magnitude [19-21]. Therefore, recently, lithium-transition metal oxide materials, including Li_xCoO_2 [22], $Li_xTi_yO_2$ [23], $LiFePO_4$ [24], $LiLaTiO_3$ [25], and $LiNiO_x$ [26], have been studied as the resistive switching layer for RMs simply by adjusting the lithium stoichiometry and phase spatial pattern. These studies have shown that Li ions-based memristors have enormous potential as artificial synapses for neuromorphic computing with high density, low power consumption, and fast operating devices, offering applications beyond energy storage. The resistance switching behaviors are suggested to be controlled by the migration and accumulation of Li ions without large structural distortion, and therefore it is highly analogous to the transmission of neurotransmitters from the presynaptic neuron to the postsynaptic neuron. However, understanding of the resistive switching mechanism in $LiCoO_2$ and $Li_xTi_5O_{12}$, which show an MIT transition upon the lithium intercalation/extraction, has undergone long historical debates since the initial report of analog battery materials ($NaCoO_2$/ $LiCoO_2$) as resistive switches [27,28].

In 2011, Moradpour et al. reported the possibility of $LiCoO_2$ (LCO) as a resistive memory material for the first time [28]. Conductive Atomic Force Microscope (c-AFM) was used to measure the resistive switching behavior of conductive AFM tip/ LCO/$Si_{p^{++}}$ micro-nano battery memristor [29-30], and the authors proposed that the resistive switching phenomenon originates from the redox reaction between Co and H_2O inside the LCO-tip meniscus. This mechanism was also accepted in the follow-up reports [29,31]. However, Fuller et al. fabricated the first three-terminal $LiCoO_2$-based RM device to mimic the stimuli-responsive nature of neural networks [32], claiming that the resistive switching originated from the MIT of LCO switching layer due to the change of the lithium content that was locally driven by the electric field. This contradicted the previously proposed mechanism of interfacial redox reaction between Co and H_2O. Later, the diffusion of Li ions driven by the electric field and the interfacial reaction between the LCO switching layer and silicon oxide trapping layer

were confirmed by Nguyen et al. [30], revealing the necessity of a dielectric silicon oxide trap layer for the LCO resistive switching. Hu et al. [33] also found that a suitable thickness of the SiO_2 trapping layer can reduce the total electromotive force field [34] and prevent the backward migration of lithium ions to LCO. Recently, the symmetric two-terminal memristor based on the MIT of lithium titanate oxide has been demonstrated as a promising artificial synapse [23], in which an electric field-induced non-equilibrium phase separation was proposed as the underlining switching mechanism. Although this provides new insights toward the MIT phase separation switching model for LCO [35], the phase separation pattern hasn't yet been verified experimentally in real space and nanoscale spatial resolution due to the lack of analytical tools. Moreover, the sharp MIT transition during the phase separation seems to be contradictive to the obtained decent tunability and linearity of conductance [23]. Significantly, the interplay between ion migration/redistribution dynamics and metal-insulator transition [36], which defines the memristive behavior and directly affects the performance of Li ions-based devices [17,23], has not yet been explained by existing switching theoretical models.

In this work, we fabricate the three-terminal memristive transistor with LCO switching layer as a close-to-ideal model to explore the switching fundamentals in lithium-ion based RMs. The system allows also control of the lithium diffusion dynamic and permittivity of the switching layer by changing the LCO crystal orientation. We found that the devices with different LCO crystal orientations show different switching threshold voltage (switching energy barrier), conductance linearity and retainability. The resistive switching of the NVTRs derives from the percolation and MIT phase separation of the LCO layer (bulk effect) and the trapping of lithium ions by the dielectric SiO_x layer (interfacial effect). The percolation that drives the conductivity gain, as well as the interfacial ion trapping, stems from the localized redistribution of lithium ions. This fundamentally eliminates the internal stress variation caused by the repetitive formation and rupture of conductive filaments within the switching layer, eliminating the strain-induced damage to devices during cycling. The designed NVRTs operating in the *post-percolation* region provide good linearity of conductance modulations. Significantly, the proposed electric field-induced nanoscale MIT phase separation and percolation mechanism are directly verified by 3D nano-tomography AFM in good agreement with the analytical solutions via nonequilibrium thermodynamics. These findings pave the way for mixed ion-electron conductors with MIT as a powerful platform for the development of synaptic transistors with tunable electrical properties.

2. Results and discussion

2.1 Three-terminal NVRT with tunable switching characteristics

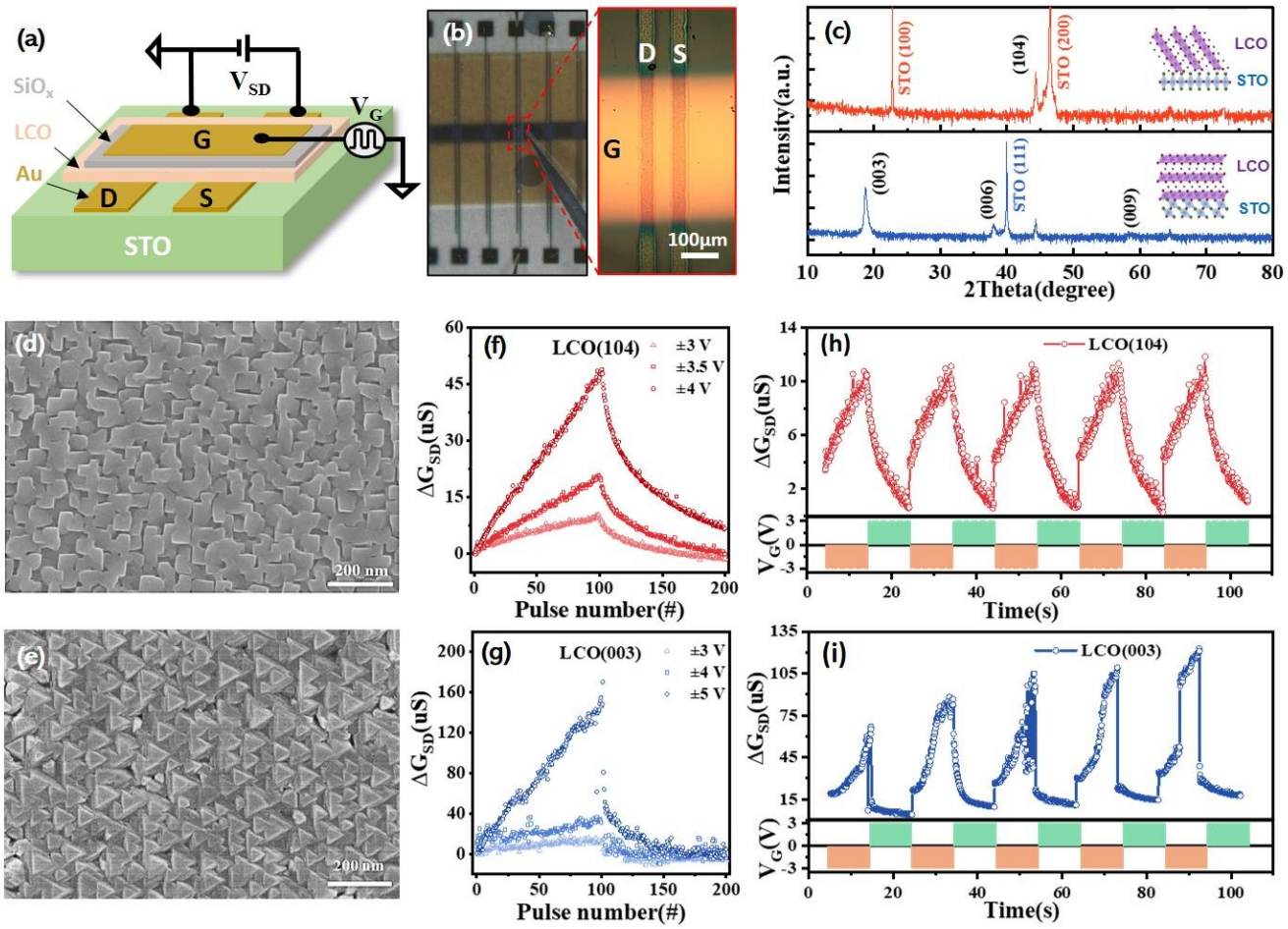

Figure 1. (a) The sketch of a three-terminal NVRT unit. (b) Top view of the NVRT unit array. (c) XRD patterns of LCO channel layer with (104) and (003) preferred orientation. (Insets - the crystal structure models showing epitaxial relationships) (d) and (e) SEM images of surface morphology of LCO channel layer with different orientations. (f) and (g) The long-term potentiation (LTP) and long-term depression (LTD) curves of LCO-(104) and LCO-(003) NVRT, where training pulses consisting of 100 negative pulses (200 ms) followed by 100 positive pulses (200 ms) at the voltages specified in the graph. (h) and (i) Reproducible analog channel conductance modulation of LCO-(104) and LCO-(003) NVRT, where 50 negative (-3 V, 200 ms) and 50 positive pulses (3 V, 200 ms) are performed.

We fabricated the NVRT device as shown in **Figure 1**a using LCO as the switching channel layer, and silica as the gate ion trapping layer. The trapping effect [30,33] of the amorphous silica gate dielectric layer was evaluated by testing the robust switching behavior in the $LiCoO_2/SiO_x/Si$ stack (see supplementary information, SI, section 1). The advantage of this NVRT device structure is that the direction of the applied 'write' electric field is perpendicular to the direction of the 'read' electric field (between source and drain electrodes). This drastically reduces the crosstalk of data writing and reading processes and hence considerably improves the device's robustness. Figure 1b is the top view photo of an NVRT unit during the electrical performance tests, the drain electrode is grounded, the

voltage pulses (V_G) are applied to the gate electrodes, and the small DC voltage (V_{SD}) was applied between the source and drain for the conductivity measurements. Additionally, to understand the effects of anisotropic lithium-ion transportation on the switching performance of this LCO-based memristor [22,37], we employed two orientations of $SrTiO_3$ (STO), (100) and (111) signal crystal substrates [38-40], to control the orientation of LCO channel layers. The thickness of the channel layer was targeted to be ~70 nm (SI, Figure S4). The XRD pattern in Figure 1c shows that the LCO channel layer with (104) and (003) preferred orientations are obtained on the STO (100) and (111) substrates respectively. The SEM images in Figures 1d and 1e further confirmed the characteristic crystal faces on different LCO crystal planes. The LCO channel layer surface consists of 'cubic' crystal facets has (104) preferred orientation, while the one with 'triangle' crystal facets is the (003) preferred orientation [41]. This is consistent with the XRD results in Figure 1c. Moreover, this epitaxial relation between LCO and STO substrate is well maintained at the nanoscale boundary between the Au source/drain bottom electrodes and channel (SI, Figures S6 and S7), facilitating the further scaling down of the NVRT device.

Figures 1f and 1g are the long-term potentiation (LTP) and long-term depression (LTD) curves of LCO-(104) and LCO-(003) NVRT. In each cycle, the changes in source-drain conductance (ΔG_{SD}) were recorded after applying the negative "set" voltage pulses during the LTP, followed by the positive "reset" pulses with the same amplitude and width during the LTD. It is worth noting in Figure 1g that, at the pulse amplitude of 4 V, the ΔG_{SD} of LCO-(003) is about 1.88 times compared to its initial conductance value G_{SD0} ($\Delta G_{SD}/G_{SD0}$ ~1.88) after the 100^{th} negative voltage pulse. However, when the voltage pulse amplitude increases to 5 V, a drastic modulation of NVRT conductance can be observed in Figure 1g, the $\Delta G_{SD}/G_{SD0}$ value increases to about 10 after the 100^{th} negative voltage pulse. By contrast, as shown in Figure 1f, the LCO-(104) NVRT not only has a lower pulse amplitude threshold ($\Delta G_{SD}/G_{SD0}$ ~16 under the plus amplitude of 4 V) but also shows a better linearity and retention capability for conductance modulations compared to the LCO-(003) (see SI, section 3). Importantly, the "linearity coefficient" of LTP of LCO-(104) is about 0.11 (see SI, section 4), which is smaller than the values reported recently in metal oxide analogue memristors, such as $NaNbO_3$ [42] and WO_3-based [43]. We also noticed that the LTD process shows much less linearity compared to the LTP. This nonlinearity is closely related to the different lithium-ion migration dynamics in the NVRTs, which are discussed in detail in SI, section 5. Figures 1h and 1i are the five cycles of LTP and LTD curves. The obtained channel conductance in LCO-(003) NVRT shows poor symmetry and an abrupt increase of conductance during LTP due to the lithium congestion effect [43]. The LCO-(104) device shows good linearity and symmetry even when the

identical gate pulses were used in both potentiation and depression processes. This high linearity and symmetry are essential indicators for synaptic transistors to accurately control and predict learning processes in hardware neural networks. Overall, we demonstrate that the LCO NVRT with a low switching voltage, as well as a highly linear switching operation, can be obtained by adjusting the crystal orientation of the LCO channel layer.

2.2 The effects of anisotropic lithium migration within the switching layer

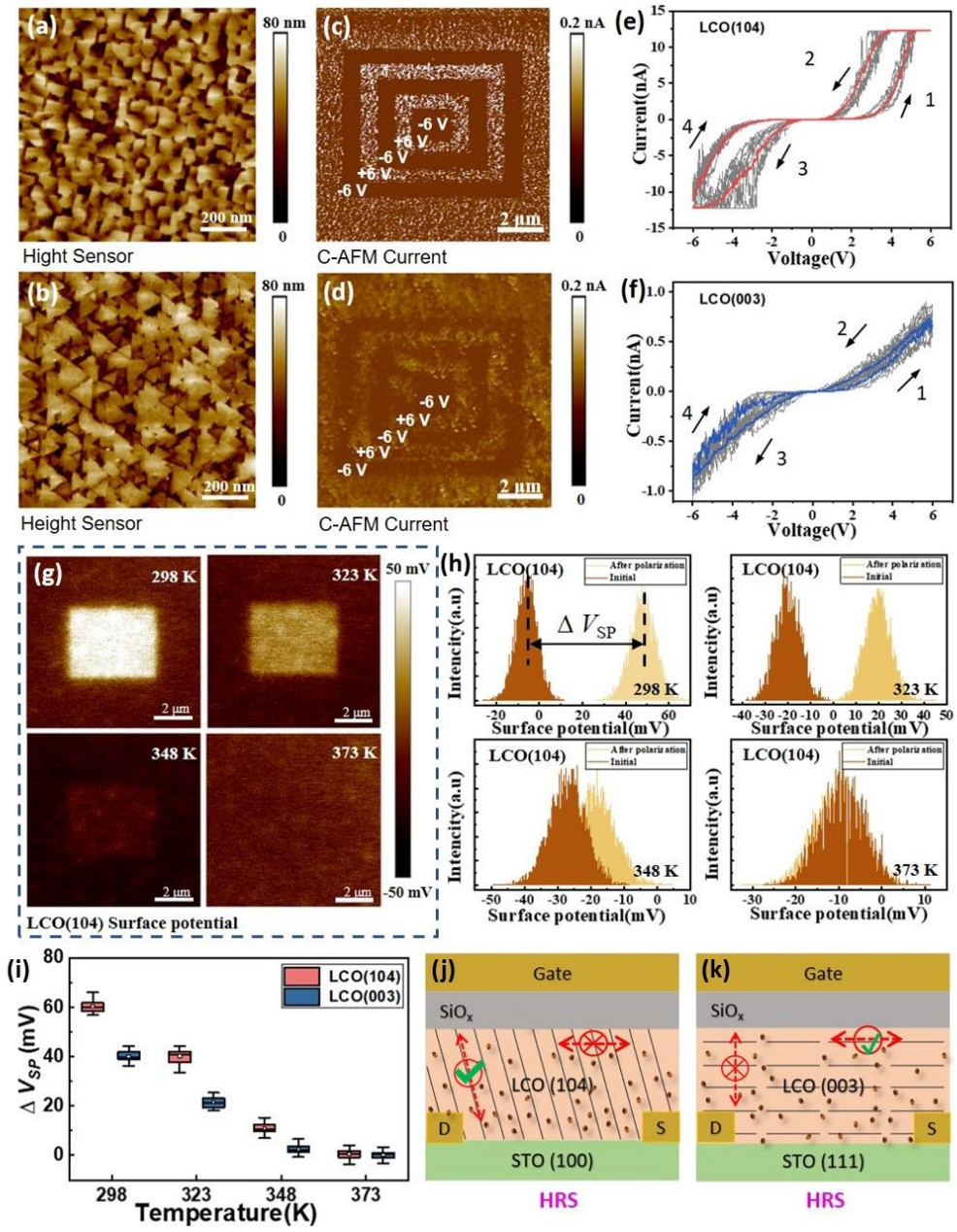

Figure 2. (a, b) AFM surface topography images, (b, c) C-AFM conductivity switching patterns, (e, f) multi-cycled *I-V* curves. (g) KPFM surface potential images of a square polarization region on LCO surface at temperatures of 298K, 323K, 348K, 373K. (h) The statistics of four surface potential distributions of polarized and unpolarized regions after different temperatures initiated the destruction of polarization corresponding to Figure g. (i) The changes of the average value of Δ V_{SP} at different temperatures for LCO-

(104) and LCO-(003) surface. (j) and (k) The sketching of ion migration/redistribution models of LCO-(104) channel layer and LCO-(003) channel layer.

The electrical performance characterizations in Figure 1 show that the NVRT unit with LCO-(104) channel layer exhibits a smaller switching voltage and better retention capability compared to LCO-(003). To further understand this difference, c-AFM and temperature-dependent KPFM were introduced to study the lithium diffusion dynamic under the applied electric field and thermal field in LCO-(104) and LCO-(003).

The AFM topography images of LCO-(104) and LCO-(003) in **Figures 2**a and 2b show numerous cuboidal and triangular domains respectively, which is consistent with the SEM images in Figures 1d, e. The c-AFM images in Figures 2c and 2d were recorded after electrical tip-writing using the concentric square method [28]. As shown in Figure 2c, the c-AFM image of LCO-(104) has a clear boundary of high and low resistance state areas, indicating good stability and repeatability in resistance switching behaviour. However, the c-AFM image on the LCO-(003) surface, as seen in Figure 2d, shows a blurred conductivity distribution map. Meanwhile, as shown in the *I*-*V* curves in Figures 2e and 2f, both films show similar and robust bipolar resistance switching behaviours, and the switching is but LCO-(104) has a higher current response (higher conductivity) along the direction perpendicular to the film surface compared to LCO-(003). These results confirm that the conductivity modification is easier to achieve along the out-of-plane direction in LCO-(104). We present the localized Li-ion migration models under the applied electric field in Figures 2j and 2k. The LCO-(104) film has Li-ion transport channels (Co-O octahedra interlayers) almost perpendicular to the film surface, and the low lithium/electron diffusion energy barriers within the two-dimensional Co-O layers [44] result in the low switching write voltage of LCO-(104) NVRT. In contrast, the LCO-(003) film surface is parallel to the Li-ion channels, the local redistribution of Li-ions needs to be realized via the diffusion of Li-ions along the grain boundaries, as shown in Figure 2k. Along the grain boundaries, the high diffusion energy barrier of lithium-ions and low conductivity of electrons [45] both contribute to the high switching voltage of LCO-(003) NVRT.

The surface potential retention was assessed to understand the stability of the NVRT devices toward thermal destruction. Inside a 10×10 μm scanning region, a 5×5 μm square region was polarized by applying a +6 V bias to the substrate. Afterwards, the surface potential images of the LCO-(104) films were recorded at different destructive temperatures, as shown in Figure 2g. As the temperature increases, the average value of the surface potential difference (ΔV_{SP}) between the central region and

marginal region tends to reduce leading to the destruction of the recorded pattern. The statistical distributions of the surface potential of polarized and unpolarized regions under different temperatures were shown in Figure 2h (see also SI, Figure S4). Figure 2i shows the temperature-dependent ΔV_{SP} for LCO-(104) and LCO-(003). From the figures, one can find that the LCO-(104) film displays better retention and higher ΔV_{SP} at each temperature than LCO-(003) film. For example, at 348 K, the average value of ΔVSP of LCO-(003) is close to zero eV, while that of LCO-(104) is nearly 10 mV. This indicates the LCO-(104) NVRT has higher retainability than LCO-(003) NVRT. The schematic diagrams are shown in Figures 2j and 2k. Under the thermally induced destruction of the recorded potential pattern, the Li-ions in LCO-(104) NVRT redistribute slowly in the horizontal direction (between source and drain) due to the pinning effect of Co-O layers, while the Li-ions flow relatively 'free' between the source and drain in the LCO-(003) NVRT. Therefore, the LCO-(104) NVRT shows much more symmetric LTP and LTD curves in Figures 1f-i. Most importantly, a much better retention capability can be found in the LCO-(104) NVRT during the conductance depression training.

2.3 The electric field-induced MIT phase separation and percolation of metallic phase

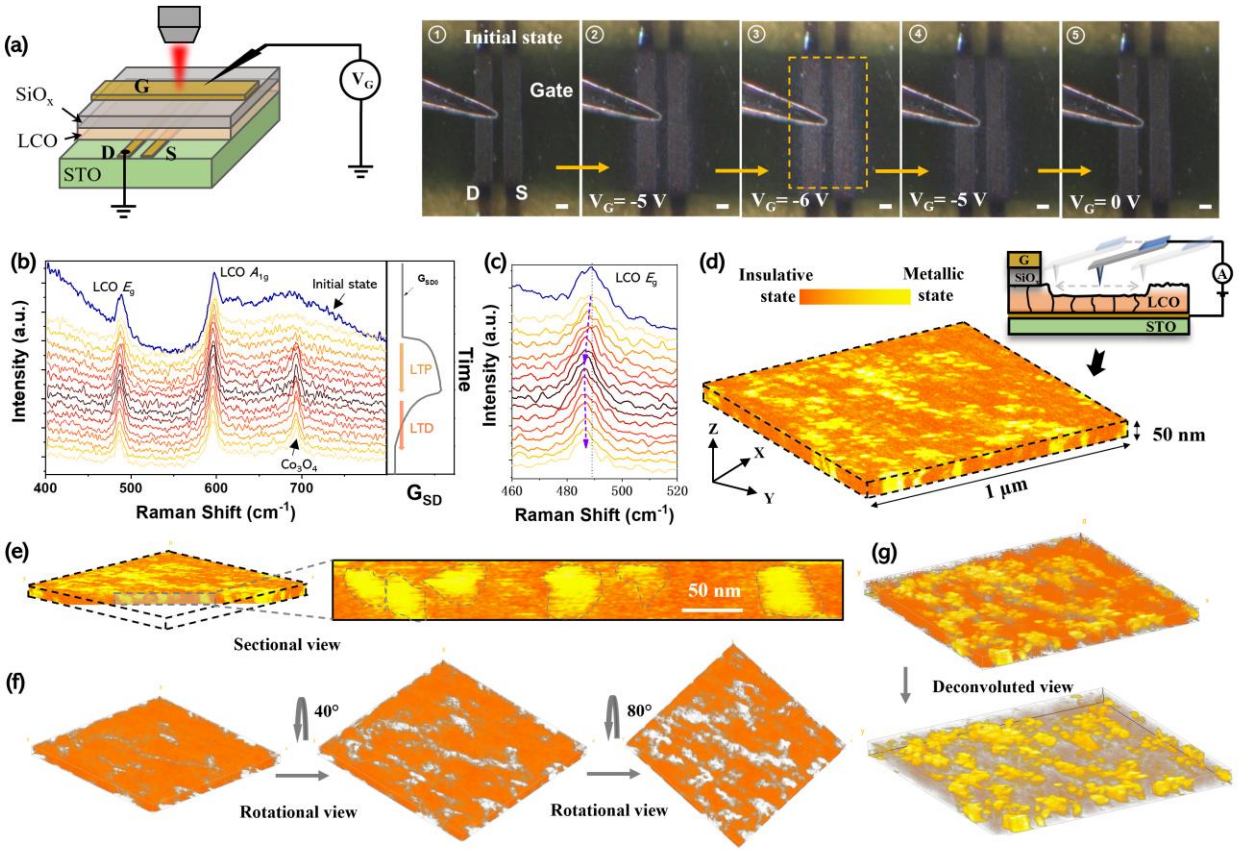

Figure 3. (a) Schematic diagram of the optical microscope and optical images of the device with LCO-(003) during the LTP test at different gate voltages. The gate voltage pulse is a triangular pulse with an amplitude of -6 V and a width of 2 seconds. The inset scale bars are 50 μm. (b) *in situ* Raman full range (400-800 cm^{-1}) spectra and (c) E_g peak shifting of LCO-(104) channel layer during the

LTP and LTD tests. A_{1g} band shifting can be found in SI, section 7. (d) Reconstructed 3D distribution of metallic and insulating LCO phases for LCO-(104) channel layer. (e) Section view, (f) rotation view, and (g) deconvoluted view of metallic and insulative phases inside the LCO-(104) channel layer corresponding to Figure 3d. (The full video recording can be found in SI).

To reveal the microscopic nanoscale switching mechanism and dynamics in the LCO transistors, we recorded the switching process of an NVRT unit using *in situ* optical spectroscopy as shown in **Figure 3**a. From the optical images, one can find that a metallic phase with high reflectivity [46] (the shinning area) underneath the gate electrode reversibly appears during the large negative voltage (-6 V) polarization cycles (The full video can be found in the supplementary information, VIDEO 1). This indicates that the MIT phase transition and relaxation [19,47] of LCO layer are happening under voltage polarization. *In situ* Raman spectroscopy was used to further reveal the phase transition of the LCO-(104) NVRT under gate voltage polarizations during LTP and LTD tests. As seen in Figures 3b and 3c, the initial LCO E_g and A_{1g} peaks blue shift to the lower wavenumber region during the LTP test (negative gate voltage polarization), and then moving back to the high wavenumber region during the LTD, unambiguously indicating the reversible phase transition between the lithium-deficient LCO metallic phase and lithium-rich LCO insulative phase [48,49]. The peak position shifting of E_g and A_{1g} bands are summarized in SI, Figure S15. Besides, it's also worth noting that, when the device conductance is approaching the saturation value in LTP training, further applying the negative gate pulses results in the formation of the Co_3O_4 phase (Raman peak ~ 691 cm^{-1}). This implies that the NVRTs should be operated at the linear LTP conductance modulation region to avoid the over-extraction of lithium from the LCO lattice which will cause the irreversible phase transition.

This reversible phase transition in the LCO materials can be realized by either the intercalation/de-intercalation of lithium through the solid-state electrochemical reaction with the SiO_x layer (long rang diffusion), or the localized redistribution of lithium (inside or between the LCO grains). To verify which of these assumptions is correct, we introduced a 3D tomography conductive AFM [50] to explore the subsurface conductive properties in the LCO-(104) channel layer. As shown in Figure 3d, 3D tomography conductive AFM uses a relatively stiff (spring constant of ~100 N m^{-1}) conductive diamond-coated tip to 'scratch' the LCO channel layer after negative gate voltage polarization. During the scratching, a high force of ~10 μN was applied to the tip to 'dig' into the bulk region of the LCO layer, and the Z scanner feedback gain was reduced to achieve a 'loose' feedback loop. The tomographic conductivity maps were recorded during the tip milling through the LCO layer eventually reaching the substrate. By reconstructing the tomographic conductive maps along the Z direction, the conductivity distribution inside the LCO layer can be revealed. The

obtained 3D reconstructed conductivity mapping is shown in Figure 3d. From the figure, it is found that after the LCO layer was polarized and switched to the low resistance state by a negative gate voltage, some active grains (bright yellow colour) show a high current signal (metallic LCO phase), while the rest of regions show low conductivity (insulative LCO grains and the grain boundaries that are also of low conductivity) with sparse conductive areas. The 3D sectional view in Figure 3e shows the internal distribution of the conductive grains. Interestingly, each of the metallic grains serves as a "conductive hotspot" of the LCO channel layer (see the full video in the SI, VIDEO 2). The 3D rotational view of insulative components in Figure 3f further indicates that the metallic grains serve as the filaments, not only "intersecting" the whole LCO layer, but also "interconnecting" with each other to form a percolated conductive cluster [51,52]. Meanwhile, from the deconvoluted view in Figure 3g, one can see that the metallic phase grains are interconnected in the lateral direction, building up a conductive network along the in-plane direction (between the source and drain electrodes), and thereby increasing the G_{SD}.

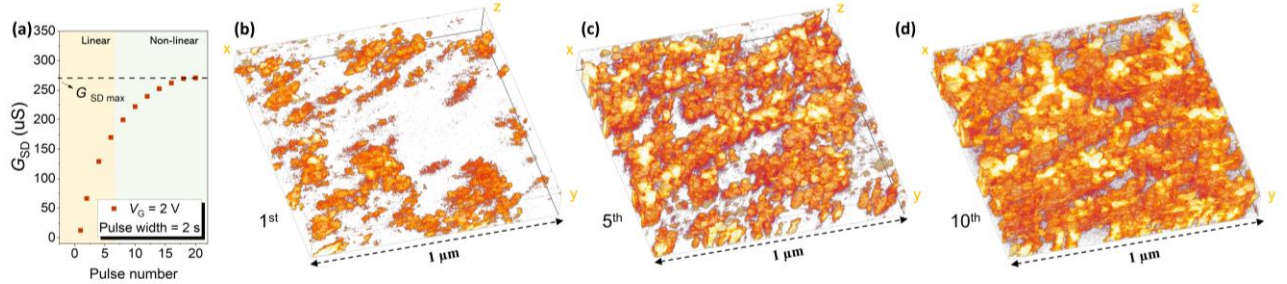

Figure 4. (a) G_{SD} of LCO-(104) NVRT as a function voltage plus number during the Long-term potentiation (LTP). The applied gate voltage pulse is 2 V with a width of 2 seconds. (b), (c) and (d) 3D distribution of conductive regions in LCO-(104) layer after 1st, 5th and 10th gate pulse cycles, respectively. The zero current regions were masked out in the 3D reconstruction maps.

We further reconstructed the network of metallic LCO grains inside the LCO-(104) layer after a set of wide gate voltage pulses as shown in **Figure 4**. In Figure 4a, by applying a wide voltage pulse (2 seconds), the G_{SD} as a function of the pulse number shows a tendency to saturate in the LTP curve. The LTP curves in Figures 1f-i were measured in the linear conductance modulation region far away from the device conductance reaching the saturation value ($G_{SD\ max}$). Within this linear region, as shown in Figures 4b-d, one can find that the numbers of the metallic grains increased upon the gate voltage pulse cycles. Moreover, the statistical volume percentage of the conductive regions in these three states is about 21%, 67% and 82%, respectively. This indicates that after the device switching (suitable gate voltage/pulse was applied), the LCO layer nearly operating in the *post-percolation* region [11]. It is this *post-percolation* region that enables the device conductance (G_{SD}) to be changed continuously with good linearity as shown in Figures 1f-i. This conductance modulation

mechanism based on the percolation here was unambiguously supported by the 3D tomography c-AFM results, suggesting that the resistive switching mechanism in our LCO NVRT is distinct from the conventional memristors [53-56].

2.4 Dynamics of the electrical field-induced MIT phase separation in the LCO layer

As we demonstrated, the underlining fundamentals of the MIT switching in our NVRT are related to the lithium-ion diffusion [30], while it is unlikely that the suggested nano-battery mechanism [33,34] can guarantee the highly reversible switching processes since the huge volume expansion and solid-state-interphases caused by the lithiation of the SiO_x layer could be detrimental to the device reversibility [57]. Additionally, the formation of a percolation conductive network has been observed only inside the LCO layer according to the 3D nano-tomography conductive AFM measurement, as seen in Figures 3 and 4. Therefore, based on the optical observation, 3D c-AFM mapping and Raman spectra results, we believe that the switching mechanism of our NVRT should be triggered by an electric field-induced MIT phase separation [23,35,58] in the LCO channel layer, which involves short-term lithium-ion rearrangement in the LCO grain (inter-grain) or between the grain (intro-grain), rather than the massive redistribution by crossing the grain boundaries.

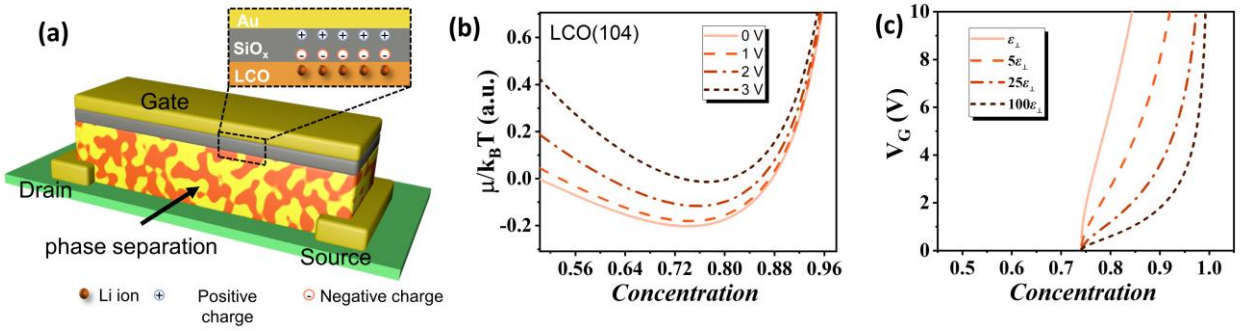

Figure 5. (a) Schematic of LCO phase separating under an applied electrical field. (b) The reduced chemical potential of LCO-(104) as a function of the concentration under different gate voltage. (c) The critical phase separation voltage (V_{set}) of NVRTs with arbitrary LCO crystal orientation (different permittivity values: $\varepsilon_\perp$, $5\varepsilon_\perp$, $25\varepsilon_\perp$, $100\varepsilon_\perp$) as a function of concentration. The simulation parameters can be found in the supplementary information.

The model of the device with a phase separation LCO channel layer is shown in **Figure 5**a. From the thermodynamic point of view, phase separation occurs in a homogenous binary system when the free energy of the system locates at the miscibility gap in which the spinodal and nuclear decomposition could both occur [59]. When a voltage V_G was applied to the gate electrode, the electrostatic potential ϕ was built within the LCO channel layer. The free energy of the LCO in the channel layer can be written as [23,58]

$$F[c,\emptyset] = \int_v \left[G(c,\nabla c) - \frac{1}{2}\varepsilon(c)|\nabla\emptyset|^2 + \rho(c)\emptyset\right] dv \quad (1)$$

Where c is the normalized concentration of lithium-ion inside the channel layer, c=0 and c=1 represent the metallic and insulative LCO phases respectively. The actual concentration of c=0 and c=1 are equal to about $Li_{0.93\text{-}0.97}CoO_2$ and $LiCoO_2$, respectively [18,60,61]. The first term, $G(c,\nabla c)$ function, represents the free energy density of the solid solution, and later two terms describe the total electrostatic energy, in which $\varepsilon(c)$ and $\rho(c)$ are the permittivity and charge carrier density, respectively. The lattice parameter changes between the metallic and insulative phases are less than 2% [62]. Moreover, it is assumed that the redistribution of lithium is a localized process (no filament formation), therefore the changes in mechanical free energy can be neglected here. According to the regular solution model and Cahn-Hilliard approximation [63]

$$G(c,\nabla c) = \frac{\Omega}{v}c(1-c) + \frac{k_B T}{v}[c\ln c + (1-c)\ln(1-c)] + \frac{1}{2}\frac{\kappa}{v}|\nabla c|^2 \quad (2)$$

The first two terms represent the free energy density of the homogeneous solid solution, where Ω is the interaction coefficient between the species. The third term describes the volumetric phase boundary interaction, where κ is the gradient penalty. The initial LCO channel layer in the insulative state has a permittivity ($\varepsilon_i = \varepsilon(1)$) which is up to ten times of the dielectric constant of vacuum ε_0 [64], and is proportional to the lithium vacancy density inside the LCO lattice. At the same time, the permittivity of the metallic phase grows nonlinearly with the extraction of lithium ions and tends to be an infinite value (perfect conductor) after MIT transition ($\varepsilon_m = \varepsilon(0) \gg \varepsilon_i$). This characteristic of permittivity changes during the lithiation and delithiation process in lithium oxide-based phase separation materials can be described by using Clausius-Mossotti relation [23]: $\varepsilon(c) = \varepsilon_i(\frac{3}{c} - 2)$. Therefore, from Equation (1), it can be found that the generic behaviour of the permittivity has significant effects on the system thermodynamic stability under the applied electric field. The total free energy is drastically lowered by the co-existence local area of the metallic LCO phase with higher permittivity $\varepsilon(c)$, especially at low lithium concentration region ($c \rightarrow 0$) where electrostatic energy is large. Namely, a higher electric field can lead to the spontaneous decomposition of the initial homogonous insulative LCO phase. Combining Equations (1) and (2), the diffusion electrochemical potential of lithium ions in the system can be expressed as

$$\mu = \frac{\delta F}{\delta c} = \Omega(1-2c) + k_B T \ln\left(\frac{c}{1-c}\right) + \kappa\nabla^2 c + \frac{3v}{2c^2}\varepsilon_i|\nabla\emptyset|^2 + v\rho'(c)\emptyset \quad (3)$$

Using this, we can now analyse the critical condition of system phase separation mediated resistive switching. Initially, the LCO layer is a single phase homogenous solid solution without phase boundaries, and there is no concentration gradient inside the channel layer ($\kappa\nabla^2 c = 0$), with the charge carrier density staying relatively constant before MIT transition ($v\rho'(c)\emptyset \approx 0$). When a pulse voltage with an amplitude higher than V_{set} is applied to the gate, the generated electric field between the gate and source electrodes may drive the system into the miscibility gap, in which the spinodal decomposition or nucleation and growth occurs from the local lithium deficient areas. The spinodal points of the initial homogenous system under the applied critical voltage V_{set} thus is given by

$$\frac{\partial \mu}{\partial c} = -2\Omega + \frac{k_B T}{c(1-c)} - \frac{3v}{c^3}\varepsilon_i|\nabla\emptyset|^2 = 0 \quad (4)$$

where $\nabla\emptyset = \frac{V_{set}}{L}$, L is the thickness of the LCO channel layer, thus the critical voltage

$$V_{set} = L\sqrt{\frac{c^3}{3v\varepsilon_i}\left[\frac{k_B T}{c(1-c)} - 2\Omega\right]} \quad (5)$$

According to Equation (3), Figure 5b shows the simulation plots of reduced chemical potential ($\frac{\mu}{k_B T}$) of LCO-(104) as a function of concentration (c) of the initial homogenous state ($LiCoO_2$, c=1) under different applied voltages. Here, $\simeq 50\,nm$, $\Omega \simeq 2.6\,k_B T$, $v \simeq 1\,nm^3$, $\varepsilon_{i(104)} \simeq 10\varepsilon_0$ [58, 64, 65]. We can see from Figure 5 that, with the increase of applied V_G value from 0 V to 3 V, the phase separation threshold concentration increases from about 0.74 to 0.79. This implies that the MIT phase separation can occur in the LCO channel layer under a smaller concentration fluctuation with the assistance of a localized lithium redistribution. Similar results of LCO-(003) can be found in Supplementary Figure S5. This is consistent with nanotomography 3D c-AFM results where redistribution of lithium ions in some LCO grains results in the formation of the metallic LCO phase. In this 3D map of physical properties, a homogeneous initial solid solution of lithium ions is driven to phase separate above a critical voltage (V_{set}), leading to the formation of electronically conducting local areas. These conductive areas connect to form a conductive network and increase the conductance between the source and drain electrodes, as sketched in Figure 5a. Meanwhile, the accumulation of opposite polarity carriers (electrons) on the LCO/SiO_x interface can also be

preserved by the dielectric SiO_x layer. This bulk effect, combined with the interfacial effect on the LCO/SiO_x interface where the accumulated Li-ion were trapped in the SiO_x layer, retaining the device at the high conductance state. In contrast, reversing the polarity (applying a positive gate voltage) can drive the backflow of lithium-ions and destroy the phase separation 'conductive network' with a time delay to allow for local rupturing of the percolation conductive network. In summary, the positive/negative gate pulse voltage cycling leads to reversible creation and destruction of the percolation cluster of the metallic phase with hysteresis due to spinodal decomposition of the homogeneous state and nucleation/growth of new phases, meanwhile, the SiO_x serves as a trapping layer to increase the retentivity of the NVRTs.

This model also can be used to explain the microscopic fundamentals of the switching threshold voltage difference in LCO-(104) and LCO-(003) NVRTs. According to Equation (5), the critical phase separation voltage (V_{set}) of four systems with the permittivity value of $\varepsilon_\perp$, $5\varepsilon_\perp$, $25\varepsilon_\perp$, $100\varepsilon_\perp$ are plotted as a function of concentration in Figure 5c. $\varepsilon_\perp$ is the permittivity of LCO crystal along the *c*-axis. With the increase of LCO permittivity along the device's out-of-plane direction, the critical V_G for the LCO layer to reach the phase separation concentration is reduced. In other words, in the system with high permittivity ($100\varepsilon_\perp$), at the same V_G, negligible localized lithium redistribution could trigger the insulative LCO (c=1) to enter the phase separation concentration region. Considering that the in-plane ($\varepsilon_\parallel$) permittivity of LCO (001) crystal plane is higher than its out-of-plane ($\varepsilon_\perp$) value [64], therefore, the channel layer permittivity between gate and source/drain electrode in LCO-(104) NVRT (corresponding to the permittivity parallel to the Co-O octahedra layer in LCO crystal lattice) is higher than the permittivity in LCO-(003) NVRT (corresponding to the permittivity perpendicular to the Co-O octahedra plane in LCO crystal lattice). This difference is even magnified at low-frequency region as discussed in SI, section 8. As a result, the smaller V_G value was observed for driving the switching of LCO-(104) NVRT as shown in Figure 1f.

2.5 Challenges and opportunities of Li-ion based three-terminal synaptic transistor

After more than 10 years of effort put into the development of lithium-ion based memristor by the worldwide scientific communities [5,22-23,28,33], significant advances have been achieved, including optimized device architecture [32], switching performance [33], as well as fundamental understanding [23, 35] of the resistive switching phenomena. Yet, some question remains elusive.

First of all, the role of oxygen vacancy on the channel layer's electrical conductivity is rarely discussed in Li-ion based memristors. Oxygen vacancy plays a significant role in many metal oxides-based memristors, especially the correlated oxides with MIT. For example, Jian et al. demonstrated the synaptic action in three-terminal correlated oxide ($SmNiO_3$) devices [66]. Interestingly, they found that the increase of oxygen vacancy leads to an increase in resistivity in the metallic state of $SmNiO_3$, while in the insulating regime, introducing oxygen vacancies modulates the resistivity of $SmNiO_3$ channel layer non-monotonously. But in our case, the dependence of the conductance of LCO channel layer on lithium concentration is relatively monotonous in both insulator and metallic states, and the effect of oxygen vacancy can be negated in this lithium-ion migration induced MIT. To be more specific, in the electrical field-polarized LCO thin film, the main charge carriers are lithium-ions, and the migrations of oxygen vacancies are negligible compared to the lithium-ions [45,67-68]. The activation energy of lithium-ion diffusion in side LCO is at the order of magnitude of ~10^{-2}-10^{-1} eV [69-70], which is one order of magnitude smaller than that of oxygen vacancies. Additionally, the mobility of lithium ions inside the LCO is higher than the mobility of oxygen vacancies [67]. Such behaviour is explained as the oxygen ions are covalently bound with cobalt ions and form the stable framework of edge-sharing CoO_6 octahedra layers [71], which guarantees the crystal structure integrity during the reversible lithium-ion intercalation/deintercalation, enabling LCO to be the most widely used and electrochemically stable lithium-ion battery cathode materials [72]. Therefore, given the high mobility and low diffusion energy barrier of lithium-ions in LCO, we believe that the applied electrical fields in our device mainly drive the lithium migration and redistribution inside the LCO thin film. However, one should also notice that, at highly de-lithiated states, the oxygen vacancies migration/formation energy barrier can be significantly reduced, even causing oxygen evolution [73-75]. These oxygen vacancy migration-induced Co-O layer rearrangements can cause irreversible phase transitions with the migration of oxygen vacancies being detrimental to the LCO crystal structure integrity. Nevertheless, such conditions are avoided in our memristor devices where the operation envelope does not reach such values.

Secondly, being a type of solid-state ionic-based memristor, the operation speed of LCO NVRTs could be a bottleneck for their application for high-frequency neuromorphic computation. Although the diffusion kinetics of lithium in solid is much better compared with other cations (such as Ag^+ and Cu^+ in electrochemical metallization memories), the migrations of Lithium-ions in lithium transition metal oxide often is accompanied by the phase transition with non-negligible energy barriers [76-78]. Recent reports on metal oxide-based memristors, such as TiO_2 [79], Ta_2O_5 [80], Nb_2O_5 [81] etc., show sub-microsecond/nanosecond operation speed with neuromorphic functionality, which is better

than the common electrochemical random-access memories that are limited by the slow ion kinetics [82] on the order of milli-second write-read delays [22] and/or requiring long read pulses to ensure accurate readout of a non-volatile change [83-84]. As discussed above, lithium-ion based NVRTs' operation speed is intrinsically limited by the diffusion of Li^+ in the LCO, but it can be tackled by shortening the characteristic diffusion length, represented by lithium-ion redistribution. This means that, in our case, lithium-ion does not have to travel back and forth between two electrodes like a "rocking chair" secondary battery, but it can redistribute between the percolation units inside the resistive layer switches, switching between two slightly non-stoichiometric states (metallic $Li_{0.95-1}CoO_2$ and insulative $Li_{0.5-0.95}CoO_2$) through inter- and intra-grain redistribution. Previous studies suggested that improving the crystallinity of LCO material will increase the diffusivity by a factor of 10^3 and extend the operability to the μs regime [32,85]. Therefore, we believe that reducing the characteristic diffusion length inside LCO, such as reducing the grain size or increasing the dislocation density, can both reduce the Li^+ redistribution/diffusion time, resulting in a further enhancement of the operation speed. This assumption has been validated by our preliminary results measured on the device with a shorter channel layer distance of 10 μm. The scaled-down device has shown a linear LTP behaviour under the stimulation plus with a width of 1 μs (SI, Figure S8d). Similar strategies were adopted by Onen et al. to achieve a nanosecond protonic programmable memristor [86].

However, it is worth noticing that when compared with other types of memristor, the key advantages of our NVRT memristor rely on the small energy consumption, absence of electroforming, process tunability, and in particular, its high robustness. LCO-based memristor devices were found to maintain conductance levels and hold the state of charge for several weeks after "write" operations [33] as additional energy is needed to drive the lithium redistribution inside the percolation network of LCO after the MIT phase separation. The high electrical resistivity of SiO_x layer ensures that the resistance switching is non-volatile and shows a high level of robustness [30,33]. In some cases, Li out-diffusion can contribute to self-discharge, a typical slow degradation process (>1–2% lithium backflow per month) during the storage of lithium-ion batteries. But neural applications often target training periods of less than one week after which the weight information can be read and stored digitally if needed [32]. Therefore, we believe that our LCO NVRTs with good robustness can play a significant role in the further development of neural applications.

3. Conclusions

In summary, we fabricated the three-terminal transistor with memristive behavior. In this transistor, the key parameters, including the retention capability, thermal stability and switching voltage, can be effectively adjusted by tuning the crystal orientation of the LCO channel layers between the source and gate electrodes. The low switching voltage and high linearity were found in the NVRT device with the LCO (104) crystal planes perpendicular to the 'writing' electrical field direction (parallel to the device 'reading' electrical field direction). Significantly, the highly reversible trapping/releasing effects of the SiO_x gate dielectric layer, rather than the interfacial solid-electrochemical reaction with lithium-ions, guarantee the stability of long-term resistive switching cycles and low energy required for the operation of such a neuromorphic device. The energy consumption per "write" (E_{write}) in our LCO NVRTs is estimated at the order of magnitude of pico-joule which is comparable with the recently reported values in three-terminal transistor [87], and it can be further reduced by scaling down the device size (see energy consumption analysis in SI, section 9). Apart from the interfacial SiO_x trapping effect, the electric field-induced phase separation, as well as the percolation of metallic LCO phase within the channel layer, were observed in the three-terminal NVRT by *in situ* Raman and 3D nano-tomography conductive AFM. The phase separation dynamic was numerically studied by nonequilibrium thermodynamics analysis, in which we found that the dielectric permittivity of the LCO channel layer plays a key role in determining the electrostatic energy term that can significantly affect the phase separation threshold concentration. This phase separation mechanism of the LCO switching layer was suggested as the synergy effect of the SiO_x interfacial trapping mechanism, resulting in the robust resistive switching behavior of the LCO NVRTs. With further scaling down the devices, we believe our LCO synaptic transistor based on the percolation theory with decent linearity and tunable lithium ionic migration dynamic will be is a promising NVRT that overcomes the shortcomings in the conventional ECMs and VCMs.

4. Experimental Section

4.1 Thin-film deposition and device fabrication

Polycrystalline LCO was deposited on silicon wafer substrates by using RF magnetron sputtering. The substrates used were highly doped p-type Si (100) with and without the amorphous silicon oxide layer. The epitaxial LCO films with (003) and (104) preferred orientations were grown on the (111) and (100) crystal planes of $SrTiO_3$ (STO) single-crystal substrates, respectively. All LCO samples used in this study were deposited by using magnetron sputtering (Flow rate: 25 sccm O_2 + 25 sccm Argon; Areal power density: 30 W cm^{-2}; Deposition pressure: 0.5 Pa). The three-terminal nonvolatile redox transistors (NVRT) were fabricated using the bottom-up synthesis method. Two parallel Au electrodes were patterned on the substrate before the LCO channel layer was deposited, serving as

source and drain electrodes. After the epitaxial LCO films were deposited on STO substrates, a ~80 nm amorphous SiO_x was deposited by reactive sputtering to cover the whole LCO channel area. Lastly, a gold top electrode was patterned on top of the SiO_x dielectric layer as the gate electrode. (The device section SEM can be found in Figure S18a. The initial conductivity between the drain and source electrodes was determined by scanning the *I-V* curves between -1 V to 1 V, as seen in Figure S18b. The pulse width for the measurements of the synaptic plasticity of NVRTs was optimized by applying a set pulse of -3V with different pulse widths, as seen in Figure S19a, b. To avoid the over-extraction of lithium ions, the device was measured at the linear region rather than the non-linear region and saturation region as shown in Figure S19c.

4.2 Characterization

The surface morphology of thin films was captured by scanning electron microscopy (Hitachi SU-8010). Resistive state characterizations and modifications of the as-prepared films and NVRT devices were performed by conductive AFM (c-AFM), and the surface potential was measured by Kelvin probe force microscopy (Bruker Dimension Icon). To check the reversibility of the local resistive switching effects, a c-AFM image was recorded after tip 'writing' using a concentric square method under the bias voltages of ±4 V. For the *I-V* measurements, the bias was applied to the bottom Si substrate, the tip was grounded. The platinum silicide tip (k~3 N m^{-1}, f_0~75 kHz) was used for c-AFM measurements. The Boron-doped polycrystalline diamond tip (All-in-one-DD, cantilever D, k~100 N m^{-1}, f_0~450 kHz) was used in the 3D nano-tomography c-AFM measurements. The scratching force applied to the LCO is about 10 μN, corresponding to about 1 nm penetration depth per frame. The tip-milling depth was determined by measuring the step height in scratched surface topography, as seen in Supplementary Figure S20. The obtained 3D c-AFM current map was stacked using ImageJ software. All AFM measurements were performed in a glove box filled with Ar with <1ppm O_2 and H_2O concentration. The electrical and memristive switching properties were measured using the Keithley 4200 semiconductor parameter analyzer and an arbitrary function generator (AFG31000, Tektronix), respectively. X-ray photoelectron spectroscopy (ESCALAB 250 Xi, USA) was used for the detection of surface elemental composition. The permittivity of LCO-(003) and LCO-(104) thin films are measured by impedance spectroscopy, using an AC excitation signal with an amplitude of 50 mV, in the frequency region between 10^{-1}-10^7 Hz. As shown in Figure S17a, the Nb-doped conductive STO bottom electrode [40] and 100-nm-thick Au top electrode are used as two metallic blocking electrodes, forming a metal-insulator-metal stack structure. Raman spectroscopy (HORIBA Jobin Yvon Evolution, 532 nm excitation) was employed to determine the LCO phase transition during the switching. Optical video of NVRT during a switching was recorded

using a stereoscopic microscope (Motic SMZ-168). The cross-section of the LCO/SiO_x/Si stack was prepared by focusing ion beam cutting (ZEISS CROSSBEAM 550). The nanostructure of the cross-section structure was examined by TEM (FEI Talos F200).

Credit authorship contribution statement

Weijian Zhang: Investigation, Formal analysiss, Writing – original draft, Writing - review & editing, Validation. **Yue Chen:** Formal analysiss, Writing – original draft, Writing - review & editing, Validation, supervision. **Chenjie Xu, Chun Lin, Jianming Tao, Yingbin Lin, Jiaxin Li:** Characterization. **Oleg V. Kolosov, Zhigao Huang:** Conceptualization, Supervision, Project administration, Funding acquisition, Writing - review & editing.

Conflict of Interest

The authors declare no conflict of interest.

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