Efficient modular multilevel converter based on active-forced-commutated hybrid packed u-cells for HV networks

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Abstract

High-voltage DC (HVDC) converter topologies have been more desirable in the off-shore wind energy applications to increase the efficiency and reduce the losses. In this context, the paper presents a modified structure for modular multilevel voltage source converter (VSC) topology where the conduction and switching losses can be significantly reduced. As the conduction losses of the semiconductor devices affect the total efficiency of such systems, replacing part of the Insulated Gate Bipolar Transistor (IGBT) devices with thyristors in the conduction path of the proposed topology can reduce the total losses in the normal operation. Thus, both IGBTs and thyristors are implemented in a hybrid configuration. In this configuration, the IGBT devices are responsible for voltage/current transitions between the positive and negative parts of the waveforms while the thyristor devices are responsible for conducting the currents in the other constant polarity regions. MATLAB simulations and scaled-down experiments show that the modified structure can reduce the total losses of the HVDC converter significantly.

1 Introduction

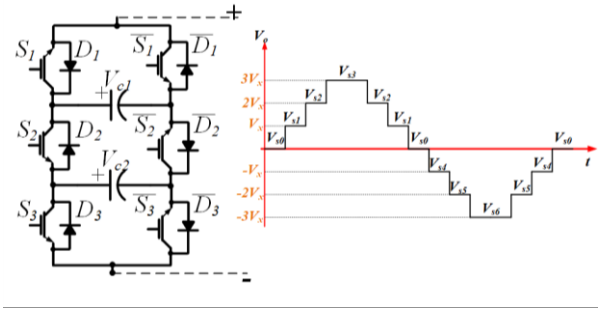
Due to the recent significant development of the renewable energy sources, such as wind energy systems, High-voltage DC (HVDC) converter topologies become very vital [1,2]. This comes from the fact that HVDC converters, operating with Insulated Gate Bipolar Transistor (IGBT) switches, have several merits such as: (i) the ability to generate output or intermediate voltages and currents with low harmonic content, (ii) the possibility of decoupled active and reactive power control, (iii) system's modularity and (iv) scalability and redundancy [3]–[5]. When the MMC is coupled with a low or medium frequency transformer, the *dv/dt* applied on the transformers' windings can be reduced significantly [6].

However, because of their very low power losses, thyristor-based Line Commutated Converters (LCC) are still dominant in high-voltage/high-power applications. To give an indication for that, the typical forward voltage of the 4.4kV/1.2kA Infineon FZ1200R45KL3_B5 IGBT is 3V while the on-state voltage of the 4.3kV/1.8kA T1800N42TOF PR thyristor from the same manufacturer is the half (1.5V).

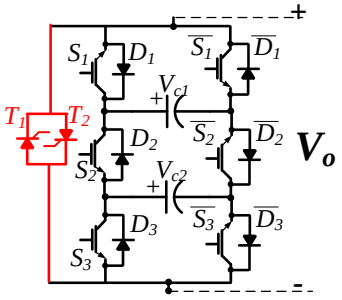
In this context, the total conducting and switching losses of a modular multilevel converter (MMC) provide an important guide for its appropriateness in high-voltage (HV) applications. Owing to their modularity and established operation, MMC structures based on half-bridge (HB) modules are used extensively in industrial HV transmission systems. However, the main drawback of the HB-MMC is its incapability for blocking dc sides faults and hence the vulnerable parallel diodes are exposed to destruction. Many researches have been carried out to improve the operation of the MMCs in terms of efficiency, reliability and fault-ride-through in case of dc faults. A promising concept, namely Quasi-two-level (Q2L), has been discussed in [6] where the proposed converter uses HB cells to generate square voltages with controllable slopes to mimic the conventional two-level Voltage Source Converters (VSC). In this way, the capacitance required in the HB cells will be significantly reduced. The same authors have proposed Transition Arm Converter (TAC) concept where the lower arm of the MMC consists of series IGBT switches. In this way, the upper arm cells are conducting currents during the transition periods of the square wave voltage between the flat top and bottom while the lower arm is responsible for generating the plateaus of the square wave voltages. In this context, Hybrid devices of IGBTs and thyristors can be used to increase the efficiency of the MMC structures. Accordingly, the power losses can be driven down to the ranges of Line Commutated Converter (LCC) topologies while achieving the advantage of MMC topologies such as black-start, bidirectional power flow, capability for weak grid connection, blocking dc faults, etc. An impressive symmetrical bipolar cell, namely Packed U Cell (PUC) has been proposed in the literature, see Fig. 1a [8]. With two semiconductor devices in the conduction path, this cell can generate five voltage levels (3V, 2V, V, 0, -V, -2V, -3V). If this cell is modified with thyristor devices as shown in Fig 1b, it can be used in the proposed MMC operating as a TAC, see Fig 1c. The proposed topology has several advantages such as: (i) reduced power losses, (ii) modularity, (iii) ability for operating with reduced dc-link voltages, and (iv) bidirectional power flow. The proposed structure is suitable for both DC/DC and DC/AC applications.

This paper will be organized in six sections. Section 2 will discuss the basic operation of the proposed topology.

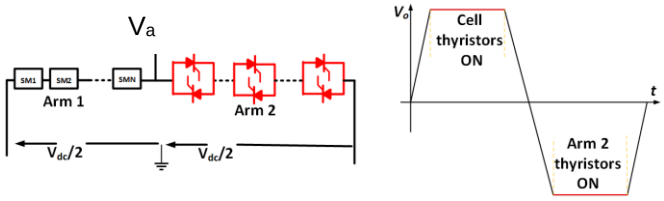
The description and MATLAB simulations of the three-phase dc-ac mode will be presented in Section 4. The dc-dc operation of the system will be shown in Section 4. Section 5 shows the experimental results of the scaled-down prototype to validate the basic principle of the system while the conclusion will be summarized in Section 6.



(a) 7-level Packed U cell



(b) Modified 7-level cell as submodule (SM)



(c) One leg of the proposed hybrid MMC and its output voltage

Fig. 1. Proposed hybrid MMC concept

2 Operation principle

As stated earlier, the PUC can generate seven voltage levels. This section explains the operation principle for the proposed MMC with one cell per arm per phase. In this case, the switching states of the cell are listed in Table 1.

State	T_1	T_2	S_1	S_2	S_3	V_o
St1	OFF	OFF	1	0	0	V_{dc}/N
St2	OFF	OFF	1	0	1	$2V_{dc}/3N$
St3	OFF	OFF	1	1	0	$V_{dc}/3N$
St4	ON	ON	0	0	0	0
St5	OFF	OFF	0	0	1	$-V_{dc}/3N$
St6	OFF	OFF	0	1	0	$-2V_{dc}/3N$
St7	OFF	OFF	0	1	1	$-V_{dc}/N$

Table 1: Switching states.

Fig. 2 shows the simplified operation when only one cell is inserter in Arm 1 of each phase (N=1). During the transition

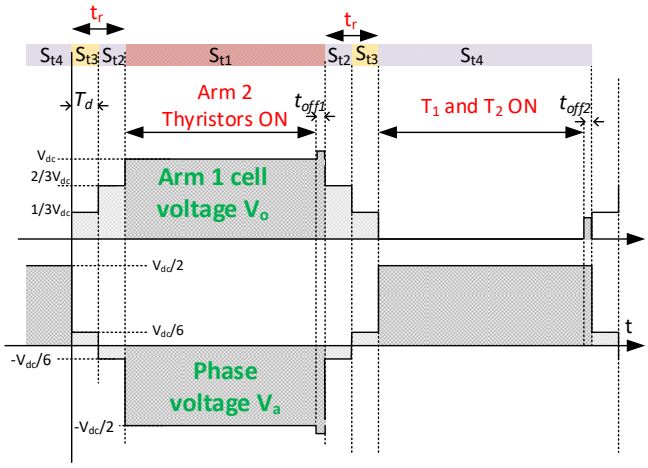


Fig. 2. Operation of the proposed converter

period (t_r), the PUC in Arm 1 is switching its states in order to change its terminal voltage from zero to V_{dc} as shown in Table 1. Meanwhile, the phase voltage (V_a) is switching from its positive half cycle value ($V_{an} = V_{dc}/2$) to the negative half cycle ($V_{an} = -V_{dc}/2$). In this way, the IGBTs of each cell are switching and conducting in very short duration which is the transition period while the thyristor are responsible for conducting the currents in all other durations. Because the cells are able to generate voltage with different polarities, the negative voltages are used to turn of the cell thyristors (T_1 and T_2). In the normal operation where Arm 1 has numerous cells, redundant cells N_R are responsible to generate additional voltage to Arm 1 in order to turn off the thyristors of Arm 1 when required. These redundant cells can be of PUC type or of the conventional HB cells. Their role will be to provide an additional voltage during a short duration (t_{off1}) to ensure turning off the thyristors of Arm 2 if the current is passing through Arm 2 thyristors from up to down. If the current is passing in the opposite direction, one or some of Arm 1 cells will produce negative voltage on its terminals in order to turn Arm 2 thyristors off. This will be repeated to turn off Arm 1 cell thyristors according to the current direction in the cells. Because the thyristors are ON for relatively long time durations, the cell capacitors of the PUC can be charged using the redundant states of the cells by the knowledge of the current polarity and capacitors voltage values [9].

3 DC/AC converter

The trapezoidal voltage modulation concept of the dc/dc converter, shown in Fig. 2, has been proposed in [6] as an efficient alternative for HVDC systems. As stated earlier, the converter size can be significantly reduced according to the smaller capacitances required. Although the trapezoidal waveform has higher harmonic content, this can be eliminated by using Selective Harmonic Elimination (SHE) modulation technique and/or the installation of line filters to meet the grid standards. In this system, the arm inductances are only needed when the lower thyristor (Arm 2) arm is ON. Thus, no or very small arm inductances can be used in the said trapezoidal mode of operation and therefore the converter size can be

reduced dramatically. The three-phase converter based on the modified PUC cells, mentioned in Fig. 1b, is shown in Fig. 3. Arm 1, 3 and 5 will be referred to as "*transition*" arms while Arm 2, 4, and 6 will be referred to as "*bi-state*" arms.

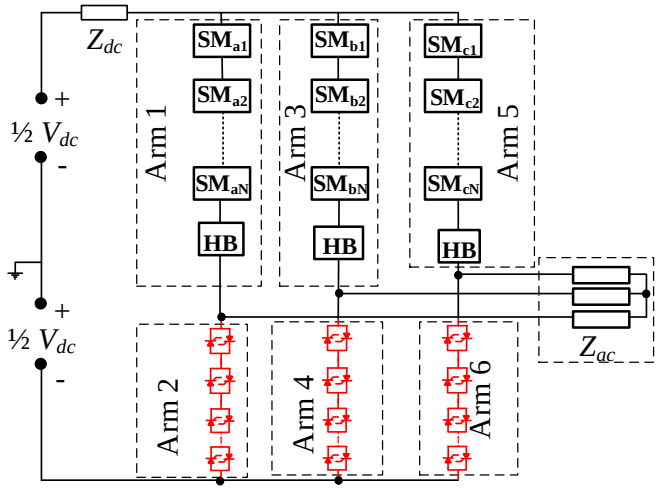


Fig. 3. Proposed converter in DC/AC mode

A simulation model is built with Matlab/Simulink® to study the operation of the DC/AC three-phase converter shown in Fig. 3 with 12 levels and using the parameters listed in Table 2.

DC side voltage V_{dc}	±25 kV
DC impedance Z_{dc}	R_{dc} = 0.25 Ω and L_{dc} = 0.5mH
Dwell time T_d	200 µs
Fundamental frequency f	50 Hz
Cell capacitance	30 µF
Arm impedance Z_{arm}	R_{arm} = 0.2 Ω and L_{arm} =10µH
Three-phase load	R_L = 50 Ω and L_L = 2mH

Table 2: Parameters of the proposed DC/AC converter

The converter is supplied from a 50kV dc source and modulated to generate trapezoidal 3-phase voltage waveforms across the three-phase inductive load. As stated earlier, a very small arm inductance is required to limit the arm currents during the transition periods between the bi-state and transition arms. It should be noted that series cells can be grouped together with the same switching signals in order to ease the gate driving process. Increasing the dwell time (T_d) of the trapezoidal waveforms will lead to lower *dv/dt* but on the expenses of higher cell capacitances. Fig. 4 shows the simulation results for the abovementioned system. The arm currents are shown in Fig. 4a and 4b. As shown in Fig. 4c and 4d, the upper capacitors voltages are set to V_{dc}/N while the lower capacitors voltages are set to $V_{dc}/3N$. The ripple voltages are within the range of 1% using the conventional sorting technique where the cells are ordered according to their voltages and to the arm current direction. The upper and lower arms voltages are shown in Fig.4e and 4f. Finally, the output phase voltages and load currents are shown in Fig. 4g and 4h.

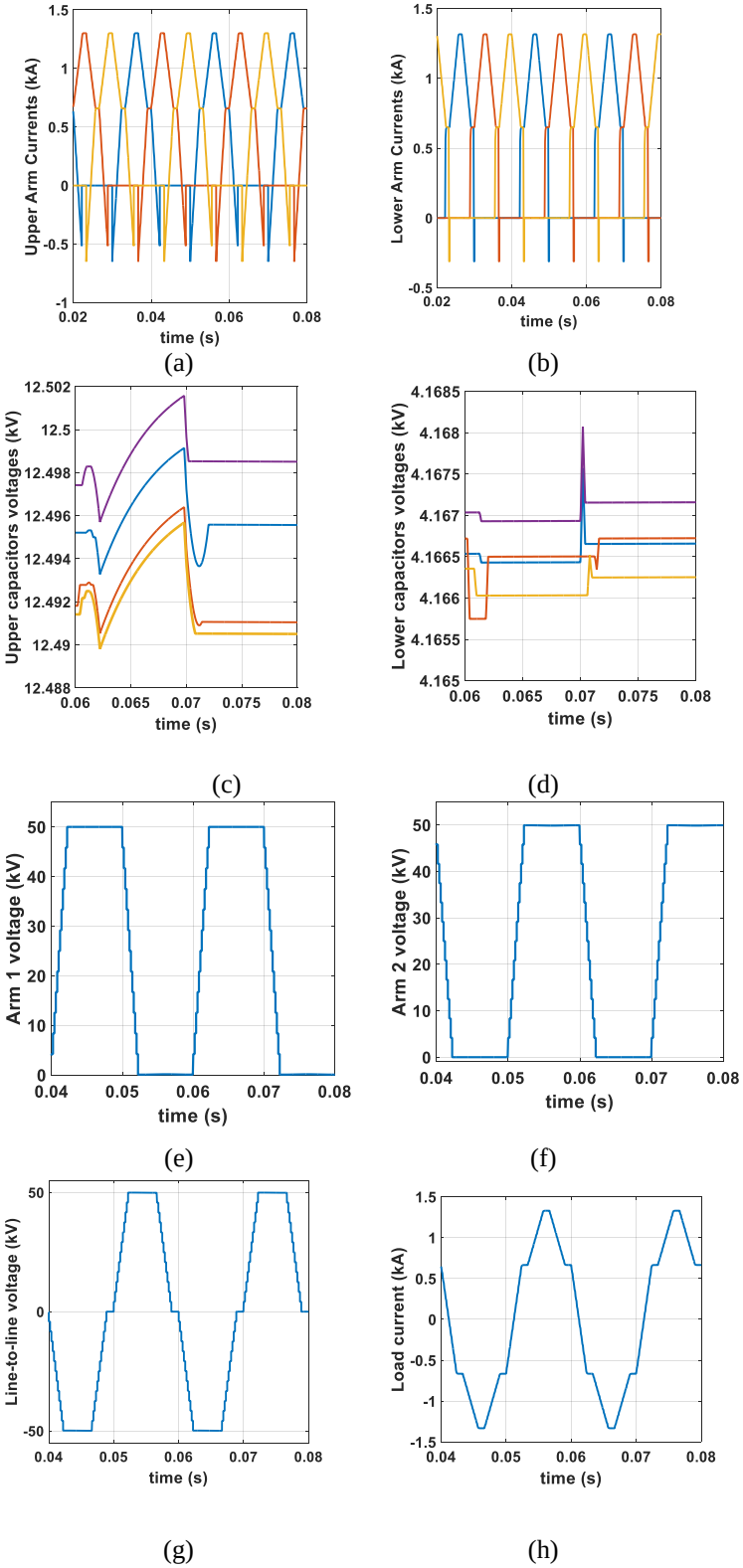


Fig. 4. Simulation results of DC/AC converter: (a) Upper arms currents, (b) lower arms currents, (c) upper capacitors voltages of Arm 1, (d) lower capacitors voltages of Arm 1, (e) Arm 1 voltage, (f) Arm 2 voltage, (g) Line-to-line voltage (V_{ab}), and phase a load current

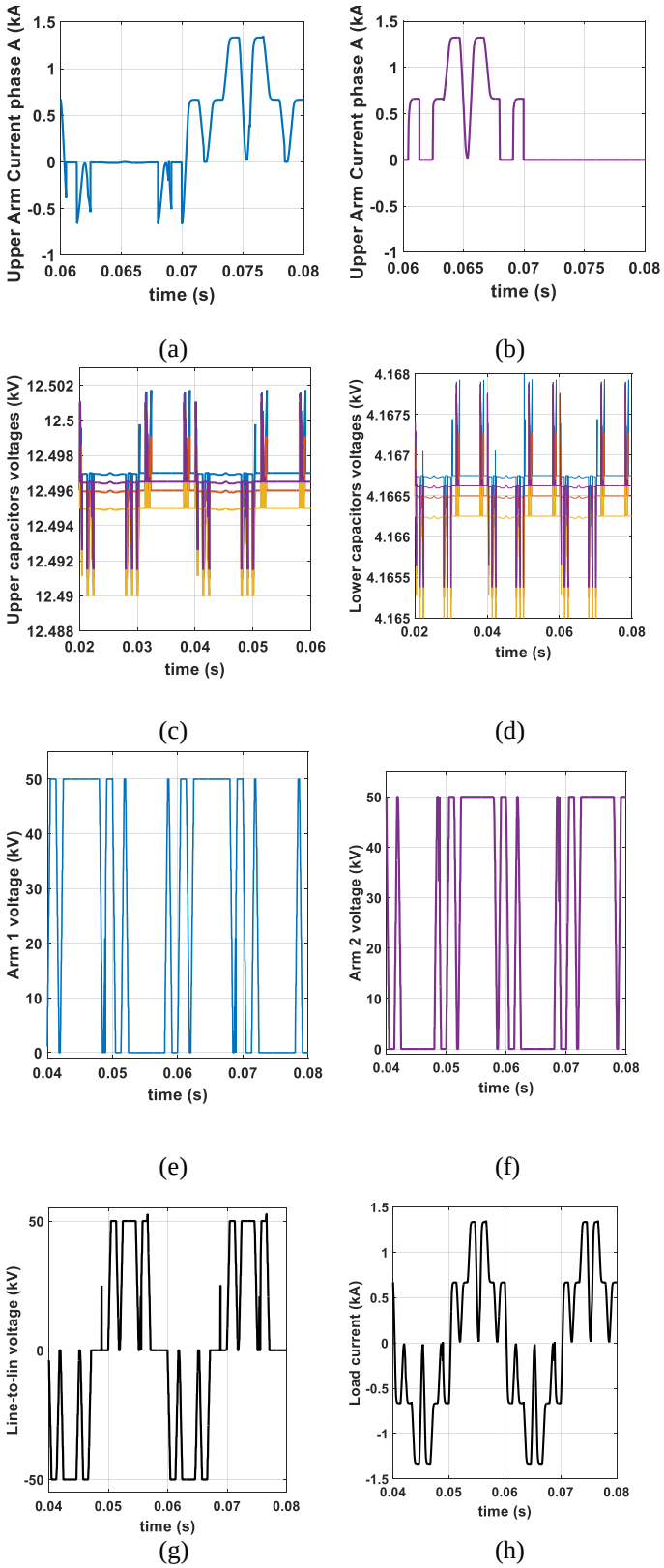


Fig. 5. Simulation results of DC/AC converter with SHE modulation: (a) Upper arms currents, (b) lower arms currents, (c) upper capacitors voltages of Arm 1, (d) lower capacitors voltages of Arm 1, (e) Arm 1 voltage, (f) Arm 2 voltage, (g) Line-to-line voltage (V_{ab}), and (h) phase a load current

To reduce the harmonic content of the output voltages and currents, SHE modulation technique can be used. To give an example for that, the results in Fig. 5 show the operation of the DC/AC converter when operating using the SHE modulation to eliminate the fifth harmonic in the output current. Fig. 6 shows the THD of the output current with and without the SHE.

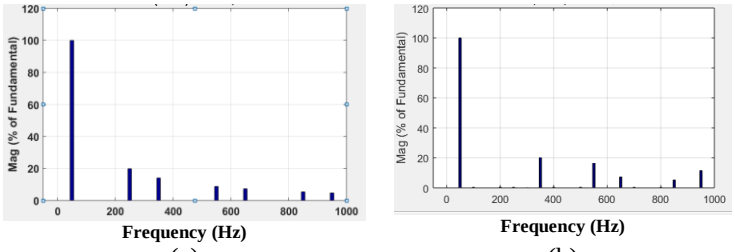


Fig. 6. THD of output current: (a) without SHE and (b) with SHE for fifth harmonic (250 Hz).

4 DC/DC operation

The proposed topology is more suitable to operate in front-to-front dc-dc transformer and can act as a dual active bridge (DAB) converter [10]. Generally, there are two dc/ac and ac/dc converters connected together via three-phase two-winding transformer at the line frequency as shown in Fig. 7. However, increasing this frequency will lead to a significant reduction in the transformer size. In addition using the trapezoidal waveforms as described in Fig. 1 and Fig. 2 will reduce the *dv/dt* stresses on the cells and the interfacing transformer and will lead to another significant reduction in the size of submodule cells and therefore the total size of the DAB. Using thyristors in the PUC cells as well as the lower arm is expected to reduce the conduction losses and increase the total efficiency significantly.

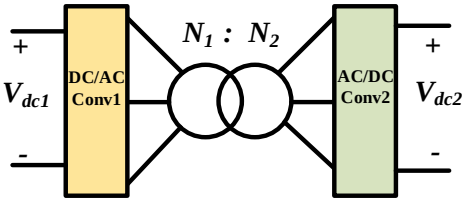


Fig. 7. Basic structure of DAB converter

In addition to the DAB operation in Fig. 7, the proposed topology can be used in other HVDC structures such as HVDC auto-transformers. The proposed topology is capable of providing black start following dc grid faults. Because the proposed cells are bidirectional, it is possible to generate the required voltage to block the dc side faults. In addition, the ac-link transformer should be able to prevent fault propagating between the primary and secondary sides. A Simulink/MATLAB model is built for the system in Fig. 7 using the parameters in Table 3.

Fig. 8 shows the results of the DC/AC converter (Conv 1) while Fig. 9 shows the results for the AC/DC converter (Conv 2).

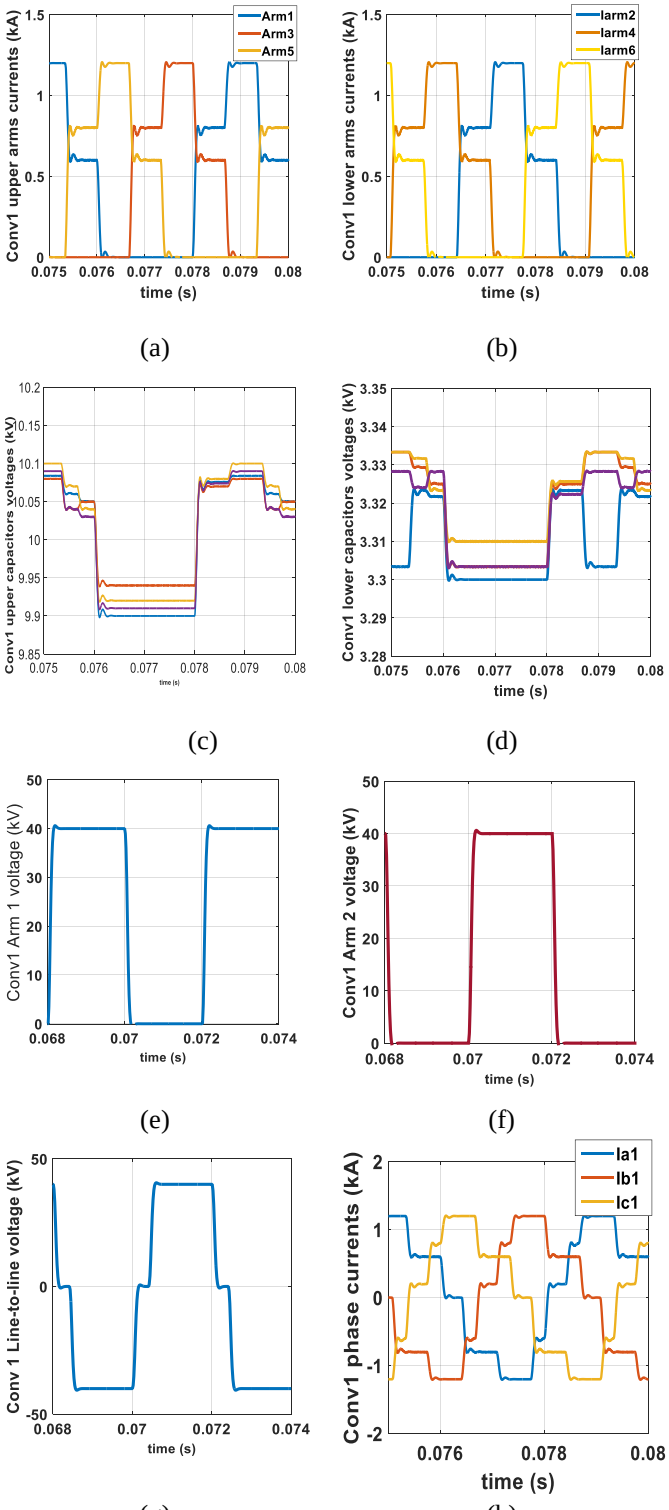


Fig. 8. Simulation results of DAB system (Conv 1): (a) Upper arms currents, (b) lower arms currents, (c) upper capacitors voltages of Arm 1, (d) lower capacitors voltages of Arm 1, (e) Arm 1 voltage, (f) Arm 2 voltage, (g) Line-to-line voltage (V_{ab}), and phase a load current

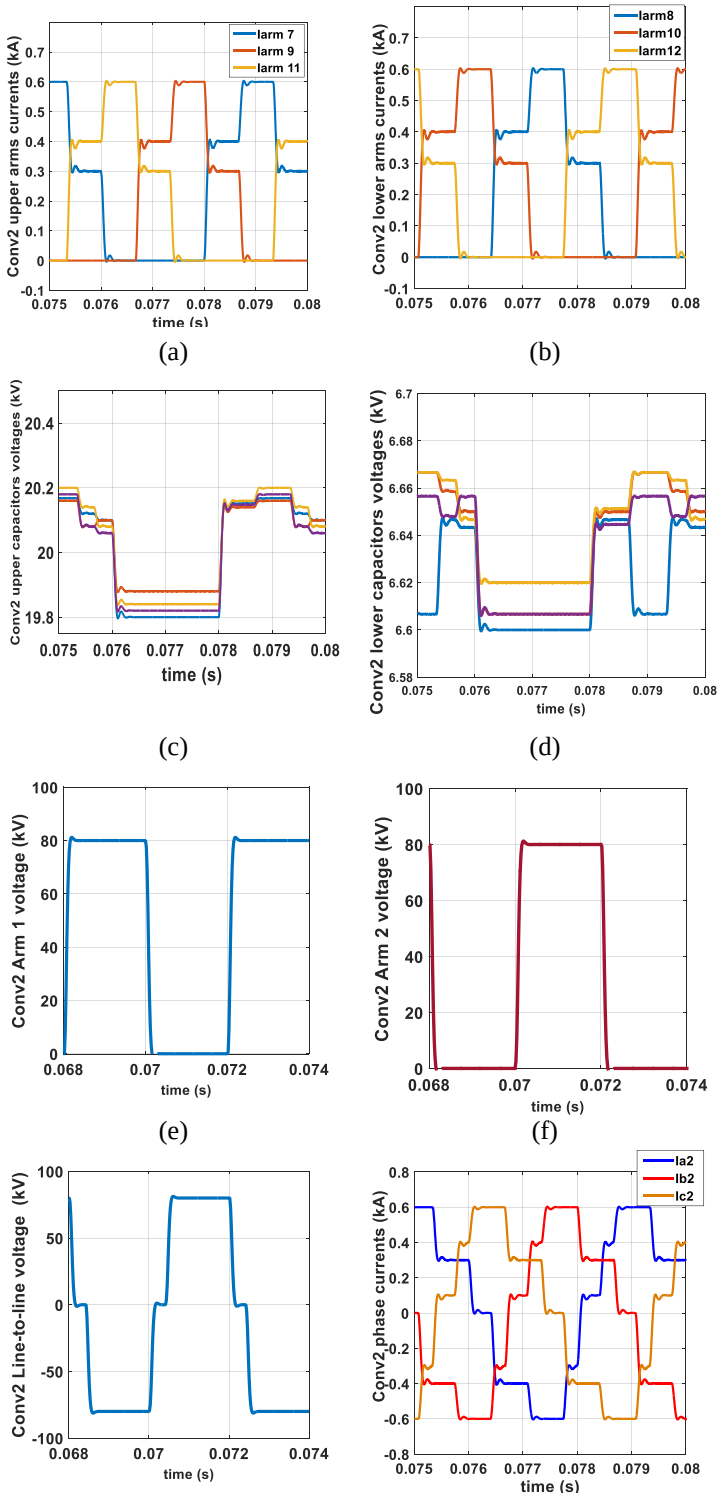


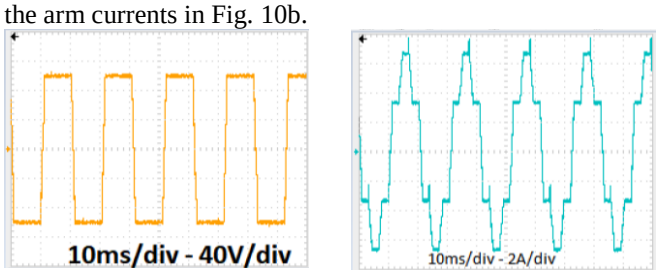
Fig. 9. Simulation results of DAB system (Conv 2): (a) Upper arms currents, (b) lower arms currents, (c) upper capacitors voltages of Arm 1, (d) lower capacitors voltages of Arm 1, (e) Arm 1 voltage, (f) Arm 2 voltage, (g) Line-to-line voltage (V_{ab}), and phase a load current

Side 1 dc voltage V_{dc1}	±20 kV
Side 2 dc voltage V_{dc2}	±40 kV
DC impedance Z_{dc}	R_{dc} = 0.25 Ω and L_{dc} = 0.5mH
Dwell time T_d	10 µs
Fundamental frequency f	250 Hz
Cell capacitance	30 µF
Arm impedance Z_{arm}	R_{arm} = 0.2 Ω and L_{arm} =10µH
Number of PUC cells per arm N	4

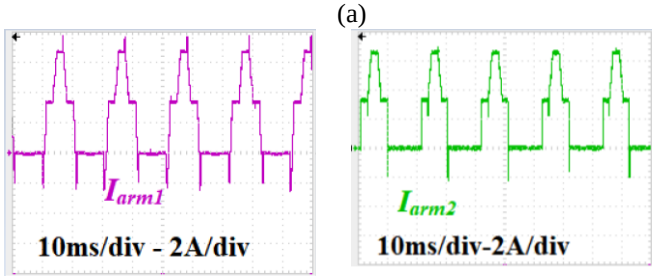
Table 3: Parameters of the proposed DAB system

5 Experimental results

A scaled down DC/AC prototype with two cells in each arm has been built and controlled with TMS32028335 DSP in order to show the basic operation of the proposed topology. The dc side voltage is set to 100V while the load resistance is 22Ω. Fig. 10a shows the phase load voltage and current while the arm currents in Fig. 10b.



(a)



(b)

Fig. 10. Experimental results of DC/AC converter: (a) phase load voltage and current and (b) upper and lower arm currents

6 Conclusion

A modified seven-level Packed-U-cell has been used in a hybrid dc/ac topology for HVDC application. The proposed topology can be extended to DAB front-to-front and dc-dc autotransformer configurations. The cells of the upper arm have been modified by adding back-to-back thyristors while the lower arms have been replaced with series back-to-back thyristors to enable generating trapezoidal output voltages at its terminals. Consequently, the conduction losses of the converter can be reduced to half the value of its conventional counter parts. Additionally, the proposed converter is expected to have smaller cell capacitances as well as arm inductances and hence, smaller overall size. The proposed converter has the advantages of low power dissipation experienced in LCC with the same advantages of voltage sourced converters such as bidirectional power flow, black-start operation after dc link fault, and dc fault blocking.

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