Current-Source Modular Medium-Voltage Grid-Connected System with High-Frequency Isolation for Photovoltaic Applications

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***Abstract*—Large-scale grid-connected photovoltaic energy generation systems are progressing remarkably benefiting from the latest developments in solid-state semiconductors technology. In such systems, the photovoltaic arrays can be connected directly to the medium-voltage grid without employing a bulky line-frequency transformer to step up the voltage. Nano-crystalline cores with a small size and a high permeability operating at medium or high frequency can be installed in the power conversion stage. Hence, the necessary isolation as well as voltage boosting features can be provided. However, only a few power converters allow this type of isolation. This paper proposes a new modular converter structure suitable for medium-voltage grid connected systems with high-frequency isolation. The output voltages of the series-connected modules are added in order to provide the necessary voltage boosting. Four different power converter topologies with small input capacitors can be used as submodules for the presented medium-voltage configuration having different advantages and drawbacks. These different topologies are analysed in terms of power losses, footprint and functionality. To validate the mathematical analysis and the computer simulations, a scaled-down 5 kVA three-phase, 1 kV prototype is built and tested with four modules for each phase.**

***Index Terms*-- Modular medium-voltage converter, photovoltaic power plants, renewable energy systems.**

I. Introduction

RECENTLY, there is a remarkable increase in the installed capacity of renewable energy power plants, especially photovoltaic systems. The cumulative capacity of installed PV system worldwide is estimated to be more than 500 GW by the end of 2018 [1]. India and China have several PV plants with power capacity of more than 50 MW. Other projects generating electrical power of more than 300 MW are already in service. However, these extremely large-scale power plants have to be built on large areas and therefore they are convenient in rural areas. The total installed capacity in Europe has exceeded 103 GW in 2016 [1]. In the near future, it is expected that a huge number of PV power plants will be installed in the Middle East and North Africa (MENA) region which has excellent conditions for PV power generation investments. In Europe, new PV power plants of capacity more than 8 GW are installed in 2015 [2]. Accordingly, increasing the efficiency and improving the reliability of such PV plants becomes more important. In total, PV power shares around 5% of the total European power demand [2].

To interface these PV systems to the medium/high-voltage grids, a large step-up transformer operating at the ac line-frequency is installed to match the voltage levels, which are normally between 6.6kV to 33kV. For example, the 12 kV, 2 MVA vacuum cast coil dry-type Tier 1 transformer from ABB weights 5 tons and has a volume of 11 m^3. This adds to the total cost, weight and size, let alone the required maintenance of the system especially when it is installed in rural distant areas.

The latest developments in semi-conductor power switches technology led to the emergence of cascaded modular multi-level converter (MMC) with large number of submodules (SMs) as key players in several applications [3]–[5]. Such systems have the advantages of modularity and scalability where additional modules can be easily installed if it is required to increase the voltage/power levels in the future. Also, it is easy to replace a faulted module if it has been damaged for any unplanned reason and hence the reliability of the system is increased. However, MMC topologies require balancing techniques for the different SMs voltages or balanced multiple dc supplies have to be used. In addition, the conventional half-bridge MMC modules are not able to provide fault-ride-through capability for faults at the input side, exposing the vulnerable diodes to severe and destructive currents [6]. In [7], an MMC topology with H-bridge modules is used with multiple PV arrays acting as isolated input dc sources proposing important features for medium-voltage systems. As a drawback, the leakage currents flowing through the stray capacitance between the PV neutral point and the ground form a major risk for the system safety, operation and lifetime [8]. For this reason, dc/dc modular structures based on small-size High Frequency (HF) isolating transformers are proposed to avoid risks and improve the system safety conditions. Increasing the switching frequency of the converter leads to a significant decrease in the isolating transformers sizes, weights, and volumes [8]. In addition, the isolating transformer provide a beneficial voltage boosting as well as Electro-Magnetic Interference (EMI) mitigation which is very critical in these applications [9].

Inspecting the different topologies of power electronic converters in [10] and [11], four buck-boost topologies that have the ability to be isolated with HF isolating transformers can be found namely, C5 (Cuk), F5, G5 (SEPIC), and P5, see Fig. 1. These converters have two principles for energy transfer between the input and output sides. For C5, G5, and P5, the energy is transferred instantaneously between the primary and secondary sides of the transformer without being

stored inside it. Consequently, a small transformer core can be used. While in F5, the energy is temporarily stored in the magnetic core of the transformer and then released after a period of time. So, the core volume limits the maximum transferred energy which equals ½BH ×Volume [9].

For the abovementioned buck-boost topologies, the input current is continuous and therefore the input filtering capacitances are not necessarily large. This allows using plastic or film capacitors which have lifetime much longer than electrolytic capacitors rated at the same operating voltages and currents. The rise of the system operational temperature causes a significant reduction in the electrolytic capacitors lifetime [9]. Consequently, eliminating electrolytic capacitors can significantly improve the reliability of converters [12]-[13].

This paper presents a new modular converter structure for a three-phase medium-voltage PV system based on the HF isolated current source buck-boost converters shown in Fig. 1. As shown in the block diagram in Fig. 2, the output terminals of the modules of each phase are connected in series in order to increase the total output voltage and to enable direct grid connection. The proposed structure provides the required galvanic grid-isolation and voltage boosting. In addition, it eliminates the need to bulky line-frequency transformers and reduces the required line filters. The magnetic isolation in each submodule aids in reducing the common mode and voltage imbalance problems in PV modules. Owing to the continuous current nature at the input side, the candidates for this structure are suitable for Maximum Power Point Tracking (MPPT) operation for PV applications without the need to install large electrolytic capacitors. Therefore, the system's reliability can be improved. Unlike the conventional half-bridge MMC structures, the proposed topology can block dc and ac faults at input and output sides respectively. The modular and scalable nature of the proposed topology helps in reducing the cost and increase the reliability in the perspective of large-scale PV applications [14]-[15].

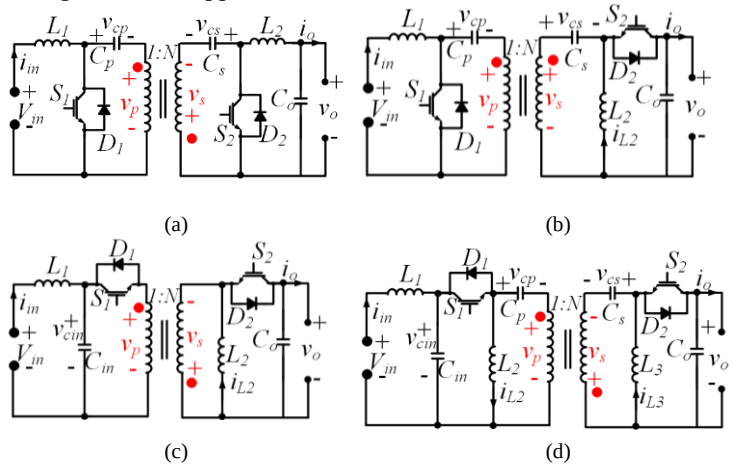


Fig. 1. HF-isolated converters (a) C5, (b) F5, (c) G5, and (d) P5

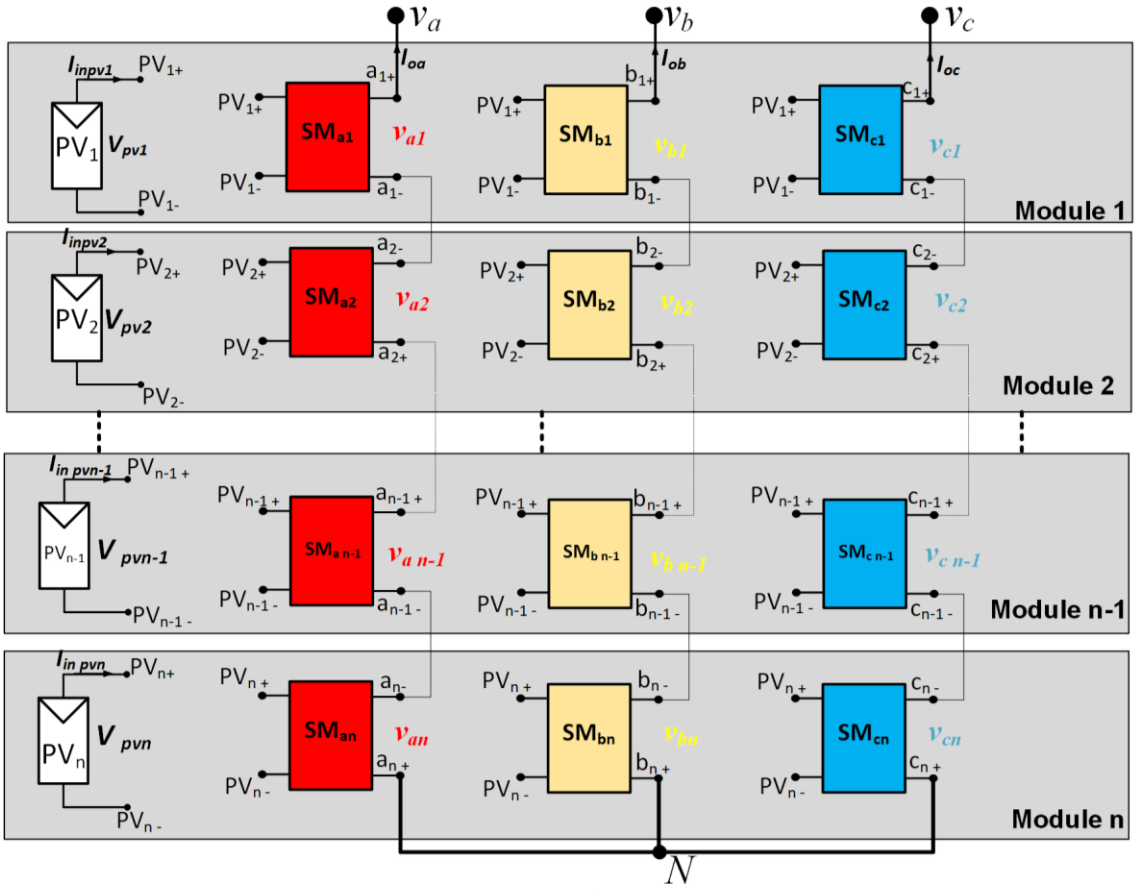


Fig. 2. Block diagram of the proposed converter

The paper explains the basic operation and provides the mathematical analysis of the proposed structure. Additionally, comparisons between the different possible candidates in terms of power losses, voltage/current ripples, stresses, switch ratings and total efficiencies are provided. The practical feasibility of the proposed structure is assessed with a scaled-down 5 kVA three-phase, 1 kV prototype using four modules for each phase and controlled with TMS320F28335 DSP.

II. System Description

For all the selected converter candidates, the modulation principle is shown in Fig. 3 and can be described as follows:

(i) During period t_{on}, where S_1 is on and S_2 is off, the inductors energize while the capacitors discharge. δ is the duty ratio as $t_{on} = \delta t_s$ while t_s is the switching period of the converter.
(ii) During period t_{off}, where S_1 is off and S_2 is on, the inductors de-energize while the capacitors charge. $t_{off} = (1-\delta)t_s$. The duty ratio value is compared to a saw-tooth carrier signal with frequency $f_s = 1/t_s$. Hence, v_o can be expressed as:

$$v_o = \frac{\delta}{1-\delta} NV_{in} \tag{1}$$

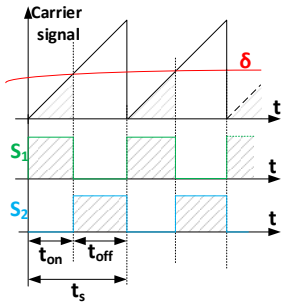


Fig. 3. Modulation principle for the converter candidates

The proposed system in Fig. 2 can operate in two different modes of operation. To explain that, two successive submodules (SMs) *m*-1 and *m* have been selected in Fig. 4a where *m* is an even number. In the first mode (Mode 1), the modules are fed from different PV arrays as shown in Fig.4b. The SMs output voltages can be written as:

$$v_{a\,m-1} = \tfrac{1}{2} V_{m-1} \sin \omega t + V_{d\,cm-1} \tag{2a}$$

$$v_{a\,m} = \tfrac{1}{2} V_m \sin(\omega t + \pi) + V_{d\,cm} \tag{2b}$$

$$v_{a\,mo} = \tfrac{1}{2} V_{m-1} \sin \omega t + V_{d\,cm-1} - \tfrac{1}{2} V_m \sin(\omega t + \pi) - V_{d\,cm} \tag{2c}$$

if $V_{m-1} = V_m$ and $V_{dcm-1} = V_{dc\,m}$ so the output voltage is:

$$v_{a\,mo} = V_m \sin \omega t \tag{3}$$

In the second mode of operation (Mode 2), shown in Fig.4c, the two successive SMs are fed from the same PV arrays and each SM operates for only half cycle without adding the dc offset. The equations can be expressed as:

$$v_{a\,m-1} = \begin{cases} V_{m-1} \sin \omega t & 0 \geq \omega t \geq \pi \\ 0 & \pi > \omega t \geq 2\pi \end{cases} \tag{4a}$$

$$v_{a\,m} = \begin{cases} 0 & 0 \geq \omega t \geq \pi \\ V_m \sin(\omega t + \pi) & \pi > \omega t \geq 2\pi \end{cases} \tag{4b}$$

Again, if $V_{m-1} = V_m$, the output voltage is:

$$v_{a\,mo} = V_m \sin \omega t \tag{5}$$

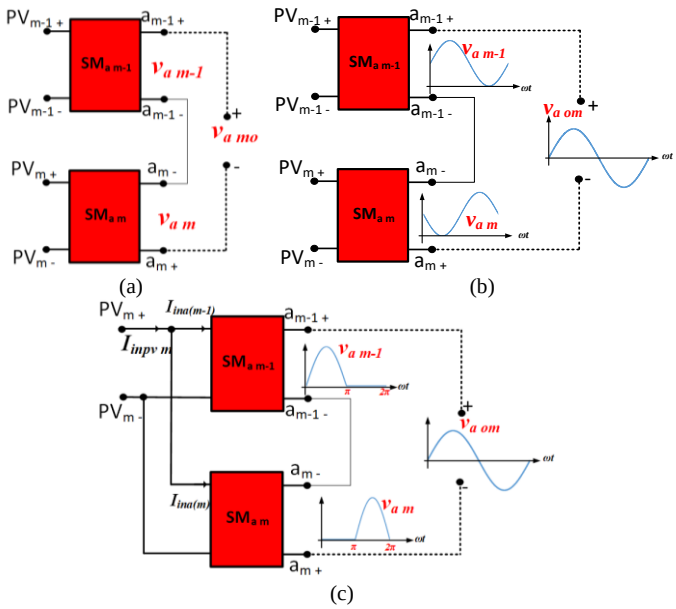


Fig. 4. Modes of operations: (a) basic structure, (b) Mode 1, and (c) Mode 2

If the output voltage peaks are equal in the two modes, the input PV current ($I_{inpv\,m}$) will be doubled in Mode 2. However, the maximum voltage and current stresses across and through the switches and the diodes are equal in the two modes. Due to the absence of dc voltages in the SMs, it is expected that Mode 2 will have lower losses and better efficiency than Mode 1. In this paper, Mode 2 will be analyzed in details and then a comparison with Mode 1 will be provided.
The output voltages and currents can be expressed as:

$$v_{oj} = V_m \sin(\omega t + \varphi_j) \tag{6a}$$

$$i_{oj} = I_m \sin(\omega t + \varphi_j - \gamma) \tag{6b}$$

where *j* represents phase a, b, or c and $\varphi_j = \{0, -\tfrac{2}{3}\pi, \tfrac{2}{3}\pi\}$. The duty ratio of the SM number '*k*' in phase '*j*' can be calculated from:

$$\frac{v_{ojk}}{NV_{in}} = \frac{\delta_{jk}}{1-\delta_{jk}}$$
$$\delta_{jk} = \frac{v_{ojk}}{v_{ojk} + NV_{in}} \tag{7}$$

To show the basic operation of the three-phase system, a MATLAB/SIMULINK® model is built using the conditions and parameters in Table I for the C5 converter. Because the system is balanced and all SMs are identical, the first SM in phase *a* has been shown. Fig. 5a shows the simulation results for the first PV array current I_{inpv1} with the input current of the first C5 SM in phase a (I_{ina1}). Because each two successive SMs in any phase are connected to the same PV array, the PV arrays number is halved. Figs. 5b shows the voltage across the primary and secondary capacitors (V_{cpa1} and V_{csa1}) respectively. The output voltages for the first successive two SMs in phase a (V_{a1} and V_{a2}) are shown in Fig. 5c. The three-phase output current of the system is shown in Fig. 5d.

TABLE I
PARASITIC COMPONENT VALUES AND CIRCUIT CONDITIONS

Parameter	Value
Three-phase output voltage	11 kV
Output power	P_o = 1 MW
Number of modules	n = 50
PV array voltage	V_{in} = 300VDC
Turns ratio	N = 2
Input and output inductors	$L_1 = L_2$ = 1 mH
Primary and secondary sides capacitors	$C_p = C_s$ = 10 µF
Output capacitor	C_o =1 µF

As shown in the results in Fig. 5, the PV arrays currents are continuous and constant so MPPT can be applied. The voltage and current stresses across the elements and the semiconductor switches can be reduced by increasing the modules number and decreasing the PV arrays voltages.

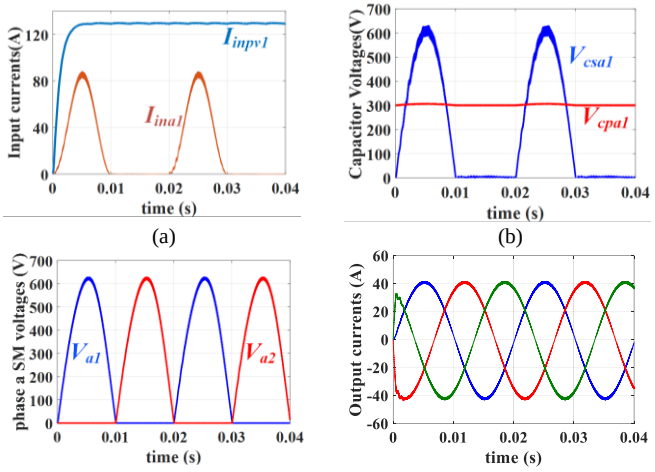


Fig. 5. Simulation results of the proposed system using C5 SMs: (a) I_{inpv1} and $I_{ina1,}$ (b) V_{cpa1} and V_{csa1}, (c) V_{a1} and V_{a2}, and (d) three-phase output current

III. COMPARISONS BETWEEN CANDIDATES

This section discusses the parameter selection of the different converter candidates and provides comparisons between them. The four possible candidates have differences regarding their input/output ripples, passive elements stresses and the transformer core size as stated earlier. However, all candidates have the same semiconductors stresses (voltages and currents) at the same operating conditions.

A. Parameters Selection and Comparison

Assuming short switching periods (t_s) for C5 converter, the currents and voltages can be considered linear as in Fig. 6. Averaging the circuit of C5 SM along the periods t_{on} and t_{off} yields:

$$L_1 = \frac{\delta_{\max} V_{in} t_s}{I_{mL1} x_{L1}} \tag{8a}$$

$$L_2 = \frac{\delta_{\max} V_{in} t_s}{I_m x_{L2}} .N \tag{8b}$$

where x_{L1} and x_{L2} are the maximum allowable current ripple factor for L_1 and L_2 currents respectively.

$$x_{L1} = \frac{\Delta I_{L1(peak)}}{I_{mL1}} \quad and \quad x_{L2} = \frac{\Delta I_{L2(peak)}}{I_m} \tag{9}$$

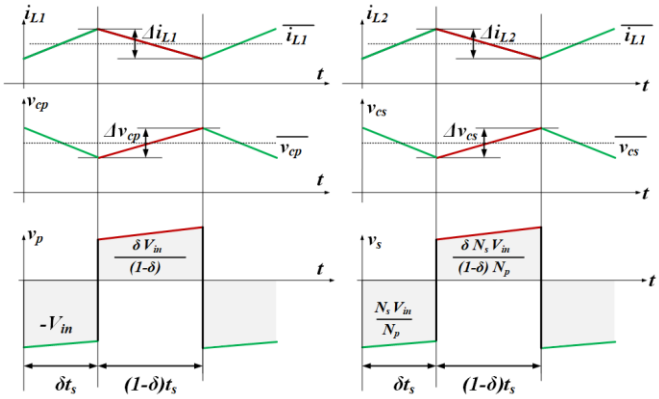


Fig. 6. C5 (*Ćuk*) operation during one sample period t_s

In practice, these factors are usually selected as 10% of the peak current values. Similarly, the capacitor of the SM can be expressed as:

$$C_p = \frac{\delta_{\max} I_m t_s T}{V_{in} x_{cp}} \tag{10a}$$

$$C_s = \frac{\delta_{\max} I_m t_s}{N V_{in} x_{cs}} \tag{10b}$$

where x_{cp} and x_{cs} are the maximum allowable voltage ripple factor for C_p and C_s currents respectively.

$$x_{cp} = \frac{\Delta V_{c_p(peak)}}{V_{in}} \quad and \quad x_{cs} = \frac{\Delta V_{c_s(peak)}}{V_m} \tag{11}$$

The output capacitance C_o is responsible for improving the Total Harmonic Distortion (THD) by providing additional filtering to I_{L2} and reduce the ripples in the output current I_o and can be selected according to:

$$C_o = \frac{I_m t_s}{2\pi V_m x_o} \tag{12}$$

where x_o is the maximum output current ripple:

$$x_o = \frac{\Delta I_{o(peak)}}{\Delta I_{L2(peak)}} \tag{13}$$

Table II lists the formulas for selecting the parameters of other candidate converters. The passive elements are usually selected to keep the currents and voltages of the passive elements under 10% and to keep the THD of the output current below 5%. Also, the input current ripples should be kept low as possible to enable a proper operation of the MPPT controller and hence maximum power can be harvested from the PV arrays [16]. Figs. 7, 8 and 9 show the simulation results for the proposed three-phase system with the other SM candidates. Since the three phases are identical and balanced, the currents and voltages of the first SM in phase *a* are only shown. Fig. 10a shows a comparison between the required capacitances for different candidate SMs. Fig. 10b shows the total inductance required for the different SMs. It is obvious that although the P5-based system requires the highest capacitance values, it requires the lowest inductances. So, it is

controversy to interpret that as an indicator for SMs sizes. The maximum stored energy in a SM can be calculated from (14).

TABLE II
PARASITIC COMPONENT FORMULAS

SM type	Element	Formula	Ripple factor
F5	C_{in}	$\frac{\delta_{\max} N I_m t_s}{V_{in} x_{cin}}$	$x_{cin} = \frac{\Delta V_{cin\ (peak)}}{V_{in}}$
	L_1	$\frac{(1-\delta_{\max}) t_s^{\ 2}}{4 C_{in} V_{in} x_{L1}}$	$x_{L1} = \frac{\Delta I_{in\ (peak)}}{I_{in}}$
	L_2	$\frac{\delta_{\max}(1-\delta_{\max}) t_s N V_{in}}{x_{L2} I_m}$	$x_{L2} = \frac{\Delta I_{L2\ (peak)}}{I_m}$
	C_o	$\frac{(1-\delta_{\max}) t_s I_m}{x_o N V_{in}}$	$x_o = \frac{\Delta I_{o\ (peak)}}{I_m}$
G5	L_1	$\frac{\delta_{\max} V_{in} t_s}{I_{mL1} x_{L1}}$	$x_{L1} = \frac{\Delta I_{L1(peak)}}{I_{mL1}}$
	C_p	$\frac{\delta_{\max} I_m t_s N}{V_{in} x_{cp}}$	$x_{cp} = \frac{\Delta V_{c_p(peak)}}{V_{in}}$
	C_s	$\frac{(1-\delta_{\max}) t_s I_m}{x_{cs} N V_{in}}$	$x_{cs} = \frac{\Delta V_{c_s(peak)}}{V_m}$
	L_2	$\frac{\delta_{\max} V_{in} t_s}{I_m x_{L2}} . N$	$x_{L2} = \frac{\Delta I_{L2(peak)}}{I_m}$
	C_o	$\frac{\delta_{\max} I_m t_s}{N V_{in} x_o}$	$x_o = \frac{\Delta I_{o\ (peak)}}{I_m}$
P5	L_1, C_{in} and C_o	Same as F5	Same as F5
	L_2	$\frac{(1-\delta_{\max}) t_s V_{in}}{x_{L2} I_m N}$	$x_{L2} = \frac{\Delta I_{L2\ (peak)}}{I_m}$
	C_p	$\frac{\delta_{\max} I_m t_s N}{V_{in} x_{cp}}$	$x_{cp} = \frac{\Delta V_{c_p(peak)}}{V_{in}}$
	L_3	$\frac{\delta_{\max} V_{in} t_s N}{x_{L3} I_m}$	$x_{L3} = \frac{\Delta I_{L3\ (peak)}}{I_m}$
	C_s	$\frac{\delta_{\max} t_s I_m}{x_{cs} V_m}$	$x_{cs} = \frac{\Delta V_{c_p(peak)}}{V_m}$

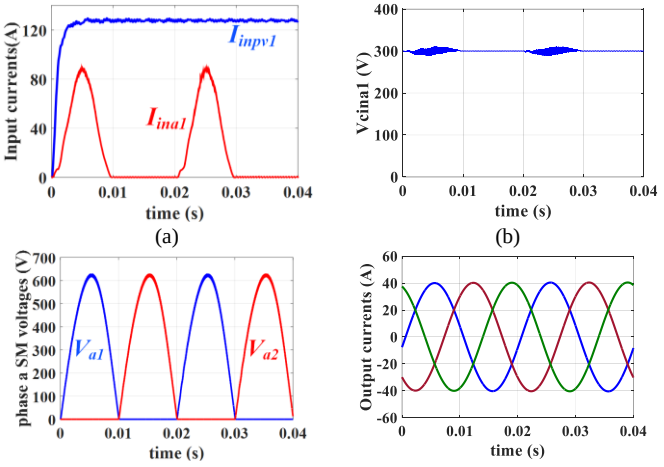


Fig. 7. Simulation results of the proposed system using F5 SMs: (a) I_{inpv1} and $I_{ina1,}$ (b) V_{cina1}, (c) V_{a1} and V_{a2}, and (d) three-phase output current

$$E_{stored} = \sum_{k=1}^{n} \left[\frac{1}{2} L_k I^2_{Lk-peak} + \frac{1}{2} C_k V^2_{Ck-peak} \right] \qquad (14)$$

Table III lists the maximum value of the stresses on each passive element. Fig. 11 is generated by substituting these maximum values in (14) to show the different estimated sizes of the different SMs. The C5 SM stores the lowest energy and therefore is expected to have the smallest size and volume.

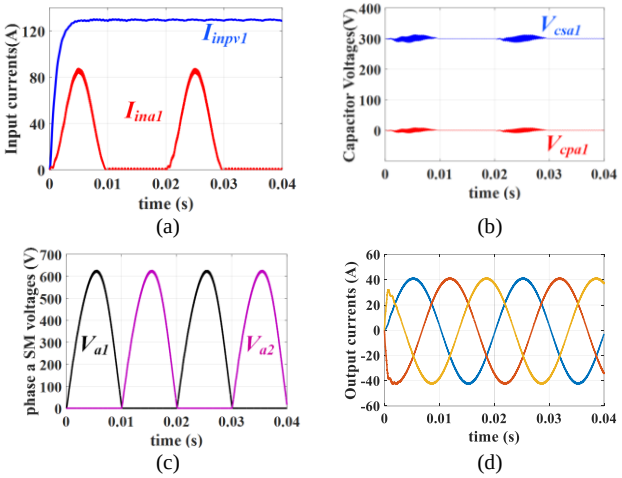


Fig. 8. Simulation results of the proposed system using G5 SMs: (a) I_{inpv1} and $I_{ina1,}$ (b) V_{cpa1} and V_{csa1}, (c) V_{a1} and V_{a2}, and (d) output current

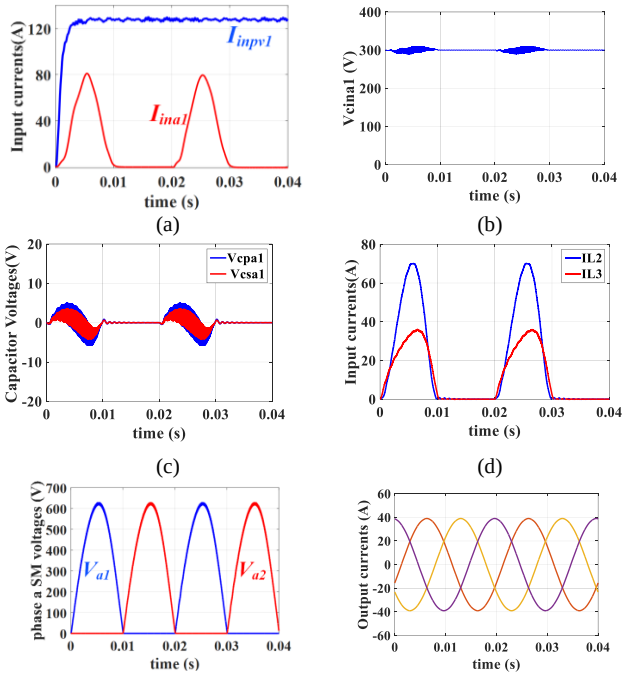


Fig. 9. Simulation results of the proposed system using P5 SMs: (a) I_{inpv1} and $I_{ina1,}$ (b) V_{cina1}, (c) V_{cpa1} and V_{csa1}, and (d) I_{L2a1} and I_{L3a1} (e) V_{a1} and $V_{a2,}$ and (f) three-phase output current

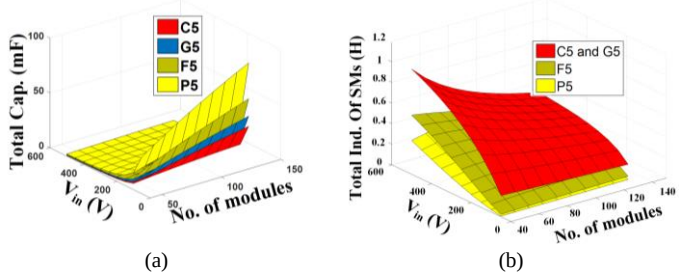


Fig. 10. Passive elements in candidate SMs: (a) Capacitance and (b) inductance

On the other hand, F5 SM stores the highest energy and hence it will have the largest size. A further discussion about the practicality, advantages and disadvantages of different SMs will be carried out in Section VII.

TABLE III
STRESSES ON PASSIVE ELEMENTS

SM type	Element	V/I	Formula	Maximum Value
C5	C_p	v_{cp}	V_{in}	V_{in}
	L_1	i_{L1}	$\frac{\delta}{1-\delta} i_o N$	$\frac{V_m}{V_{in}} I_m$
	C_s	v_{cs}	$\frac{\delta}{1-\delta} V_{in} N$	V_m
	L_2	i_{L2}	i_o	I_m
	C_o	v_{co}	v_o	V_m
F5	L_1	i_{in}	$\frac{\delta}{1-\delta} i_o N$	$\frac{V_m}{V_{in}} I_m$
	C_{in}	v_{cin}	V_{in}	V_{in}
	L_2	I_{L2}	$\frac{1}{1-\delta} i_o$	$\frac{V_m / N + V_{in}}{V_{in}} I_m$
	C_o	v_{co}	v_o	V_m
G5	L_1	i_{L1}	$\frac{\delta}{1-\delta} i_o N$	$\frac{V_m}{V_{in}} I_m$
	C_p	v_{cp}	V_{in}	V_{in}
	C_s	v_{cs}	0	0
	L_2	i_{L2}	i_o	I_m
	C_o	v_{co}	v_o	V_m
P5	L_1	i_{in}	$\frac{\delta}{1-\delta} i_o N$	$\frac{V_m}{V_{in}} I_m$
	C_{in}	v_{Cin}	V_{in}	V_{in}
	L_2	i_{L2}	$\frac{\delta}{1-\delta} i_o N$	$\frac{V_m}{V_{in}} I_m$
	C_p	v_{cp}	0	0
	L_3	i_{L2}	i_o	I_m
	C_p	v_{cs}	0	0
	C_o	v_{co}	v_o	V_m

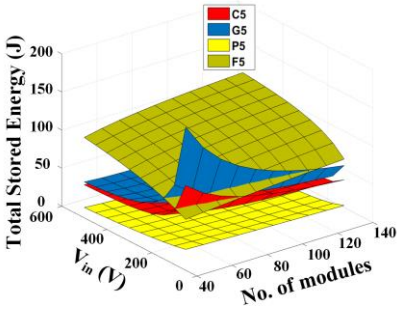
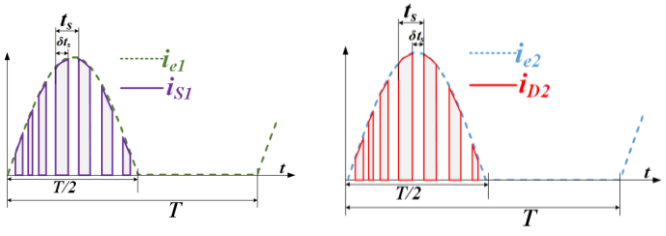


Fig. 11. Total Stored Energy Comparison

B. Semiconductors power losses

By operating in Mode 2, stated earlier, the four SM candidates have the same current and voltage through and across them. Devices S_1 and D_2 are conducting current in one half cycle while they are off in the other one. Devices S_2 and D_1 are always off and they are required only in Mode 1. The currents through these devices are shown in Fig. 12.



(a) $S_1 - D_1$ (b) $D_2 - S_2$

Fig. 12. Semiconductor devices currents in Mode 2

The devices conduction power loss in one SM can be expressed as [17]:

$$P_{SM-cond} = P_{s1-cond} + P_{D2-cond} \tag{15a}$$

where

$$P_{S1-cond} = R_{on} I^2_{s1-rms} + v_{co} I_{s1-avg}$$
$$P_{D2-cond} = R_F I^2_{D2-rms} + v_F I_{D2-avg} \tag{15b}$$

where I_{s1_rms} and I_{D2_rms} are the rms currents through S_1 and D_2, currents I_{s1_avg} and I_{D2_avg} are the average currents, R_{on} and R_F are the on-state and forward resistances of S_1 and D_2 devices, v_{co}, v_F are the collector–emitter and forward voltage drops of S_1 and D_2 respectively. From Fig. 12, the rms currents can be calculated as:

$$\begin{aligned} I^2_{s1-rms} &= \frac{1}{T}\int_0^{T/2} i^2_{s1} dt = \frac{1}{T}\int_0^{T/2} i^2_{e1}\delta dt \\ &= \frac{1}{T}\int_0^{T/2} (\frac{N}{1-\delta} i_o)^2 \delta dt \\ &= \frac{I_m^2 V_m}{V_{in}} \left\{ \frac{N(3+\cos 2\gamma)}{6\pi} + \frac{V_m(2+\cos 2\gamma)}{32\pi V_{in}} \right\} \end{aligned} \tag{16}$$

$$\begin{aligned} I^2_{D2-rms} &= \frac{1}{T}\int_0^{T/2} i^2_{D2} dt = \frac{1}{T}\int_0^{T/2} i^2_{e2}(1-\delta) dt \\ &= \frac{1}{T}\int_0^{T/2} (\frac{i_o}{1-\delta})^2 (1-\delta) dt \\ &= \frac{I_m^2}{4} + \frac{I_m^2 V_m}{V_{in}} \left\{ \frac{3+\cos 2\gamma}{24\pi} \right\} \end{aligned} \tag{17}$$

Similarly, the average currents can be calculated as:

$$\begin{aligned} I_{s1-avg} &= \frac{1}{T}\int_0^{T/2} i_{s1} dt = \frac{1}{T}\int_0^{T/2} i_{e1}\delta dt \\ &= \frac{1}{T}\int_0^{T/2} (\frac{N\delta}{1-\delta} i_o) dt \\ &= \frac{I_m V_m}{4V_{in}} \cos\gamma \end{aligned} \tag{18}$$

$$\begin{aligned} I_{D2-avg} &= \frac{1}{T}\int_0^{T/2} i_{D2} dt = \frac{1}{T}\int_0^{T/2} i_{e1}(1-\delta) dt \\ &= \frac{1}{T}\int_0^{T/2} (\frac{i_o}{1-\delta})(1-\delta) dt \\ &= \frac{I_m}{\pi} \end{aligned} \tag{19}$$

Assuming balanced three-phase system, the total devices conduction power loss can be calculated from:

$$P_{sys-cond} = 3n(P_{s1-cond} + P_{D2-cond}) \tag{20}$$

The switching power can be estimated as [18]

$$P_{SM-sw} = \frac{V_{in} I_{s1-avg}}{2}(T_{on} + T_{off}) \tag{21}$$

where T_{on} and T_{off} are the turn-on time and turn-off time of the switch S_1. Similarly, the total switching power losses in the three-phase system can be calculated from:

$$P_{sys-sw} = 3\ n\ P_{SM-sw} \tag{22}$$

C. Inductors power losses

The formulas describing the current through the inductor of each candidate converter are listed in Table III. For C5 as an

example, the current through L_1 can be expressed as:

$$i_{L1}=\begin{cases}\dfrac{\delta}{1-\delta}i_o N=\dfrac{V_m I_m}{2V_{in}}\cos\gamma-\dfrac{V_m I_m}{2V_{in}}\cos(2\omega t-\gamma) & 0\le\omega t<\pi\\ 0 & \pi\le\omega t<2\pi\end{cases} \quad (23)$$

If r_1 is the internal resistance of L_1, the power loss can be estimated from:

$$P_{L1}=i^2_{L1-rms}\,r_1=\frac{V^2_m I^2_m}{16V^2_{in}}(2+\cos 2\gamma)r_1 \quad (24)$$

Similarly, the current in L_2 is:

$$i_{L2}=\begin{cases}i_o & 0\le\omega t<\pi\\ 0 & \pi\le\omega t<2\pi\end{cases} \quad (25)$$

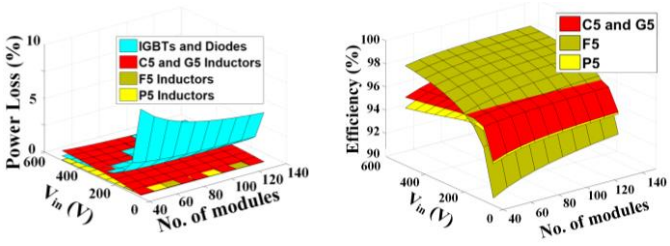
And the power loss in L_2:

$$P_{L2}=i^2_{L2-rms}\,r_2=\frac{I^2_m}{4}r_2 \quad (26)$$

For inductor currents with formula of $\frac{1}{1-\delta}i_o$, as i_{L2} in F5, the power loss and rms current can be expressed as:

$$P_{L2}=i^2_{L2-rms}\,r_2=\frac{V^2_m I^2_m}{V^2_{in}}\left(\frac{\cos^2\gamma}{8N^2}+\frac{1}{16N^2}+\frac{1}{4}+\frac{\cos\gamma}{N\pi}\right)r_2 \quad (27)$$

The inductors losses in any converter can be estimated from (24), (26), and (27) as all SM currents are following these three formulas, see Table III. Fig. 13a shows the power losses plots for the different SMs while Fig. 13b shows the total efficiency of the SMs according to the previous analysis.



(a) (b)

Fig. 13. (a) Power losses in switches and inductors and (b) total efficiency

IV. Experimental Results for Mode 2

To show the operation of the proposed structure, a scaled-down 5 kVA three-phase, 1 kV prototype is built with four modules and controlled with TMS320F28335 DSP. The experimental setup is shown in Fig. 14. The SMs are built with changeable terminals to enable testing different converter candidates using the same configuration. Table IV shows the circuit parameters for the setup. Figs. 15 to 18 show the results of the proposed three-phase system under an open-loop operation and considering the small mismatches between the different passive elements in each SM. The results can be compared to the computer simulations in section III.

V. A Comparison between Mode 1 and Mode 2

Examining Mode 1 in a similar way, the devices currents can be shown as in Fig. 19. For S_1 and D_1 (the input side devices), each device is conducting in one half cycle period. For S_1, the rms current I_{s1_rms} can be calculated from:

$$I^2_{s1-rms}=\frac{V_m I^2_m}{V^2_{in}}\left[\frac{2NV_{in}+V_m}{8}+\frac{(V_m+NV_{in})(3+\cos 2\gamma)}{6\pi}+\frac{V_m(2+\cos 2\gamma)}{32}\right] \quad (28)$$

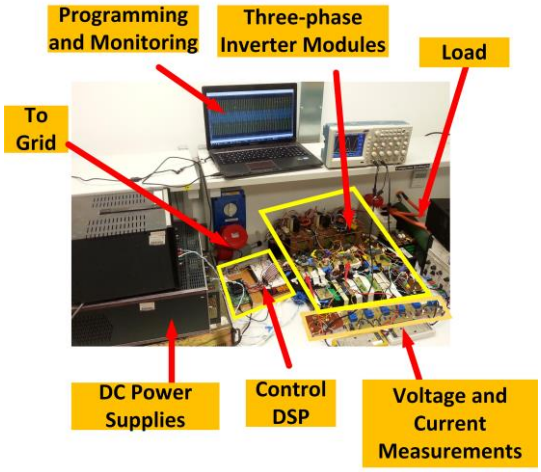
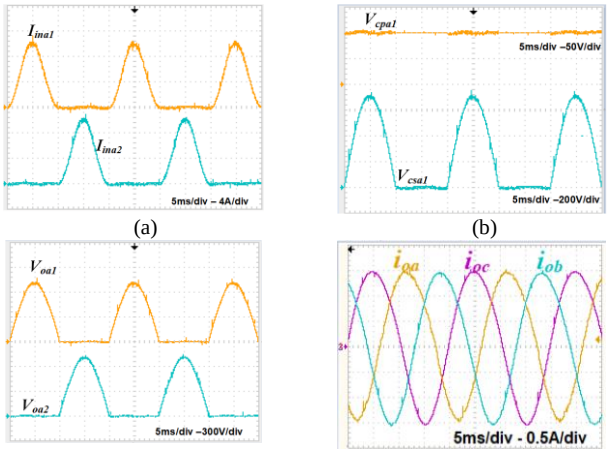
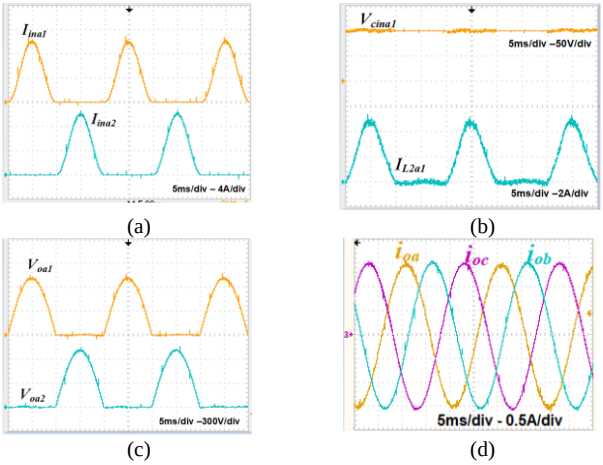


Fig. 14. Experimental setup



(a) (b) (c) (d)

Fig. 15. Experimental results of the C5-based system: (a) input currents for the SM1a and SM2a, (b) middle capacitors' voltages of SM1a, (c) output voltages of SM1a and SM2a, and (d) output three-phase currents



(a) (b) (c) (d)

Fig. 16. Experimental results of the F5-based system: (a) input currents for the SM1a and SM2a, (b) input capacitor (C_{in}) voltage and secondary inductor current (L_2) of SM1a, (c) output voltages of SM1a and SM2a, and (d) output three-phase currents

The rms value for the diode current I_{D1} can be calculated from:

$$I^2_{D1-rms} = \frac{I_m^2}{V_{in}^2}\left[\frac{V_m(2NV_{in}+V_m)}{4} - \frac{V_m(V_m+NV_mV_{in})(3+\cos 2\gamma)}{6\pi} + \frac{V_m^2(2+\cos 2\gamma)}{32}\right] \quad (29)$$

TABLE IV
CIRCUIT PARAMETERS OF EXPERIMENTAL SETUP

Parameter	Value
R.M.S output voltage	1 kV
Output power	P_o = 3 kW
Number of modules	n = 4
Input DC voltage	V_{in} = 100VDC
Turns' ratio	N = 3
Switching frequency	25 kHz
Semiconductor switch (IGBT)	IRG4PC50FPbF (600V, 70A)
Diode	FFSH40120ADN (1200V, 40A)
Output load	500 Ω

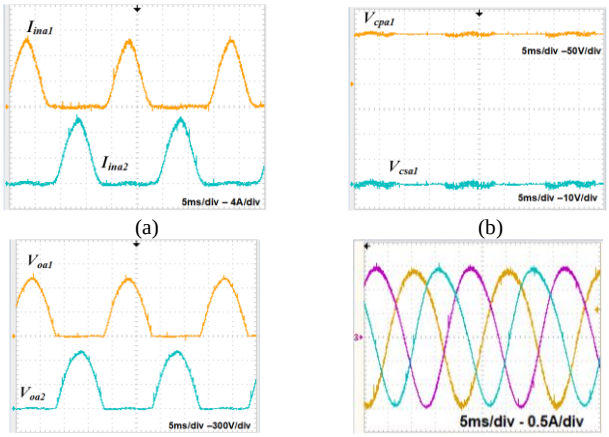


Fig. 17. Experimental results of the G5-based system: (a) input currents for the SM1a and SM2a, (b) middle capacitors' voltages of SM1a, (c) output voltages of SM1a and SM2a, and (d) output three-phase currents

The average values of I_{s1} and I_{D1} can be expressed as:

$$I_{s1-avg} = \frac{I_m V_m \cos\gamma}{V_{in}}\left(\frac{4+\pi}{8\pi}\right) \quad (30)$$

$$I_{D1-avg} = \frac{I_m \cos\gamma}{V_{in}}\left(\frac{V_{dc}}{\pi} + \frac{V_m}{8}\right) \quad (31)$$

Similarly, the rms and average values of the output side devices (S_2 and D_2) can be calculated from:

$$I^2_{s2-rms} = \frac{I_m^2}{V_{in}}\left[\frac{NV_{in}+V_{dc}}{4N} + \frac{V_m(3+\cos 2\gamma)}{12N\pi}\right] \quad (32)$$

$$I^2_{D2-rms} = \frac{I_m^2}{V_{in}}\left[\frac{NV_{in}+V_{dc}}{4N} - \frac{V_m(3+\cos 2\gamma)}{12N\pi}\right] \quad (33)$$

$$I_{s2-avg} = I_{D2-avg} = \frac{I_m \cos\gamma}{\pi} \quad (34)$$

The total semiconductor conduction losses can be calculated from:

$$P_{SM-cond} = P_{s1-cond} + P_{D1-cond} + P_{s2-cond} + P_{D2-cond} \quad (35)$$

$$P_{S1-cond} = R_{on} I^2_{s1-rms} + v_{co} I_{s1-avg}$$

$$P_{D1-cond} = R_F I^2_{D1-rms} + v_F I_{D1-avg}$$

$$P_{S2-cond} = R_{on} I^2_{s2-rms} + v_{co} I_{s2-avg}$$

$$P_{D2-cond} = R_F I^2_{D2-rms} + v_F I_{D2-avg}$$

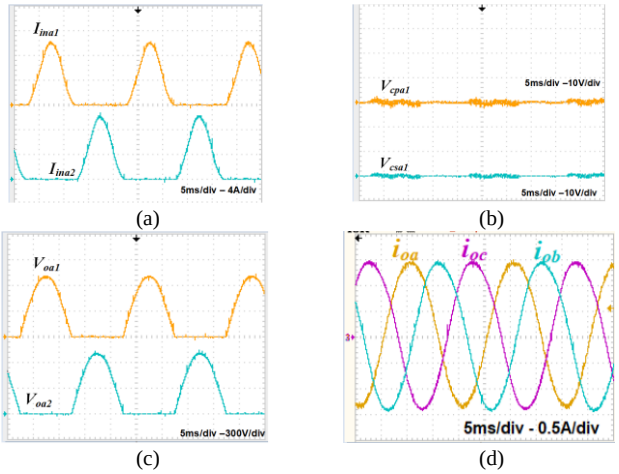
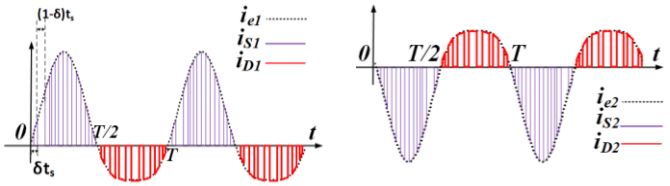


Fig. 18. Experimental results of the P5-based system: (a) input currents for the SM1a and SM2a, (b) middle capacitors' voltages of SM1a, (c) output voltages of SM1a and SM2a, and (d) output three-phase currents



(a) $S_1 - D_1$ (b) $S_2 - D_2$

Fig. 19. Semiconductor devices currents in Mode 1

The currents through different inductors have three different formulas as listed in Table III.

The three formulas are: (i) $i_{L1} = \frac{\delta}{1-\delta} i_o N$, (ii) $i_{L2} = i_o$ and (iii) $i_{L3} = \frac{i_o}{1-\delta}$.

The rms values for these formulas can be expressed as:

$$i^2_{L1\_rms} = \frac{V_{dc}^2 I_m^2}{2V_{in}^2} + \frac{V_m^2 I_m^2 (2+\cos 2\gamma)}{32V_{in}^2} \quad (36a)$$

$$i^2_{L2\_rms} = \frac{(NV_{in}+V_{dc})^2 I_m^2}{2N^2 V_{in}^2} + \frac{V_m^2 I_m^2 (2+\cos 2\gamma)}{32N^2 V_{in}^2} \quad (36b)$$

$$i^2_{L3\_rms} = \frac{I_m^2}{2} \quad (36c)$$

Because the system is balanced and identical, the total power losses in the inductors can be calculated by multiplying the power losses in the submodule by 3n.

Comparing the devices and inductor power losses, it can be deduced that the power losses of the submodules operating in Mode 1 are higher when compared with Mode 2. The experimental comparison of the system under the two modes is shown in Fig. 20. The losses breakdown of each converter are shown in Fig. 21. On the other hand, the input module current is halved in Mode 1 and therefore it may be desirable when it is required to reduce the dc current of the PV arrays. The selection process of the most suitable converter candidate depends on the system conditions as well as its desired performance. The system's performance can be measured by four main aspects: (i) total efficiency, (ii) system's reliability (iii) total size, and (iv) number of passive element.

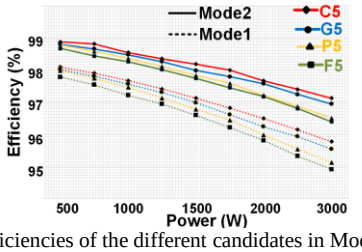


Fig. 20. Total efficiencies of the different candidates in Mode 1 and Mode 2

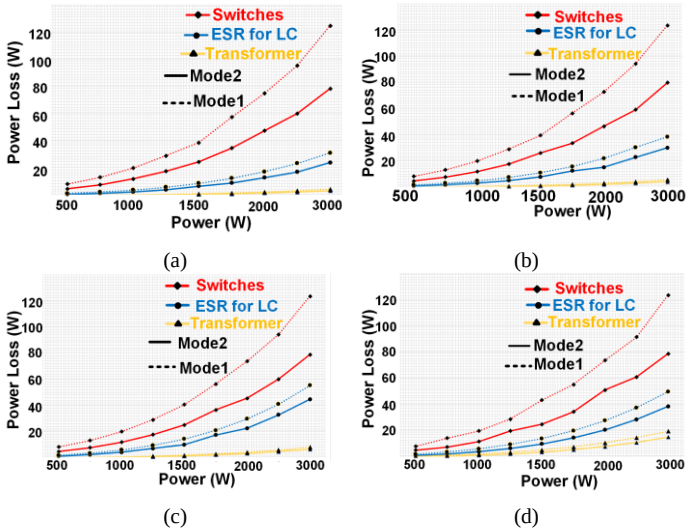


Fig. 21. Losses breakdown: (a) C5, (b) G5, P5, and (d) F5

The total efficiency can be measured from the total losses of each candidate while the reliability of the system is directly proportional with reducing the maximum stresses of the semiconductor devices as well as the electrolytic capacitors in the system. The total size of the system can be sensed by calculating the stored energy inside the passive elements. From the previous analyses and results, the selection process will depend on the nominal input voltage from the PV arrays as well as the number of the modules. For the system in Table I as an example, the PV arrays at the input side are connected to provide a nominal voltage of 300V to the terminals of each of the 50 modules. From the efficiency analysis in Fig. 13b, it can be deduced that the best candidate in terms of the total efficiency is F5, followed by C5, G5 and finally P5. Considering the reliability of the different candidates in the second place, it can be found that the total required capacitances as well as the maximum stresses of the semiconductor devices are very similar at 300V input voltage, see Fig. 10. Then, it can be seen from Fig. 11 that F5 has the largest size followed by G5, C5 and then P5. However, P5 converter has the highest number of passive elements, followed by C5, G5 and then F5. For these reasons, it can be deduced that C5 converter is the best compromise at the decided conditions and criteria. However, this choice will be different if the nominal arrays voltages have been changed or the design priorities are different. For example, if the size is not an important criterion for the designer.

VI. Performance of the Proposed Topology During Partial Shading

This section describes the general performance for the proposed system's operation during partial shading of PV arrays and the basic methodology for the MPPT controller. Assuming that the system is operating in Mode 1 and connected to the grid via three-phase lines of per-phase impedance $z = r+X_L$, the output currents can be expressed as:

$$i_{oj}(t) = \frac{n/2\left[V_m + V_m \sin(\omega t + \theta + \varphi_j)\right] - V_g \sin(\omega t + \varphi_j)}{r + jX_L} = I_m \sin(\omega t - \gamma + \varphi_j) \quad (37)$$

where V_g, V_m, I_m are the peak values of the ac grid voltage, submodules ac output voltage, and system output current respectively. θ and γ are the phase-shift angles of submodule ac voltages and the output currents respectively while j represents phase a, b, *or* c and $\varphi_j = \{0, -⅔\pi, ⅔\pi\}$.

Neglecting the power loss in the cable resistances, the total output power of the system is calculated from:

$$P_{total} = \frac{3nV_m I_m \cos(\theta - \gamma)}{4} \approx \frac{3V_g I_m \cos(\gamma)}{2} \quad (38)$$

In normal operation, the unshaded modules power can be expresses as:

$$P_{\mathrm{mod}\_u} = V_{in} I_{in} \approx \frac{3V_m I_m \cos(\theta - \gamma)}{4} \quad (39)$$

The system reference voltages and currents are calculated from solving equations (37), (38) and (39), hence the system can track the maximum power point.

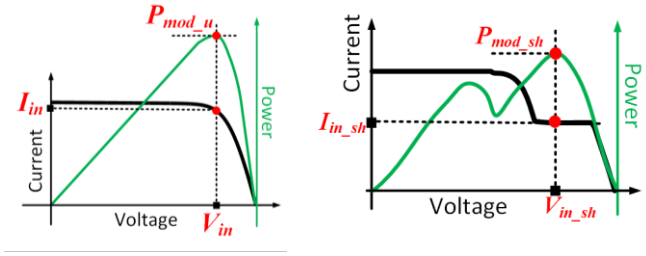


Fig. 22. I_V and P_V characteristics of the PV arrays: (a) unshaded, shaded

Fig. 22a shows the I–V and P–V characteristics of the unshaded PV arrays during normal conditions. During partial shading, the reference values of the grid current and modules output voltages can be adjusted to harvest the maximum available power from the system. To explain that briefly, a case where k modules of the system are shaded while other modules (n-k) are unshaded. Fig. 22b shows the I–V and P–V characteristics of the shaded PV arrays. It should be noted that the characteristics of the PV arrays change with their type, number of series/parallel cells inside each array. However, there will always be global and local peaks as shown in Fig. 22b. In this case, the new output currents can be calculated as:

$$i'_{oj}(t) = \frac{\left[\begin{array}{l} k/2\left[V_{m\_sh} + V_{m\_sh} \sin(\omega t + \theta_{sh} + \varphi_j)\right] + \\ (n-k)/2\left[V_m + V_m \sin(\omega t + \theta + \varphi_j)\right] - V_g \sin(\omega t + \varphi_j) \end{array}\right]}{r + jX_L} = I'_m \sin(\omega t - \gamma + \varphi_j) \quad (40)$$

where V_{m_sh} is the peak value of the shaded submodule output voltage, $I`_m$ is the new peak value of the output currents, and θ_{sh} is the phase angle of the shaded modules ac voltages. The shaded modules power can be calculated from:

$$P_{\mathrm{mod}\_sh} = V_{in\_sh} I_{in\_sh} \approx \frac{3V_{m\_sh} I'_m \cos(\theta_{sh} - \gamma)}{4} \quad (41)$$

The new total system power can be calculated from:

$$P'_{total} = \frac{3(n-k)V_m I'_m \cos(\theta - \gamma) + 3kV_{m\_sh} I'_m \cos(\theta_{sh} - \gamma)}{4} \approx \frac{3V_g I'_m \cos(\gamma)}{2} \quad (42)$$

The system new reference voltages and currents are calculated from solving equations (40), (41) and (42) in order to track the maximum available power points for unshaded and shaded modules.

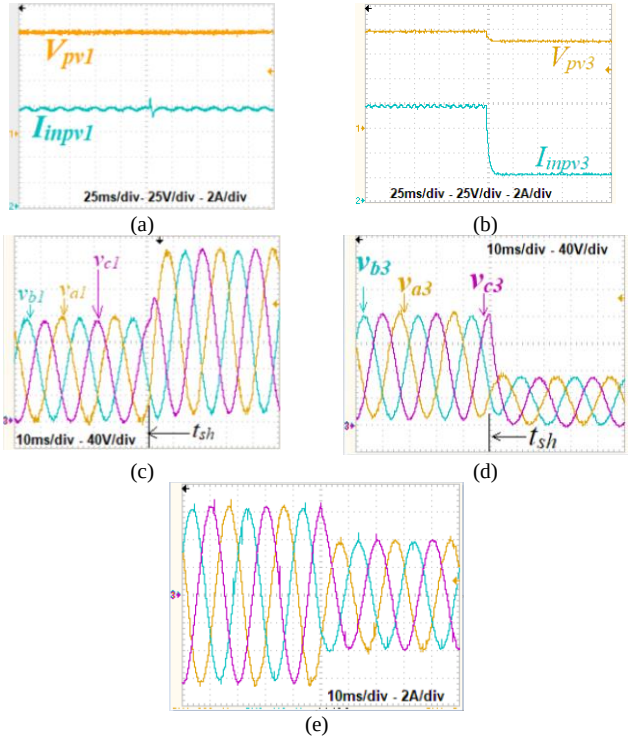


Fig. 23. Experimental results for C5 system in Mode 1 during partial shading: (a) input voltage and current of Module 1 (unshaded), (b) input voltage and current of Module 1 (shaded), (c) Module 1 output voltages, (d) Module 2 output voltages, and (e) output three-phase currents

Fig. 23 shows the experimental results of C5-based three-phase inverter, operating in Mode 1, to mimic the case when two of the four modules are shaded at a shading time (t_{sh}). In the normal unshaded condition, the system is connected to the grid and generates 3 kW evenly shared by the four modules per phase. So, each SM generates 250W and each three-phase module generates 750W. The peak of the three-phase voltage at the point of common coupling is V_g = 311V while the input voltage is 100V. At the shading conditions, the generated power of the lower two modules drops to 25%. Figs 23a and 23b show the input currents and voltages in module 1 and module 3. Fig 23c and d show the output voltages of module 1 and module 3. The system's output three-phase current is shown in Fig. 23e. In this case, the controller changed the reference values of the modules' voltages, and hence the output currents, in order to keep the two unshaded modules unchanged and deliver the maximum available power from the other two shaded modules.

VII. Discussion

According to the aforementioned theoretical analysis, computer simulations and experimental results, the following points can be deduced:

- The devices of the SMs are operating in only one half cycle in Mode 2 and therefore the semiconductor and copper losses are lower when compared with Mode 1. However, the input PV array currents are doubled in Mode 2 which requires more PV arrays to be connected in parallel at the input side.
- The total capacitance required in the SMs increases significantly when the input voltage (PV arrays' voltage) decreases. To satisfy the same voltage/current ripples requirements, P5 SM should have the highest capacitance values while the C5 SM should have the lowest.
- On the other hand, the total inductance required in the SMs increases with the input dc voltage. C5 SM has the highest inductance value while the P5 module has the lowest.
- Considering the energy in the SMs, P5 stores the lowest amount inside the transformer core and passive elements and hence the transformer core will have the smallest volume. F5 SM has the highest stored energy while C5 and G5 are close to each other. Although the P5 SM has the smallest volume, it requires more passive elements than the other modules, especially F5. So, there is a trade-off between the number of elements and the total SM size.
- P5 SM has two primary and secondary side capacitors (C_p and C_s) having almost zero average voltage, see Fig. 9 and Table III. Consequently, these capacitors can be very small and cheap when compared with the C5 and G5 SMs.
- The voltages, currents and switching pattern of the semiconductor devices are the same for all SMs. For this reason, the switching and conducting losses are the same for each Mode of operation.
- The C5-based system has the best efficiency when the input voltage is moderate, see Fig. 13 and Fig. 20. However, when the input voltage increases F5-based system offers the best efficiency. Generally, all candidates have an optimum point versus the input voltage and SMs number. After this point, the efficiency of the system decreases.
- The total power losses increase significantly when the input dc voltage and the SMs number are low. This occurs because the devices and the inductors' currents become very high.
- The best suitable converter depends on the input PV arrays voltages as well as the number of modules. It can be sensed from the previous analyses and results that C5 is the best choice when the input voltage is low while F5 is better when the input voltage increases to very high limits.
- Although the theoretical analysis illustrates that F5-based system has the best efficiency at higher input voltages, it necessitates for a bigger transformer core with more core losses in practice. However, these transformer core losses are low when compared with the semiconductor and inductor losses.
- Because Mode 1 has balanced voltage and current waveforms, it is easier to be controlled with the classical dqo frame controllers [19].

VIII. Conclusion

This paper presents a new modular energy conversion system for medium-voltage PV applications. The proposed system has two different modes of operations. Different four candidates, able to be isolated with high-frequency transformer cores, were proposed and analyzed in terms of voltage/current ripples, sizes, volumes, and power losses. The proposed system offers the required modularity and enables cost and size reduction. The proposed system is able to operate under partial shading of some or all of the input PV arrays by changing the SMs duty ratios if the controller has the information about the PV arrays characteristics in advance. The controller design and the appropriate MPPT system are yet to be considered in further future publications.

IX. References

[1] (2017, Oct). Snapshot of Global PV Markets 2016, IEA-PVPS. [Online] http://www.iea-pvps.org/fileadmin/dam/public/report/statistics/IEA-PVPS_-_A_Snapshot_of_Global_PV_-_1992-2016__1_.pdf

[2] (2016). Solar Market Report and Membership Directory, Solar Power Europe [Online] https://zerohomebills.com/wp-content/uploads/2016/04/2016-Solar-Market-Report.pdf

[3] H. Akagi, "Classification, terminology, and application of the modular multilevel cascaded converter (MMCC)," *IEEE Trans. Power Electron*., vol. 26, no. 11, pp. 3119–3130, Nov. 2011.

[4] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana, "Circuit topologies, modeling, control schemes, and applications of modular multilevel converters," *IEEE Trans. Power Electron*., vol. 30, no. 1, pp. 4–17, Jan. 2015.

[5] M. R. Islam, Y. G. Guo, and J. G. Zhu, "A high-frequency link multilevel cascaded medium-voltage converter for direct grid integration of renewable energy systems," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4167–4182, Aug. 2014.

[6] G. P. Adam, I. A. Gowaid, S. J. Finney, D. Holliday and B. W. Williams, "Review of dc–dc converters for multi-terminal HVDC transmission networks," *IET Power Electronics*, vol. 9, no. 2, pp. 281-296, 2 10 2016

[7] B. Xiao, L. Hang, J. Mei, C. Riley, L. M. Tolbert, and B. Ozpineci, "Modular cascaded H-bridge multilevel PV inverter with distributed MPPT for grid-connected applications," *IEEE Trans. Ind. Electron*., vol. 51, no. 2,pp. 1722–1731, Mar./Apr. 2015.

[8] F. F. Edwin, W. Xiao, and V. Khadkikar, "Dynamic modeling and control of interleaved flyback module-integrated converter for PV power applications," *IEEE Trans. Ind. Electron*., vol. 61, no. 3, pp. 1377–88, Mar. 2014

[9] A. Darwish, A. M. Massoud, D. Holliday, S. Ahmed and B. W. Williams, "Single-Stage three-phase differential-mode buck-boost inverters with continuous input current for PV Applications," in IEEE Transactions on Power Electronics, vol. 31, no. 12, pp. 8218-8236, Dec. 2016.

[10] A. Darwish Badawy, " Current source dc-dc and dc-ac converters with continuous energy flow," Degree of Doctor of Philosophy, Department of Electronics and Electrical Engineering, University of Strathclyde, Glasgow, 2015.

[11] B. W. Williams, "Generation and analysis of canonical switching Cell DC to-DC converters," *IEEE Trans. Ind. Electron*., vol. 61, no. 1, pp. 329–346, Jan. 2013.

[12] J. Knight, S. Shirsavar, and W. Holderbaum, "An improved reliability Cuk based solar inverter with sliding mode con-trol," *IEEE Trans. Power Electron*., vol. 21, no. 4, pp. 1107–1115, Jul. 2006.

[13] A. Darwish, A. Elserougi, A. Abdel-Khalik, S. Ahmed, A. Massoud, D. Holliday, and B. Williams, "A single-stage three-phase DC/AC inverter based on Cuk converter for PV application," in GCC Conference and Exhibition (GCC), 2013 7th IEEE, 2013, pp. 384–389

[14] H. Akagi, "Classification, terminology, and application of the modular multilevel cascade converter (MMCC)," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3119–3130, Nov. 2011.

[15] H. Liu, K. Ma, and F. Blaabjerg, "Device loading and efficiency of modular multilevel converter under various modulation strategies," *Proc. 7th IEEE Int. Symp. Power Electron. Distrib. Gener. Syst.*, Jun. 2016, pp. 1–7.

[16] A. H. El Khateb, N. A. Rahim, J. Selvaraj and B. W. Williams, "DC-to-DC converter with low input current ripple for maximum photovoltaic power extraction," *IEEE Trans. Ind. Electron*, vol. 62, no. 4, pp. 2246-2256, April 2015.

[17] S. Rodrigues, A. Papadopoulos, E. Kontos, T. Todorcevic, and P. Bauer, "Steady-state loss model of half-bridge modular multilevel converters," *IEEE Trans. Ind. Appl*., vol. 52, no. 3, pp. 2415–2425, May/Jun. 2016.

[18] B. Hafez, H. S. Krishnamoorthy, P. Enjeti, and S. Ahmed, "Medium voltage AC collection grid for large scale photovoltaic plants based on medium frequency transformers," *Proc. IEEE Energy Convers. Congr. Expo*. 2014, pp. 5304–5311.

[19] Y. Wang, A. Darwish, D. Holliday, and B. Williams, "Plug-in repetitive control strategy for high-order, wide output range, impedance source converters," IEEE Trans. Power Electron., vol. 32, no. 8, pp. 6510–6522, Aug. 2017

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