Comparative Analysis of Active Capacitor Voltage Balancing Method for Flying Capacitor Multilevel Converters

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***Abstract*— This paper presents a comparative analysis of an active capacitor voltage balancing method for Flying Capacitor Multilevel (FCM) converters, focusing on the effectiveness of various strategies in maintaining optimal capacitor voltages. We examine both natural balancing methods and active control methods, evaluating their performance under a variety of operational scenarios. An active balancing method based on an Overall Priority Index (OPI) is utilized, which optimizes the selection of switching states to minimize voltage deviations from nominal values. An analysis of the proposed method is conducted using simulations on a five-level FCM and a six-level converter, to compare its performance with that of existing methods. OPI-based methods reduce capacitor voltage ripple, as demonstrated in the results. Various experimental results are presented to demonstrate the stability of the proposed method under various conditions of load and modulation index.**

***Keywords* - Capacitor voltage balancing, voltage control, carrier-based pulse width modulation, flying capacitor converter, multilevel converter**

I. Introduction

The growing industrial demand for high-power applications has driven the power electronics research community to develop efficient and cost-effective solutions. Multilevel converters have emerged as a key technology, leveraging mature medium-voltage and current devices to address the challenges of high-power applications such as motor drives, grid-connected converters, reactive power compensation, and wind energy conversion systems [1]-[3]. Among the well-established multilevel converter topologies are the Neutral Point Clamped (NPC) converter and its advanced derivatives [4]-[5], the Flying Capacitor Multicell (FCM) converter [6], the Cascaded H-Bridge (CHB) converter [7], and the Modular Multilevel Converter (MMC) [8].

Flying capacitors and their voltage balancing present significant challenges in the application of FCM converters, limiting their broader use. To address these challenges, researchers have introduced new flying capacitor-based (FC-based) topologies that reduce the number of flying capacitors required while incorporating effective voltage balancing strategies [9]-[10]. In FC-based multilevel converters, maintaining proper voltage levels across the capacitors is crucial for the accurate synthesis of the desired output voltage levels. Various methods for capacitor voltage balancing have been proposed in the literature, which can generally be categorized into two primary strategies. The first strategy leverages the natural balancing properties of FCM converters combined with an appropriate open-loop control approach [11]-[12]. Carrier-based schemes, such as phase-shifted carrier PWM and its modifications, naturally balance capacitor voltages under ideal conditions, offering advantages like equal distribution of switching losses and a high equivalent switching frequency. However, despite their straightforward implementation and the absence of voltage and current sensors, these natural balancing schemes may not perform reliably in practical applications [13].

The second strategy actively controls flying capacitor voltages to maintain them at desired levels [14]-[18]. For example, in [14], a PI controller is used to correct voltage deviations by adjusting the modulating signals, ensuring optimal capacitor voltage balancing. Another approach, termed multilevel hysteresis current regulation, is proposed in [15], where the output voltage level is determined by the current error processed through hysteresis comparators. An active voltage balancing method has been applied to a four-level Nested Neutral Point Clamped (NNPC) converter using a cost function scheme [16]. To simplify the computational demands of this method and to exploit redundant switching states, a straightforward single-phase modulator was introduced in [17], suitable for each phase of a three-phase four-level NNPC converter. A similar technique was developed for a five-level NNPC, focusing on controlling and balancing flying capacitor voltages [18]. However, in this approach, only two of the three flying capacitors are prioritized for balancing. An efficient voltage balancing technique for the five-level NNPC converter was later introduced in [19], where an index based on the deviation of capacitor voltages from their nominal values was used. This method optimizes the selection of switching states, leading to significantly improved capacitor voltage balancing performance compared to the method presented in [18].

In this paper, an active capacitor voltage balancing method is applied to FC-based multilevel converters. This method uses an optimized switching state selection process to maintain voltage balancing over a wide range of operating conditions. By using a priority-based approach, the method evaluates and prioritizes switching states that contribute to optimal capacitor voltage regulation. Comparison studies over a wide range of modulation indexes and power factors are provided. Detailed simulations and experimental validations demonstrate the effectiveness of the proposed method, resulting in significant improvements in voltage balancing and the reduction of capacitor voltage ripples.

II. Active Capacitor Voltage Balancing Based on Overall Priority Index

Fig. 1 shows the structure of a phase (or leg) in an FCM converter. Each phase consists of M-1 dc capacitors, known as flying capacitors, and 2×M semiconductor switches, such as insulated gate bipolar transistors (IGBTs), which are controlled in a complementary fashion. The voltages of flying capacitors are regulated in ascending order from V_{C1} to $V_{C(M-1)}$. In a symmetrical FCM converter, the nominal voltage of the flying capacitor C_k is equal to kV_{dc}/M, where V_{dc} is the voltage of the dc link, resulting in an output voltage waveform with a number of M+1 equally spaced levels [20]. The output voltage is constructed by adding or subtracting flying capacitor voltages. The output voltage has a staircase waveform with step sizes corresponding to the voltage difference between two adjacent capacitors. In this structure, the blocking voltage of each switch is equal to V_{dc}/M.

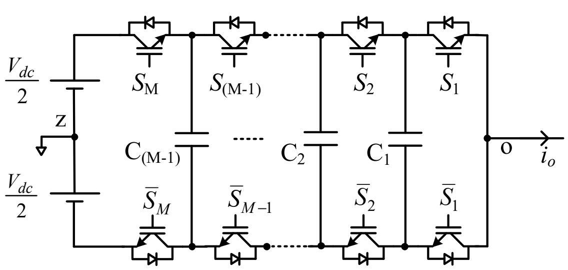


Fig. 1. M-cell FCM topology.

In an FCM converter, there are some redundant switching states for generating specific voltage levels. Each redundant state provides a different charging/discharging state for the flying capacitors and have different effect on the capacitor voltages. This feature is exploited to achieve the voltage balancing of flying capacitors. However, the impacts of redundant switching states can be contradicting each other under some capacitor voltage ripples. In this regard, different priorities can be considered for capacitor voltage balancing.

In the proposed method, to derive an efficient priority index for capacitor voltage balancing, the switching states and their effects are generally analyzed. Then, a priority is defined to optimize the state selected for capacitor voltage balancing. In the proposed method, the flying capacitors with higher voltage ripples are balanced with higher priority. Priority Index (*PI*) hereinafter, is defined for flying capacitor C_k as

$$PI_k = \begin{cases} \Delta V_{Ck} \times \mathrm{sgn}(i_o) & \text{if } C_k \text{ charged with } i_o > 0 \\ -\Delta V_{Ck} \times \mathrm{sgn}(i_o) & \text{if } C_k \text{ discharged with } i_o > 0 \\ 0 & \text{No change} \end{cases} \tag{1}$$

where $sgn(.)$ is the sign function. If the PI_k is positive for a specific switching state, this means that its selection will deteriorate V_{Ck} from its nominal value, which is not desirable. On the other hand, if a switching state results in a negative PI_k, this means that its selection helps in regulating V_{Ck} to its nominal value. The zero value of the PI_k means that a switching state has no effect on capacitor voltage.

The switching state corresponding to the lowest *OPI* is selected. As the *OPI* is the sum of the *PI*s of all phase capacitors, its minimization would result in the overall minimum deviation of capacitor voltages from their nominal values. The flowchart of the proposed method is presented in Fig. 2.

$$OPI = \sum_{k=1}^{M} PI_k \tag{2}$$

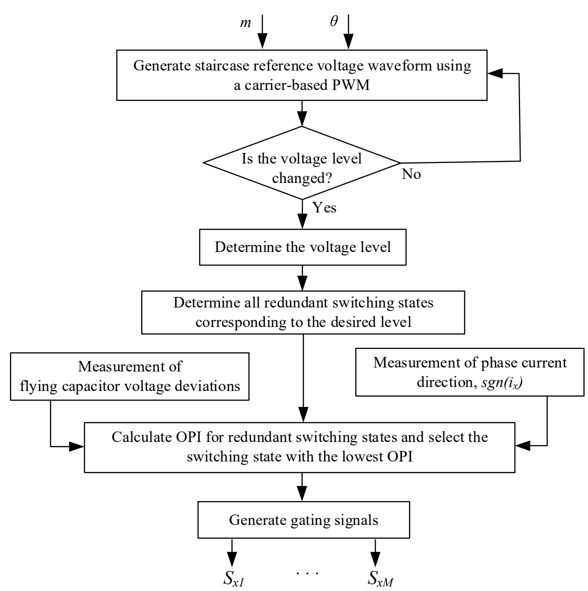


Fig. 2. Flowchart of the capacitor voltage balancing method.

III. Analysis of the Proposed Method on a Five-Level FCM Converter

In this section, the proposed voltage balancing method is applied to a symmetric five-level FCM converter as shown in Fig. 3. Table I shows different voltage levels along with corresponding switching states in a five-level FCM converter. As can be seen, five output levels can be achieved from sixteen distinct switching states. Voltage levels 4 and 0 (corresponding to V_{oZ} equal to $V_{dc}/2$ and $-V_{dc}/2$ respectively) have unique switching states. However, there are four redundant switching states to generate voltage levels 3 and 1 (corresponding to V_{oZ} equal to $V_{dc}/4$ and $-V_{dc}/4$ respectively), and six redundant switching states to generate voltage level 0 corresponding to V_{oZ}=0. The expression for the *OPI* for each switching state is also shown in Table I. As stated in the previous section, when the voltage level is determined, and phase current direction and capacitor voltage deviation from its nominal value is measured, the *OPI* associated with redundant switching states (if any) is calculated. Consequently, the switching state with the lowest *OPI* is selected for that level.

As an example, consider the instant where the determined phase voltage level is 1 (i.e. v_{oZ} equal to $-V_{dc}/4$) by the modulator and phase current is positive. Now assume that the capacitors' voltage deviations are measured as

$$\Delta V_{C1} = -0.01\,pu$$
$$\Delta V_{C2} = +0.03\,pu$$
$$\Delta V_{C3} = -0.03\,pu$$

Based on Table I, four switching states can be chosen to achieve the desired voltage level. The *OPI*s corresponding to the switching states 2, 3, 4, and 5 are equal to 0.01, -0.04, 0.06, and -0.03, respectively. In this case, the proposed algorithm selects the switching state 3 which has the lowest *OPI* to generate the desired output voltage level. With this selection, the voltage deviation of capacitors C_1 and C_2 decreases while the voltage deviation of capacitor C_3 does not change. Alternatively, if the switching state 5 is selected, the voltage deviation of capacitor C_3 decreases, but the voltage deviation of capacitors C_1 and C_2 remains unchanged. It will be seen that the overall voltage ripple of all capacitors is minimized if the switching state selected by the proposed algorithm is selected.

The proposed procedure can be fundamentally applied to any FC-based topology and a table similar to Table I can be obtained. In practice, the *OPI* calculation must be performed for each converter phase independently to regulate the flying capacitors voltages. As can be seen, this procedure is generalized and independent of the converter topology and very simple to implement in a digital controller platform.

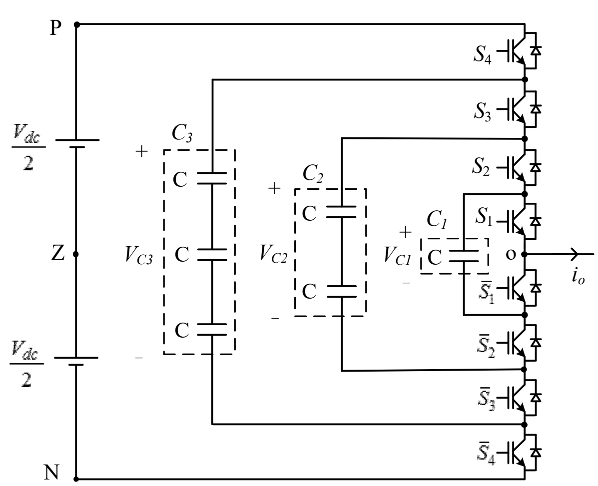


Fig. 3. A phase (leg) of a symmetrical five-level FCM topology.

Table I: Switching states and their impact on flying capacitors along with OPI calculation for a five-level FCM converter

SS No.	SS of switches ($S_4 S_3 S_2 S_1$)	v_{oZ}	Level	Impact on FCs C_1	C_2	C_3	*OPI*
16	1 1 1 1	$V_{dc}/2$	4	N	N	N	0
15	1 1 1 0	$V_{dc}/4$	3	C+	N	N	$\Delta V_{C1}\times\mathrm{sgn}(i_o)$
14	1 1 0 1			D+	C+	N	$(-\Delta V_{C1}+\Delta V_{C2})\times\mathrm{sgn}(i_o)$
13	1 0 1 1			N	D+	C+	$(-\Delta V_{C2}+\Delta V_{C3})\times\mathrm{sgn}(i_o)$
12	0 1 1 1			N	N	D+	$-\Delta V_{C3}\times\mathrm{sgn}(i_o)$
11	0 0 1 1	0	2	N	D+	N	$-\Delta V_{C2}\times\mathrm{sgn}(i_o)$
10	0 1 1 0			C+	N	D+	$(\Delta V_{C1}-\Delta V_{C3})\times\mathrm{sgn}(i_o)$
9	0 1 0 1			D+	C+	D+	$(-\Delta V_{C1}+\Delta V_{C2}-\Delta V_{C3})\times\mathrm{sgn}(i_o)$
8	1 0 1 0			C+	D+	C+	$(\Delta V_{C1}-\Delta V_{C2}+\Delta V_{C3})\times\mathrm{sgn}(i_o)$
7	1 0 0 1			D+	N	C+	$(-\Delta V_{C1}+\Delta V_{C3})\times\mathrm{sgn}(i_o)$
6	1 1 0 0			N	C+	N	$\Delta V_{C2}\times\mathrm{sgn}(i_o)$
5	1 0 0 0	$-V_{dc}/4$	1	N	N	C+	$\Delta V_{C3}\times\mathrm{sgn}(i_o)$
4	0 1 0 0			N	C+	D+	$(\Delta V_{C2}-\Delta V_{C3})\times\mathrm{sgn}(i_o)$
3	0 0 1 0			C+	D+	N	$(\Delta V_{C1}-\Delta V_{C2})\times\mathrm{sgn}(i_o)$
2	0 0 0 1			D+	N	N	$-\Delta V_{C1}\times\mathrm{sgn}(i_o)$
1	0 0 0 0	$-V_{dc}/2$	0	N	N	N	0

C+: Charging with (i_o>0), D+: Discharging with (i_o>0), N: No Change

IV. COMPARISON

To evaluate the merits of the proposed voltage balancing method, a comparison is made between the proposed method and other similar methods presented in the literature. The simulations were carried out using the PSIM software package. All simulation results are based on the parameters given in Table II.

Table II: Simulated System Parameters

System Parameter	Value
DC Source Voltage (V_{dc})	1200 V
Rated Power	50 kVA
Capacitance of Flying Capacitors (C_1, C_2, and C_3)	1.5 mF, 1 mF, and 0.5 mF
Carrier Frequency	2.5 kHz
Fundamental Output Frequency (f_o)	50 Hz
Modulation Index (m)	0.95
Load Power Factor	0.8

For comparison, the five-level NNPC converter and its capacitor voltage balancing which is presented in [18] is considered. Then, the proposed method is also applied to the

the five-level NNPC converter. The *OPI* is simply determined for redundant switching states at the desired voltage level, and then the switching state with the lowest *OPI* is selected. For comparison, various simulations of the NNPC converter have been conducted using both methods.

Fig. 4 shows the flying capacitor voltage waveforms when two methods are employed using the simulation parameter presented in Table II. As can be observed, the capacitor voltage ripple is lower in the proposed method than the one presented in [18]. To evaluate the proposed method in comparison with the method in [18], simulations have been carried out at various operating points. First, at a fixed load power factor, the simulations have been carried out for the full operating range of the modulation index. The capacitor voltage ripples resulting from the two methods for a power factor 0.9 are shown in Fig. 5. The capacitor voltage ripples are significantly reduced by applying the proposed method. To study the effect of two methods on switching frequencies, the average switching frequency is defined as follow:

$$f_{sw,av} = \frac{f_{sw,S1} + f_{sw,S2} + f_{sw,S3} + f_{sw,S4}}{4} \tag{3}$$

where $f_{sw,Sk}$ is switching frequency of switch S_k (k=1, 2, 3, 4). Fig. 6 shows the average switching frequency resulted from the two methods at various modulation indexes. As can be seen, the switching frequency is more and less the same at high modulation indexes. At lower modulation, the proposed method has a little higher switching frequency at the gain of significantly reduced capacitor voltage ripples.

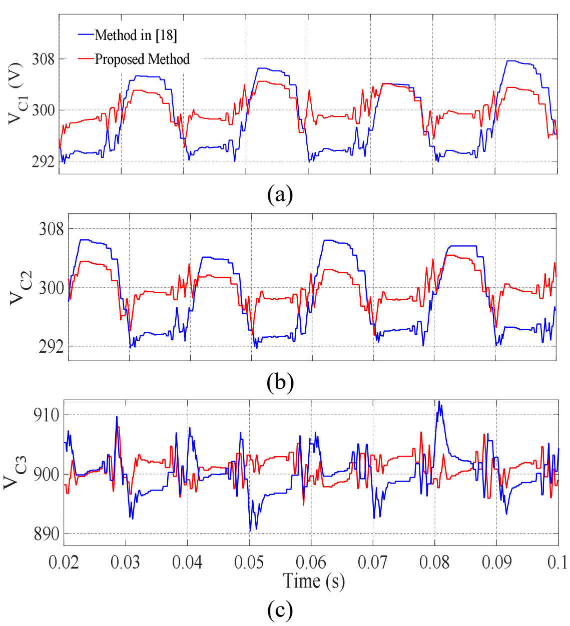


Fig. 4. Flying capacitors' voltage waveforms when using the proposed method and the method presented in [18], (a) V_{C1}, (b) V_{C2} and (c) V_{C3} voltages.

Second, the modulation index is set to a fixed value of M=0.95 and the load power factor is changed from 0 to 1. The simulation results are shown in Fig. 7. As can be seen, the proposed method results in lower capacitor voltage ripples. The average switching frequencies resulted from the two methods at various power factors are shown in Fig. 8. The switching frequency of the two methods is changed a bit with power factor variations.

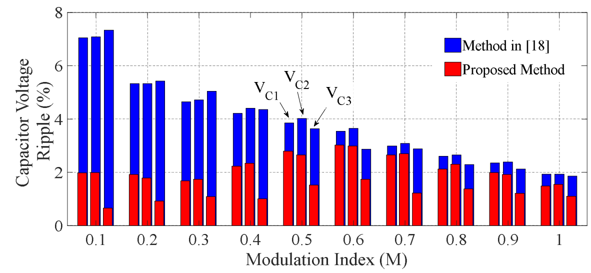


Fig. 5. Flying capacitor voltage ripples of the proposed method and method in [18] at various modulation indexes.

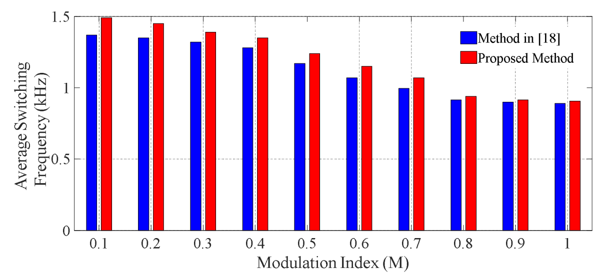


Fig. 6. Average switching frequency of the proposed method and method in [18] at various modulation indexes.

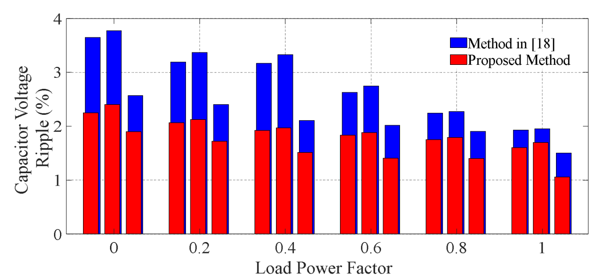


Fig. 7. Flying capacitor voltage ripples of the proposed method and method in [18] at various load power factors.

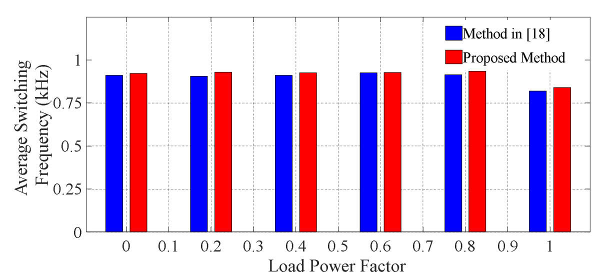


Fig. 8. Average switching frequency of the proposed method and method in [18] at various load power factors.

V. Experimental Results

To demonstrate the practicality of the presented capacitor voltage balancing method, a scaled-down prototype of the five-level FCM topology was implemented. A DSP-based digital control platform was used to generate PWM signals and perform capacitor voltage control. The amplitude of the dc voltage is 120V as this was just a proof-of-concept verification. Other parameters of the experimental system are given in Table III.

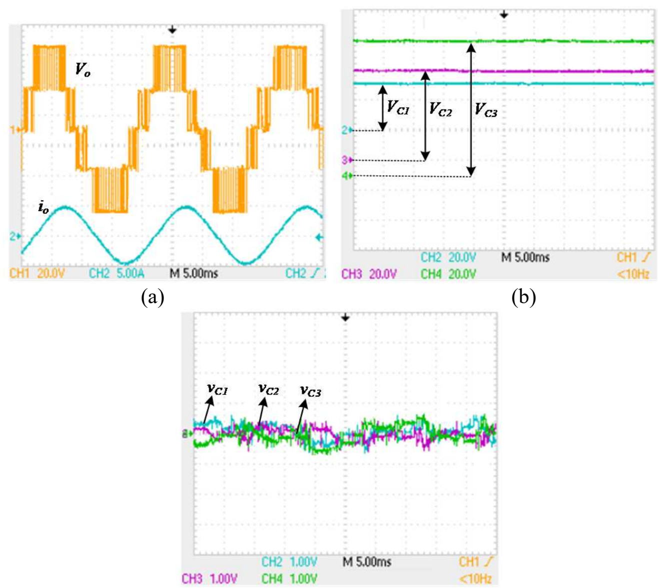
Fig. 9 shows the measured output voltage, line current and flying capacitor voltages waveforms. The modulation index is set to 0.95. As illustrated in Fig. 9(b), the proposed active voltage balancing method is able to regulate the flying capacitor voltages to the reference values (i.e. 30V, 60V, and 90V). In order to observe the capacitors' voltage ripples, the AC coupling mode of the oscilloscope at a more sensitive time/div setting is used. Fig. 9(c) shows the AC component of the flying capacitor voltages. The peak-to-peak voltage deviations of flying capacitors are around 1V.

To show the modulation index variation effect, the modulation index is decreased from 0.95 to 0.7 and decreased from 0.7 to 0.5. The experimentally measured synthesized output voltage, load current, and flying capacitor voltages are presented in Fig. 10. The modulation index is set to 0.95, 0.7, and 0.45 in the first cycle of the output voltage, the next two output cycles, and the last two output cycles, respectively. According to the experimental results for the 5-level FCM converter, the proposed method is able to regulate the flying capacitors. The voltage ripples of the flying capacitors are decreased at lower modulation indices as shown in Fig. 10(c). The peak-to-peak voltage deviations of flying capacitors at modulation indices 0.95, 0.7, and 0.45 are around 1V, 0.8V and 0.6V, respectively.

In order to show the performance of the proposed capacitor voltage balancing during transient conditions, a step change from half-load to full-load (M=0.95) is applied, as seen in Fig. 11. As shown in Fig. 11(b), the voltages of the flying capacitors are maintained at the nominal values. The voltage ripples of the flying capacitors are increased at full-load as shown in Fig. 11(c). The peak-to-peak voltage deviations of flying capacitors at half-load to full-load changes from 0.7V to 1.5V.

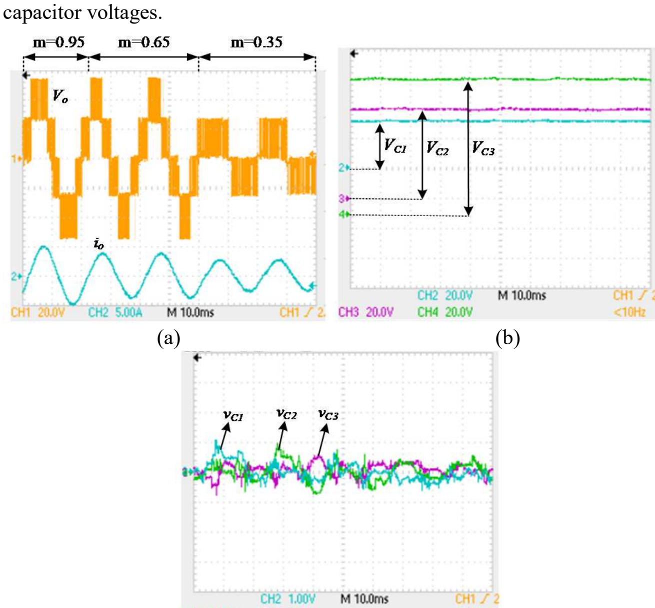
Table III: Experimental System Parameters

System Parameter	Value
Switching devices	IGBT with antiparallel diode BUP 400D
Current and voltage ratings of IGBTs	22 A, 600 V
DC sources voltage (V_{dc})	120 V
Digital signal processor	TMS320F28335
Capacitance of flying capacitors	1 mF
Sampling frequency	2.5 kHz
Reference voltage frequency (f_o)	50 Hz
Load resistance and inductance (R, L)	12 Ω, 30 mH



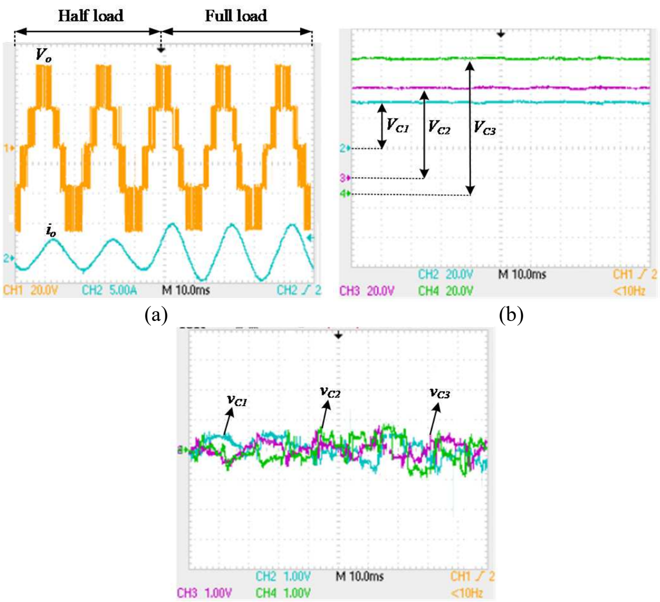
(a) (b) (c)

Fig. 9. Experimental results at m=0.95, (a) phase voltage v_{aN} and load current i_a, (b) flying capacitor voltages V_{C1}, V_{C2} and V_{C3}, (c) AC components of flying capacitor voltages.



(a) (b) (c)

Fig. 10. Experimental results with modulation index changes, (a) phase voltage v_{aN} and load current i_a, (b) flying capacitor voltages V_{C1}, V_{C2} and V_{C3}, (c) AC components of flying capacitor voltages.



(a) (b)

(c)

Fig. 11. Experimental results at load change, (a) output voltages v_{aN} and load current i_a, (b) flying capacitor voltages V_{C1a}, V_{C2a} and V_{C3a}, (c) AC components of flying capacitor voltages.

VI. Conclusion

This paper presents an optimized active capacitor voltage balancing method to control flying capacitor voltages in multilevel converters, enhancing performance while minimizing capacitor voltage ripples. The effectiveness of the proposed technique is verified through simulation results of a five-level FCM converter and a six-level flying capacitor-based converter. The proposed method effectively balances flying capacitor voltages across a wide range of operating conditions, ensuring stable and reliable converter operation. A comprehensive comparison is made to illustrate the superiority of the active voltage control method. Through comprehensive experimental validation, the method demonstrates its ability to maintain the voltages of the flying capacitors at desired level.

VII. References

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