Optimized Modular Multilevel Converter Topology using Si/SiC Hybrid Half-bridge Submodule

1st Abdulkarim Athwer
Electrical engineering department
Lancaster University
Lancaster, UK
a.athwer@lancaster.ac.uk

2nd Ahmed Darwish
Electrical engineering department
Lancaster University
Lancaster, UK
a.badawy@lancaster.ac.uk

3rd Xiandong Ma
Electrical engineering department
Lancaster University
Lancaster, UK
xiandong.ma@lancaster.ac.uk

***Abstract*—**The Modular Multilevel Converter (MMC) has emerged as a promising solution for medium and high-voltage power conversion applications. This paper proposes a modified configuration of the MMC model based on a conventional half-bridge submodule (HBSM) utilizing a Si IGBT and SiC MOSFET hybrid approach. The combination of Si IGBTs and SiC MOSFETs offers a great advantage of employing the low cost and high voltage capability of Si IGBTs along with the faster switching speeds and low power loss of SiC MOSFETs. A hybrid HBSM places the Si IGBTs on the upper side and SiC MOSFETs on the lower side in order to reduce the switching and conduction power losses. This arrangement of the hybrid system for MMC cells enables improvements in the converter's performance and efficiency. A nine-level voltage of MMC (9LMMC) model based on IGBT/SiC hybrid HBSMs is simulated using the PLECS® Standalone tool to verify the effectiveness of the modified converter topology.

Keywords—MMC topology, Si/SiC hybrid MMC-HBSM model, power losses and cost comparison

I. INTRODUCTION

Modular multilevel converter (MMC) has gained a massive attention since it was proposed in 2003 by Marquardt [1]. Recently, MMC model become the most popular voltage source converter (VSC) topology for medium and high voltage applications, due to its several features such as modularity, scalability, redundancy, and high quality of voltages and currents waveforms [2]. Conventional MMC topology usually uses half bridge (HB) or full-bridge (FB) submodules (SMs). These submodules are made up of a series-connected insulated-gate bipolar transistors (IGBTs) or metal–oxide silicon field-effect transistors (MOSFETs) based on silicon (Si) material [3].

Since the invention of the semiconductor transistor, the Si MOSFETs and IGBTs have been widely used in various power applications, due to their acceptable performance, wide availability with several voltage levels reached to 6.5 kV, and low cost. However, it appears that the performance of Si based devices has reached maturity and several limitations arise when considering the increasing energy demands. Among these limitations are high switching and conduction power losses, voltage stress on the devices which causing high dv/dt, the ability to withstand only a low switching frequency, and a maximum temperature limit of 150°C for most Si device junctions. These restrictions are considered a major concern in power conversion systems, especially in high-power applications. To address these issues, the integration of high-performance wide bandgap (WBG) semiconductor power devices, such as silicon carbide (SiC) and gallium nitride (GaN) based devices expected to offer an ideal solution for further development and improvement of the MMC topology [4], [5].

Alongside the global development of power semiconductor devices, the market for SiC and GaN based devices has been growing rapidly [6]. SiC and GaN devices offer numerous advantages over traditional Si based devices, as they can withstand high frequencies and temperatures to reach around 300 °C while significantly reducing power losses [7]. Currently, several companies are producing commercially available MOSFETs, power SiC Schottky diodes, and modules can be used for many power applications. For instance, companies like Wolf-speed® and Infineon® offer SiC MOSFETs with voltage ratings ranging from 650 V to 1.7 kV and current ratings from 5 A to 125 A [8], [9]. Furthermore, GaN System® offers a variety of GaN FET transistors with a voltage rating of 650 V and a current rating of up to 150 A. Transphorm® also provides GaN FETs in TO-247 packages with voltage levels up to 900 V and a current rating of up to 34 A [10]. Recently, Transphorm® announced its plans to demonstrate a new GaN FET device with a voltage rating of 1.2 kV, which could be more suitable for medium and high voltage applications [11].

The utilization of SiC and GaN power devices in medium and high-power converter applications appears to offer new opportunities for MMC converter modelling, aiming to reduce switching and conduction losses, as well as improving the MMC performance [5]. However, the high cost and voltage level limitations of GaN and SiC based devices are the main obstacles to completely replacing Si IGBTs with these types of devices in certain power applications [12]. Therefore, a hybrid system technology based on Si IGBTs/Gan or Si IGBTs/SiC has gained more interest for many power applications [13]. Recently, many research efforts have been conducted to propose new MMC models based on the Si/SiC hybrid system [3], [4], [14], [15], [16]. These models have been investigated in terms of MMC modelling schemes, the emerging SiC in MMC-SM structure, modulation strategies, and control systems for voltage balancing and circulating current. The hybrid MMC topology has resulted in several benefits including reduced power losses, improved performance of the converter model and cost savings [5].

In this paper, hybrid MMC topology-based Si IGBT/SiC MOSFET submodule is proposed for wind energy conversion system (WECS). The hybrid MMC-HBSM model aims to combine the advantages of both Si IGBT and SiC MOSFET to address the aforementioned problems of the MMC model based on pure Si IGBT devices. The paper has been organized as follows: Section II presents the MMC topology and its principle of operation including the proposed model. Section III presents a Si IGBT/SiC MOSFET hybrid MMC-HBSM simulation results. In section IV, power loss and cost comparison between the Si and SiC semiconductor devices, as well as the total power loss of the HBSM cell are presented. The final conclusion is presented in section V.

II. MMC Topology And Its Principle Of Operation

The basic circuit configuration of a three-phase MMC concept consists of six arms. Each phase has two arms upper arm (up_{arm}) and lower arm (lw_{arm}) are connected via two buffer inductors (L_{arm}). The inductors are very important components for handling the voltage difference between the upper and lower arms of the phase converter, they are also used to limit the current and maintain the system during faults and short-circuits. In addition, each phase arm is composed of a number (N) of nominally identical half-bridge or full-bridge sub-modules that allow for N+1 output voltage levels at the phase output voltage terminal [17].

The SM structure is a fundamental part of the MMC topology used to obtain the required output voltage. Semiconductor devices such as Si IGBTs and MOSFETs power switches play an important role in the design of SM systems, controlling the flow of voltage and current and converting them into a suitable form for user loads. Over the past 20 years, several SM circuits have been developed and successfully implemented in power converters. Among these, the HB-SMs topology is recognized as the most popular cell structure for MMC HVDC applications. However, the power loss of semiconductor devices remains a concern in the design of MMC topology, and many efforts are being conducted to resolve this problem [18].

A. *The proposed MMC model - Utilizing a Si IGBT and SiC MOSFET hybrid SM*

The proposed hybrid MMC model in this research work utilizes the conventional HBSM structure due to its simple design and low cost. Basically, the HBSM consists of two power semiconductor switches (S_1, S_2) connected with a single capacitor SM_C, operating in a complementary manner to generate two voltage levels at the output terminal (either *0* or V_C). The HBSM standard configuration has lower power loss compared to other topologies. However, it does not support DC fault, which can be achieved with the FBSM implementation [14][2].

In the proposed MMC configuration, a Si IGBT and SiC MOSFET hybrid HBSMs are used in the upper and lower arms. Where the Si IGBT is placed in the upper side of the HB cell, while the SiC MOSFET is placed in the lower side of the cell as shown in figure 1. This configuration combines the features of Si/SiC devices and allows for the benefits of high voltage and current handling capability, reducing the total power loss for each HBSM, the ability to operate at high switching frequency, reasonable cost, and improved overall converter efficiency.

B. *MMC control system*

Several MMC control techniques have been used for control of voltage and current flow connected with AC grid systems to ensure the proper operation of the converter system. In general, the MMC control system can be classified into two main categories as following [16].

First. Voltage control system: The main objective of the voltage control is to ensure the voltage balance of the NSM floating DC capacitors. This system can be further classified into two categories:

- Averaging control: This type of control is utilized to maintain the arm voltages at a desired average level, typically referred to as Vdc.
- Balancing control: The main aim of this control is to restrict the charging or discharging of the SM capacitors beyond a predetermined threshold VSM.

Second. AC power control system: The objective of this control is to regulate the flow of the power (AC voltage and current) between the MMC model and the main grid in both directions.

The control system of a three phase MMC model connected to the grid involves various control techniques and components including phase-looked loop (PLL), current control, voltage control, and pulse width modulation (PWM) technique. Figure 2 shows the closed loop control system of MMC model connected with the grid [16], [19].

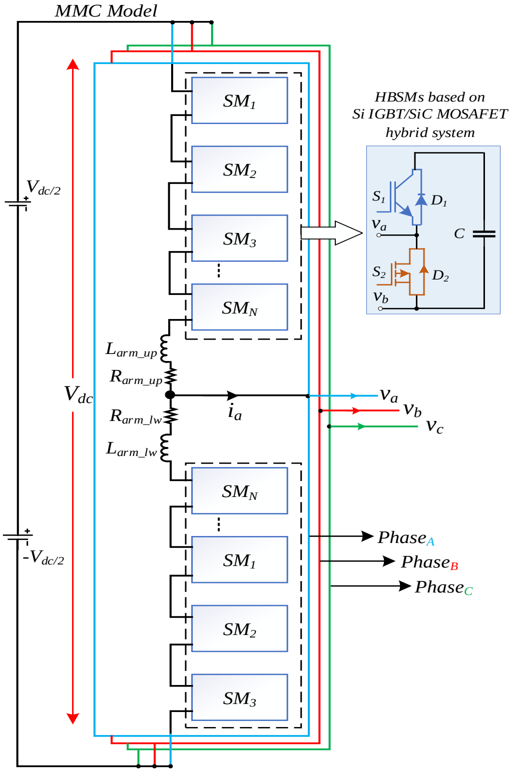

Fig1. Three-phase MMC topology based on the proposed Si/SiC hybrid HBSMs.

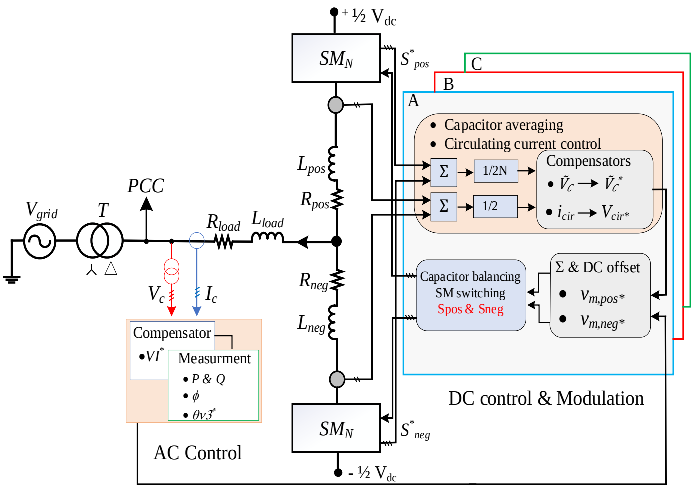

Fig 2. A control scheme of MMC model [17].

C. MMC Theoretical Voltages and Currents

By applying Kirchhoff's law, the steady state and internal dynamics of the MMC model can be explained where the voltage and current equations can be obtained. The converter terminal voltage of phase A can be expressed by equations (1). Where the positive and negative voltages relationship in phase AC are related to the DC and terminal voltages, which given by the equations (2) and (3), respectively. Phase A currents, in the positive and negative arms due to the DC and AC currents can be obtained by equations (4) and (5), while the same principle can be applied for both phases B and C [17].

$$v_{Ca} = \tilde{V}_{C1}\, cos(\omega_t) \tag{1}$$

$$v_{pos.a} = \frac{V_{dc}}{2} - v_{Ca} - v_{cir.\ a} \tag{2}$$

$$v_{neg.a} = \frac{V_{dc}}{2} + v_{Ca} - v_{cir.\ a} \tag{3}$$

$$i_{pos.a} = \frac{I_{dc}}{3} + \frac{i_{Ca}}{2} + i_{cir.\ a} \tag{4}$$

$$i_{neg.a} = \frac{I_{dc}}{3} - \frac{i_{Ca}}{2} + i_{cir.\ a} \tag{5}$$

Where v_{Ca} is the converter AC instantaneous voltage of phase A and i_{ca} is the instantaneous AC current, $\tilde{V}_{C1}$ is the converter voltage amplitude. $v_{pos.\,a}$ and $v_{neg.\,a}$ are represent the positive and negative arms of the phase voltage. Respectively, $i_{pos.\,a}$ and $i_{neg.\,a}$ are represent the positive and negative arms of the phase current. V_{dc} is the DC voltage supply, I_{dc} is the converter DC current, and $v_{cir.\,a}$ $i_{cir.\,a}$ are the voltage components with their corresponding circulating currents. The phenomenon of the circulating current is typically occurring in each phase leg and can be controlled using a suitable modulation algorithm such as a proportional-resonant controller (PR), which effectively reduces the impact of capacitor voltage fluctuations on the output voltage [20], [21].

Considering the amplitude, phase shift and the difference of the time, the periodic positive and negative voltage and current in each leg can be given by (6) and (7).

$$v_{pos.a} = \frac{V_{dc}}{2} - \tilde{V}_{C1}\, cos(\omega_0 t) \tag{6}$$

$$i_{pos.a} = \frac{I_{dc}}{3} + \frac{\tilde{I}_{C1}}{2}\, cos(\omega_0 t - \emptyset) \tag{7}$$

Similarly, the voltage and current of the negative arm are given by (8) and (9).

$$v_{neg.a} = \frac{V_{dc}}{2} + \tilde{V}_{C1}\, cos(\omega_0 t) \tag{8}$$

$$i_{neg.a} = \frac{I_{dc}}{3} + \frac{\tilde{I}_{C1}}{2}\, cos(\omega_0 t - \emptyset) \tag{9}$$

In the analysis, the phase voltage is taken as the reference with phase angle of zero. Consequently, $\emptyset$ is the power factor angle, which is the difference in phase current and phase voltage (lagging), where $\tilde{I}_{C1}$ represents the amplitude of the converter current. The grid AC voltage can be obtained by equation (10), where m_i is the modulation index [20].

$$\tilde{V}_C = m_i \frac{V_{dc}}{2} \tag{10}$$

The instantaneous power of positive and negative arms can be given by equations (11) and (12). The average power in each phase leg can be obtained by integrating the instantaneous power by applying equations (13) and (14). Where p_{pos} is the instantaneous power, $\bar{P}_{pos.a}$ and $\bar{P}_{neg.a}$ are the positive and negative average power.

$$p_{pos.a}\ (t) = v_{pos.a}\ (t)\ i_{pos.a}\ (t) \tag{11}$$

$$p_{neg.a}\ (t) = v_{neg.a}\ (t)\ i_{neg.a}\ (t) \tag{12}$$

$$\bar{P}_{pos.a}\ \frac{V_{dc} I_{dc}}{6} - \frac{\tilde{V}_{C1}\tilde{I}_{C1}}{4} cos(\emptyset) \tag{13}$$

$$\bar{P}_{neg.a}\ \frac{V_{dc} I_{dc}}{6} - \frac{\tilde{V}_{C1}\tilde{I}_{C1}}{4} cos(\emptyset) \tag{14}$$

The independent control of active and reactive power values using d-q frame transformation can be achieved by the following equations. Where the q-axis voltage component is adjusted to be zero, since PLL is synchronized with the voltage of the power grid.

$$P = \frac{3}{2}\, V_d i_d \tag{16}$$

$$Q = -\frac{3}{2}\, V_d i_d \tag{17}$$

The circulating current in MMC operation system is generated due to the mismatch between the DC voltage and output voltage of various phase arms. It manifests as a negative-sequence (a-c-b) current with a frequency twice that of the fundamental frequency. The presence of the circulating current leads to an increase of root mean square (RMS) arm current value, subsequently causing increased power loss. The expression of inner differential current of three phases can be given by the following equations. Where i_{diff} represents the differential current for three-phase, i_{2f} is the double frequency circulating current, ω is the frequency and φ_0 represents the phase angle [22][23].

$$i_{diff.a} = \frac{i_{dc}}{3} + i_{2f}\ sin(2\omega_0 t - \varphi_0) \tag{18}$$

$$i_{diff.b} = \frac{i_{dc}}{3} + i_{2f}\ \sin\left[2\left(\omega_0 t - \frac{2\pi}{3} + \varphi_0\right)\right] \tag{19}$$

$$i_{diff.c} = \frac{i_{dc}}{3} + i_{2f}\ \sin\left[2\left(\omega_0 t + \frac{2\pi}{3} + \varphi_0\right)\right] \tag{20}$$

Figure 3 shows vector control technique, which has been implemented using an inner loop for current control and an outer loop for voltage and power control. In this setup, the outer loop provides the current reference to the inner current controllers. The current controller enables decoupled control of active and reactive power by regulating the q-d axis current components. Where $V_{g.a}$, $V_{g.b}$, and $V_{g.c}$ represent the three phase grid voltage, while $I_{g.a}$, $I_{g.a}$, and $I_{g.a}$ represent the grid current, i_{ud}^* and i_{uq}^* refer to the direct and quadrature current axes, and the reference voltages used to generate insertion indices for each phase leg are represented by V_{ud}, V_{uq}. V^*_{dc}, P^*, and Q^* represent the DC voltage, active power and reactive power. Respectively, they measured values (V_{dc}, P and Q) obtained using PI controller system [16], [22].

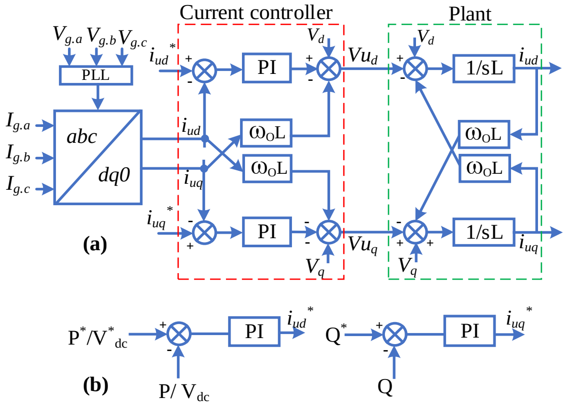

Fig 3. (a) Inner current control, (b) Outer loop power and voltage control [22].

Where the nominal voltage of each SM_C is maintained at the total voltage dc supply over the number of submodules V_{DC}/N.

III. Proposed MMC Simulation Results

A MMC power converter topology was modified and modeled using Si IGBT and SiC MOSFET semiconductor devices for the HBSMs. The simulation of the proposed MMC model was performed using the PLECS software, with the parameters presented in Table I.

TABLE I. Simulation Parameters of 9-level MMC Model

Parameters	Nominal values
Rated output power, P	10 *MW*
DC link voltage, V_{DC}	1.4 *kV*
Number of SMs per arm, N_{SM}	8
Nominal SM capacitor voltage, V_{SM}	175 *V*
SM Capacitor Capacitance, C	1.2 *mF*
Arm Inductance, L_a	6.7 *mH*
Arm Resistance, R_a	0.5 *Ω*
Modulation index, m	0.9
Frequency, f	50 *Hz*
Switching frequency, f_s	7 *kH*
Grid output voltage, V_{out}	630 *V*

A 9-levels output voltage for grid-tied MMC model has been considered for the purpose of voltage and current analysis. The three-phase MMC consists of 6 arms and each arm utilizes 8 number of Si and SiC HBSMs. The system has been implemented for medium voltage applications with a power rating of 10 MW and a DC link of 1.4 kV. From the obtained results, fig 4 shows $N+1$ voltage output levels for the upper and lower arms and the output current of phase A. The voltage across each SM is sorted and balanced at 175 V based on the DC link voltage divided by the number of SMs V_{dc}/N, as it can be seen in fig 5. The three-phase MMC voltage output with a peak voltage of 1.4 kV, and current waveform is shown in fig 6. Where fig 7 illustrates the three-phase AC grid voltage with peak of 630 V and a rated current of 11.2 kA.

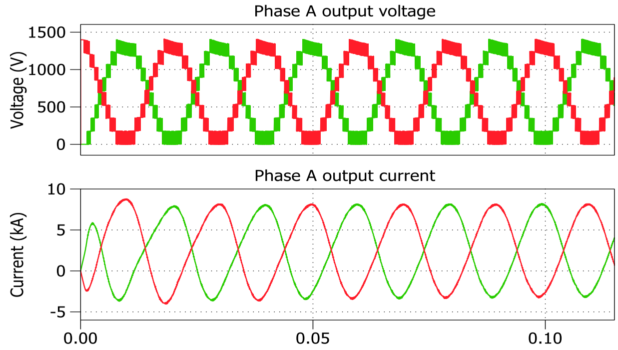

Fig 4. Phase A MMC output voltage and current.

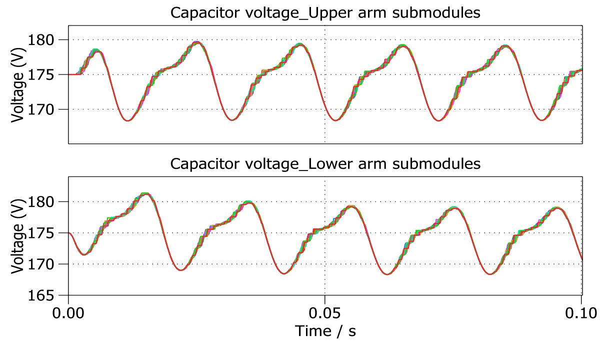

Fig 5. Phase A capacitor voltage balancing (upper and lower arms).

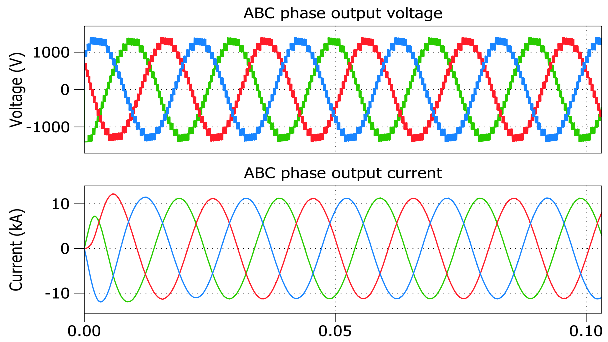

Fig 6. Three phase nine-levels MMC output voltage and current.

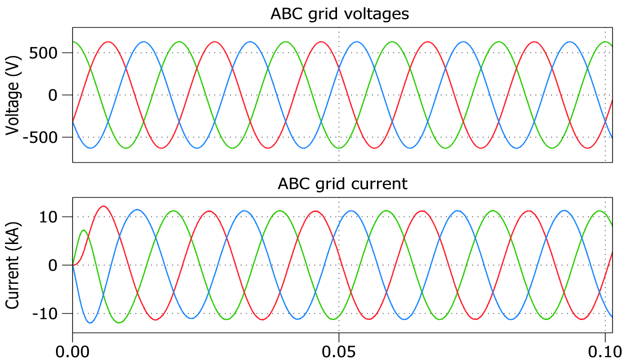

Fig 7. Three phase AC grid voltage and current.

IV. Power Loss and Cost Comparsion

In this section the switching and conduction power losses calculations were performed for both Si IGBT and SiC MOSFET devices using PLECS software programming. Two semiconductor devices have been chosen for the design of the proposed MMC_HBSMs model. The Si IGBTs device (IKWH20N65WR6) has a voltage rating of 650V and a current rating of 55A, while the SiC MOSFETs device (C3M0045065D) also has a voltage rating of 650V and a current rating of 49A. Additional parameters for both devices are listed in Table II, which have been used for power loss calculations.

In this study the thermal model has been applied for both IGBT and SiC devices to investigate the power loss at different junction temperatures and a switching frequency of 7 kHz. A PLECS/Simulink block was created for the HBSMs cell to test and estimate the switching and conduction power losses within each Si IGBT and SiC MOSFET switch, as well as the total power losses within each HBSMs cell. The switching loss analysis of both IGBT and SiC devices was calculated based on the turn-on, turn-off, and diode reverse recovery processes (t_{on}, t_{off} and t_{rr}) using equations (15 and 16) [4]. The datasheet of either Si IGBTs or SiC MOSFETs typically provides parameters such as turn-on and turn-off energies (E_{on}, E_{off}) related to the switching current at specific voltage levels.

$$P_s = E_{onT1} + E_{offT1} + E_{onT2} + E_{offT2} + E_{rrD1} + E_{rrD2} \times f_s \quad (15)$$

$$P_c = I_{rms}{}^2 \times R_{DS\,(on)} \quad (16)$$

Where P_s and P_c represent the switching and conduction loss, E_{onT1}, E_{offT1} and E_{rrD1} are represent the power loss of the upper switch of HBSM during on and off time including the diode's reverse recovery. E_{onT2}, E_{offT2} and E_{rrD2} are represent the power loss of the lower switch of HBSM during on and off time including the diode's reverse recovery. Where fs is the switching frequency.

The results of switching and conduction loss for both switches have been shown in fig 9, fig 10 and fig 11. These results indicate that the conventional Si IGBT devices have a higher power loss with a total of 15.3163 W at normal temperature 25°C. In contrast, the total power loss of SiC MOSFETs at the same temperature is three times lower than that of Si IGBT devices. However, when considering the cost SiC-based devices are six times more expensive than traditional IGBT devices. Therefore, it can be concluded that SiC MOSFETs have lower power loss and better efficiency compared to Si IGBT-based devices.

The power loss for only one HBSM cell was calculated, while assuming the same loss for all the other MMC-HBSMs. Where the HBSM cell was tested under different conditions and junction temperatures as shown in fig 12. In the first case, pure Si IGBT devices were used for the HBSM cell, resulting in a total power loss of 30.6326 W at normal temperature and 35.512 W at 150°C. In the second case, pure SiC MOSFET was used, and the power loss decreased to 9.1396 W at 25°C and 9.9884 W at high temperature 150°C compared to the pure IGBT devices. In the third case, which is the proposed model a HBSM was tested utilizing a Si IGBT and SiC MOSFET hybrid system, and the results indicate that the total power loss was reduced to 19.8861 W at 25°C and 22.7502 W at 150°C compared to a pure Si IGBT system. This suggests that the hybrid technique is the best option for MMC-HBSMs in terms of total power losses compared to HBSM based on conventional IGBT devices and is cost-effective compared to HB cell using a pure SiC switches.

TABLE II. SPECIFICATIONS OF SI IGBT AND SIC MOSFET SWITCHES

Parameters	Type of Switches	
	***Si IGBT*s**	***SiC MOSFETs***
Part Number	IKWH20N65WR6	C3M0045065D
Voltage V_{CE}, V_{DS}	650 *V*	650 *V*
Current I_{DS} (Tc = 25 °C)	55 *A*	49 *A*
Current I_{DS} (Tc = 100 °C)	35 *A*	35 *A*
V_{CEsat}, $R_{DS.on}$ (Tc = 25 °C)	1.35 *V*	45 *m*Ω
V_{CEsat}, $R_{DS.on}$ (Tc = 100 °C)	1.60 *V*	60 *m*Ω

The comparison of the MMC models was considered based on the analysis of semiconductor power devices losses, while other MMC components were ignored. The three-phase MMC 9-voltage level model based on HBSMs was tested using pure Si IGBT devices and pure SiC MOSFETs. Then compared their performance with a Si/SiC hybrid proposed model in terms of total power losses, efficiency, and cost. Where the cost of Si IGBTs and SiC MOSFETs devices was obtained from the online market.

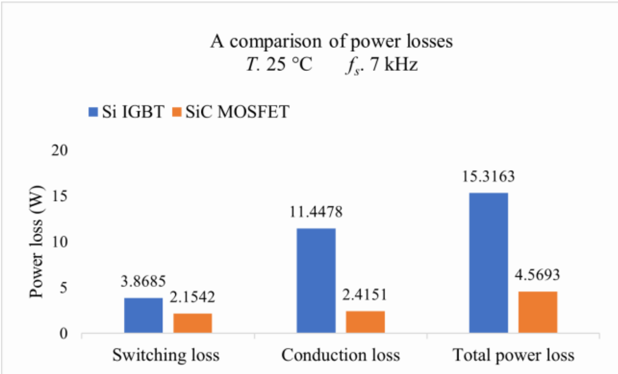

Fig 8. Power loss comparison of Si IGBT and SiC MOSFET devices. T_j = 25 °C and f_s = 7 kHz.

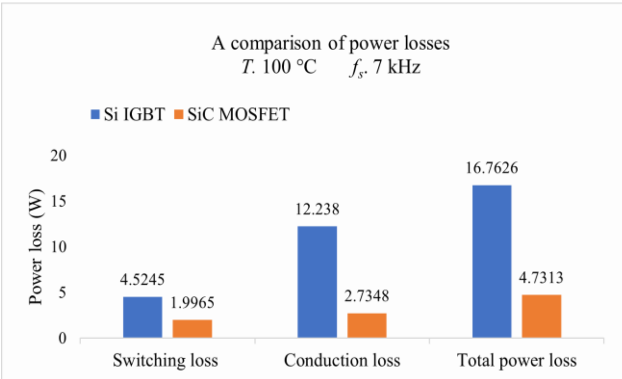

Fig 9. Power loss comparison of Si IGBT and SiC MOSFET devices. T_j = 100 °C and f_s = 7 kHz.

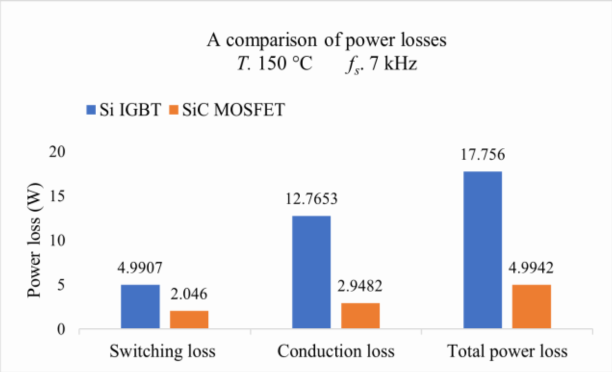

Fig 10. Power loss comparison of Si IGBT and SiC MOSFET devices. T_j = 150 °C and f_s = 7 kHz.

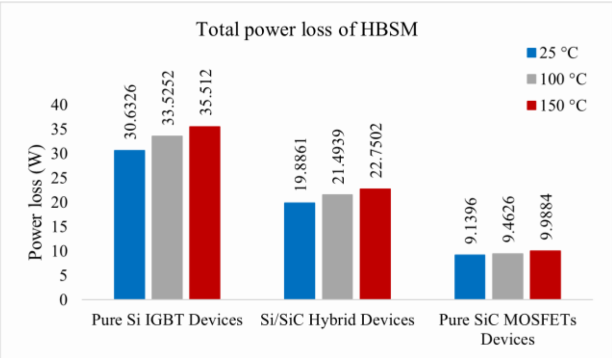

Fig 11. Power loss comparison of HBSMs at different junction temperatures T_j and f_s = 7 kHz.

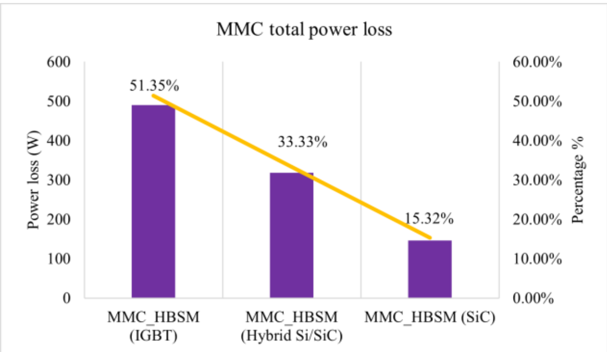

Fig 12. Total power loss comparison of MMC topologies.

From Table III, it can be observed that the total power losses of MMC-HBSMs based on conventional pure Si IGBTs is higher than the pure SiC-based model, with an efficiency of 95.3%. However, the cost of MMC-HBSMs based on pure SiC MOSFETs is five times higher than the Si IGBT-based model. Therefore, a Si IGBT/SiC MOSFET hybrid MMC model has reduced the total power loss to approximately 18% compared with the traditional MMC model, and the cost has been reduced to almost half compared with MMC based on pure SiC MOSFTs as shown in fig 12. In addition, improving the model's performance and achieving a system efficiency of 96.9% compared to the conventional MMC system.

TABEL III. POWER LOSS AND COST COMPARISON OF MMC TOPOLOGIES

Topology	Total power loss	Efficiency	Cost
MMC_HBSMs (IGBT)	490.1216 *W*	95.3 %	107.30 $
MMC_HBSMs (SiC)	146.2176 *W*	98.5 %	639.36 $
MMC_HBSMs (Hybrid IGBT/SiC)	318.1744 W	96.9 %	293.92 $

V. CONCLUSION

In this paper, a new MMC topology is presented, which utilizes a hybrid HBSM configuration consisting of Si IGBT at the upper side of the cell and SiC MOSFET at the lower side. The proposed model combines the advantages of both Si and SiC-based devices and aims to improve the overall performance of the MMC topology in terms of power losses and converter efficiency. A 9-levels output voltage for grid-connected with MMC model has been simulated to analyze the voltage and current characteristics where the converter has demonstrated excellent performance compared with the conventional topology.

A comparison of the performance, power losses, and converter's cost was considered for the proposed hybrid model based on the analysis of the switching and conduction power losses of both Si and SiC devices, as well as the total power losses within each HBSM. The MMC model based on the proposed Si and SiC hybrid HBSM achieves a reduction in total power loss of approximately 18% compared to the MMC model based on conventional Si IGBT devices, it also reduces the cost of semiconductor devices by about half compared to the MMC model based on SiC MOSFTs. The improvements of the proposed model allow for enhanced model performance and achieve a system efficiency of 96.9%.

ACKNOWLEDGMENT

The authors are sincerely grateful to the Higher Institute of Science and Technology Tigi-Libya for providing full financial support to make this research possible at the University of Lancaster.

REFERENCES

[1] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," *2003 IEEE Bol. PowerTech - Conf. Proc.*, vol. 3, pp. 6–11, 2003, doi: 10.1109/PTC.2003.1304403.

[2] M. A. Perez, S. Ceballos, G. Konstantinou, J. Pou, and R. P. Aguilera, "Modular Multilevel Converters: Recent Achievements and Challenges," *IEEE Open J. Ind. Electron. Soc.*, vol. 2, no. March, pp. 224–239, 2021, doi: 10.1109/OJIES.2021.3060791.

[3] T. Yin, L. Lin, C. Xu, D. Zhu, and K. Jing, "A Hybrid Modular Multilevel Converter Comprising SiC MOSFET and Si IGBT With Its Specialized Modulation and Voltage Balancing Scheme," *IEEE Trans. Ind. Electron.*, vol. 69, no. 11, pp. 11272–11282, 2022, doi: 10.1109/TIE.2021.3118372.

[4] A. M. Shende, S. K. Patro, and M. A. Chaudhari, "Hybrid Modular Multilevel Converter based on Si and SiC Devices with Level Multiplier Circuit," in *Proceedings of 2021 IEEE 2nd International Conference on Smart Technologies for Power, Energy and Control, STPEC 2021*, Institute of Electrical and Electronics Engineers Inc., 2021. doi: 10.1109/STPEC52385.2021.9718649.

[5] A. Athwer and A. Darwish, "A Review on Modular Converter Topologies Based on WBG Semiconductor Devices in Wind Energy Conversion Systems," *Energies*, vol. 16, no. 14, 2023, doi: 10.3390/en16145324.

[6] R. R. Duarte, G. F. Ferreira, M. A. Dalla Costa, and J. Marcos Alonso, "Performance comparison of Si and GaN transistors in a family of synchronous buck converters for LED lighting applications," *IEEE Ind. Appl. Soc. 52nd Annu. Meet. IAS 2016*, pp. 1–7, 2016, doi: 10.1109/IAS.2016.7731892.

[7] B. Zhang and S. Wang, "A Survey of EMI Research in Power Electronics Systems With Wide-Bandgap," vol. 8, no. 1, pp. 626–643, 2020.

[8] X. Yuan, I. Laird, and S. Walder, "Opportunities, Challenges, and Potential Solutions in the Application of Fast-Switching SiC Power Devices and Converters," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 3925–3945, 2021, doi: 10.1109/TPEL.2020.3024862.

[9] S. Ji, Z. Zhang, and F. F. Wang, "Overview of High Voltage SiC Power Semiconductor Devices : Development and Application," *CES Trans. Electr. Mach. Syst. 1(3), pp.254-264.*, vol. 1, no. 3, pp. 254–264, 2017.

[10] C. Gupta and S. S. Pasayat, "Vertical GaN and Vertical Ga2O3 Power Transistors: Status and Challenges," *Phys. Status Solidi Appl. Mater. Sci.*, vol. 219, no. 7, pp. 1–12, 2022, doi: 10.1002/pssa.202100659.

[11] T. Zhang, Y., Sun, M., Piedra, D., Hu, J., Liu, Z., Lin, Y., Gao, X., Shepard, K. and Palacios, "1200 V GaN vertical fin power field-effect transistors.," *IEEE Int. Electron Devices Meet. (IEDM).*, pp. 215–218, 2017.

[12] Z. Tang, Y. Yang, and F. Blaabjerg, "Power electronics: The enabling technology for renewable energy integration," *CSEE J. Power Energy Syst.*, vol. 8, no. 1, pp. 39–52, 2022, doi: 10.17775/CSEEJPES.2021.02850.

[13] X. Yuan, J. Wang, I. Laird, and W. Zhou, "Wide-Bandgap Device Enabled Multilevel Converters with Simplified Structures and Capacitor Voltage Balancing Capability," *IEEE Open J. Power Electron.*, vol. 2, no. March, pp. 401–410, 2021, doi: 10.1109/OJPEL.2021.3094713.

[14] T. Yin, L. Lin, X. Shi, and K. Jing, "A Si/SiC Hybrid Full-Bridge Submodule for Modular Multilevel Converter With its Control Scheme," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 11, no. 1, pp. 712–721, 2023, doi: 10.1109/JESTPE.2022.3208602.

[15] Y. Sun, L. Han, B. Li, Z. Xu, S. Zhou, and D. Xu, "A Hybrid Modular Multilevel Converter Comprising Si Submodules and SiC Submodules with Its Specialized Capacitor Voltage Balancing Strategy," in *2022 IEEE Transportation Electrification Conference and Expo, Asia-Pacific, ITEC Asia-Pacific 2022*, Institute of Electrical and Electronics Engineers Inc., 2022. doi: 10.1109/ITECAsia-Pacific56316.2022.9942174.

[16] M. N. Raju, J. Sreedevi, R. P. Mandi, and K. S. Meera, "Modular multilevel converters technology: A comprehensive study on its topologies, modelling, control and applications," *IET Power Electron.*, vol. 12, no. 2, pp. 149–169, 2019, doi: 10.1049/iet-pel.2018.5734.

[17] R. V. K. Challa, S. Mikkili, and P. K. Bonthagorla, "Modeling, Controlling Approaches, Modulation Schemes, and Applications of Modular Multilevel Converter: Review," *J. Control. Autom. Electr. Syst.*, vol. 34, no. 1, pp. 189–215, 2023, doi: 10.1007/s40313-022-00953-8.

[18] S. Ali, Z. Ling, K. Tian, and Z. Huang, "Recent Advancements in Submodule Topologies and Applications of MMC," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 9, no. 3, pp. 3407–3435, 2021, doi: 10.1109/JESTPE.2020.2990689.

[19] F. Martinez-Rodrigo, D. Ramirez, A. B. Rey-Boue, S. De Pablo, and L. C. Herrero-De Lucas, "Modular multilevel converters: Control and applications," *Energies*, vol. 10, no. 11, 2017, doi: 10.3390/en10111709.

[20] M. Hagiwara and H. Akagi, "Control and Experiment of Pulsewidth-Modulated Modular Multilevel Converters," *IEEE Trans. Power Electron.*, vol. 24, no. 7, pp. 1737–1746, 2009, doi: 10.1109/TPEL.2009.2014236.

[21] H. Akagi, "Multilevel Converters: Fundamental Circuits and Systems," *Proc. IEEE*, vol. 105, no. 11, pp. 2048–2065, 2017, doi: 10.1109/JPROC.2017.2682105.

[22] K. Hafeez, S. A. Khan, A. Van den Bossche, and Q. Ul Hasan, "Circulating current reduction in MMC-HVDC system using average model," *Appl. Sci.*, vol. 9, no. 7, 2019, doi: 10.3390/app9071383.

[23] A. Darwish, D. Holliday, and S. Finney, "Operation and control design of an input-series-input-parallel-output-series conversion scheme for offshore DC wind systems," *IET Power Electron.*, vol. 10, no. 15, pp. 2092–2103, 2017, doi: 10.1049/iet-pel.2016.0885.