turbation, the transformer can be approximated by a single pole system the time constant of which is mainly related to the dumping resistance of the RLC series branch in the equivalent circuit. A second pole is introduced by the rectifier [6], so the whole system could be approximated by a two pole transfer function. Note that the PWM modulator moves the negative slope edge of the input voltage signal changing the duty cycle and consequently the amplitude of the fundamental harmonic. Positive slope edges remain fixed, therefore the switching period imposed by the PFD circuit does not change and resonance operation is maintained.

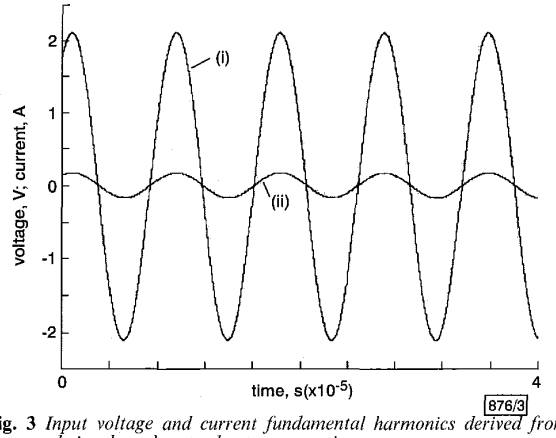

Fig. 3 *Input voltage and current fundamental harmonics derived from measured signals under steady-state operation*

(i) input voltage harmonic
(ii) input current harmonic

Experimental results: The proposed control method was applied to a laboratory prototype of the converter. Input DC voltage was 3.3 V and output was regulated at –1 kV DC (sensed through a 1/5000 voltage divider), while in open loop configuration output reached –1.7 kV DC. The VCO frequency range could vary from 90 to 130 kHz as shown in Fig. 2, which also shows basic waveforms of the converter at start-up. The VCO input grows until the loop sets the value of frequency at which the input voltage square wave is synchronous to the squared input current signal. Measured input voltage and current signals under steady-state operation were acquired numerically and elaborated to extract the fundamental harmonics. The results are shown in Fig. 3 in which we can observe their synchronism. Finally, from Fig. 2 we see the operation of the voltage error amplifier, which moves the duty cycle from 0% towards 50%. The amplifier output settles at a value which is lower than the maximum allowed, when the desired output is reached.

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E. Dallago and A. Danioni (*Power Electronics Laboratory, Department of Electrical Engineering, University of Pavia, Via Ferrata 1, I 27100 Pavia, Italy*)

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Simple digital test approach for embedded charge-pump phase-locked loops

M.J. Burbidge and A.M. Richardson

Techniques for a simple automated test approach for high performance fully embedded charge-pump phase-locked loops (CP-PLLs) are explained. The test approach is focused towards non-invasive high volume production testing of PLLs using digital only testers in conjunction with additional on-chip circuitry.

Introduction: In recent years the charge-pump phase-locked loop (CP-PLL) has become a ubiquitous mixed signal (M/S) building block. The most common application for the CP-PLL is for on-chip clock regeneration. All other on-chip functions will be reliant on the operation of the PLL, thus it is essential that it is verified correctly. Unfortunately, problems relating to test time, and test access, can lead to the PLL being insufficiently tested. Often only a simple frequency lock test (FLT) is carried out on the PLL. Although the FLT will uncover many hard faults in the PLL, it does not generally provide sufficient information relating to short-term transient operation (instability and jitter effects). Characteristics effecting transient operation such as CP mismatch, CP leakage, CP nonlinearity, loop filter (LF) leakage, voltage controlled oscillator (VCO) nonlinearity and static phase error, are strongly dependent on forward path (FP) PLL blocks. In this Letter we outline a simple non-invasive measurement technique that can be used to monitor FP operation, and thus provide improved information on PLL operation [1].

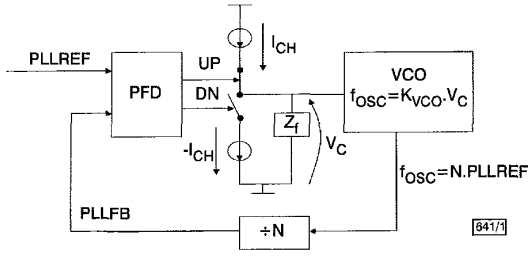

Fig. 1 *Basic CP-PLL architecture*

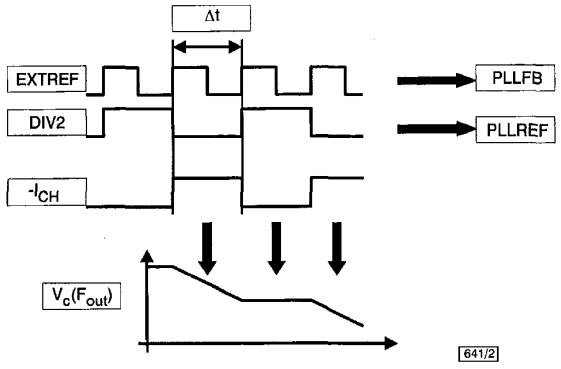

Fig. 2 *Oscillator operation for PLLREF ≈ PLLFB/2*

Basic CP-PLL structure: In Fig. 1 PLLREF and PLLFB are pulse streams. The phase frequency detector is an edge sensitive device that sets UP or DN for a time proportional to the time difference between the PLLREF and PLLFB edges. This action charges or (discharges) the LF (Zf), thus V_C increases or (decreases), and f_{OSC} increases or (decreases). The waveforms for PLLREF = PLLFB/2 (i.e. PLLREF is at half the frequency of PLLFB) are shown in Fig. 2. This basic operation can be exploited to facilitate testing of the forward path blocks. In normal operation, connection of the blocks as shown allows generation of an output signal that is phase aligned to the input signal. Further information on CP-PLL operation can be found in [2, 3].

Basic test outline: hardware description: The basic concept behind the test is to allow the FP blocks of the PLL to be exercised while

the PLL is in an open loop (OL) configuration. Input paths of the PLL are redirected using an input multiplexer (MUX). Parameter extraction is facilitated by direct measurement of the VCO output frequency using an on-chip frequency counter as in [4, 5]. The parameters are stored and scanned out using digital circuitry. Fig. 3 shows the required hardware blocks and MUX connections.

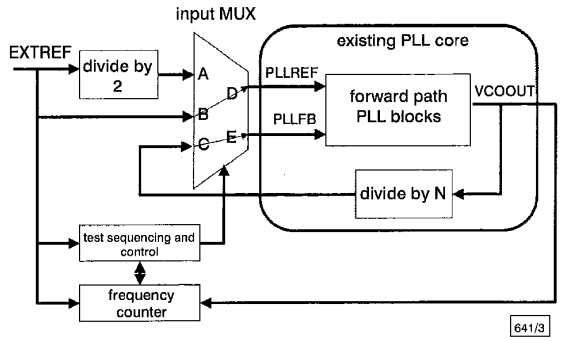

Fig. 3 *Additional on-chip test hardware*

Table 1: Test sequence and MUX connections

Step	Description	MUX connections		Result
(i)	Frequency lock test Normal operation (closed loop)	B = D	C = E	F1
(ii)	Ramp down (OL)	A = D	B = E	F2
(iii)	Ramp up (OL)	B = D	A = E	F3
(iv)	Hold mode (OL)	B = D	B = E	F4

Application and output response: The hardware at the input of the PLL can be controlled as shown in Table 1. Synchronised control of the PLL in this manner will produce a corresponding change in the VCO output frequency as shown in Fig. 4. Table 2 summarises information that can be obtained from the test. Note that to check for excessive CP or VCO nonlinearity, additional frequency measurement stages can be added in steps (ii) and (iii).

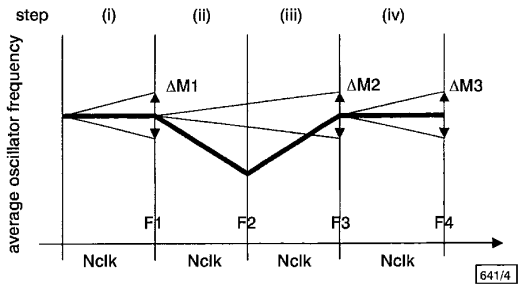

Fig. 4 *Oscillator output variation*

F# = measured frequencies after each step
ΔM# = allowable tolerance for each measurement
Nclk = N*EXTREF (equal number of cycles for each test step)

Table 2: Test information and results

Step	Description	Information	Value
(i)	Frequency lock test	Ensures that PLL can attain lock. Sets reference frequency (F1). Exercise all of PLL components at maximum operational frequency to check for high-speed faults.	F1
(ii)	Ramp down	Gain of forward path blocks. CP/VCO nonlinearity (see text).	F1–F2
(iii)	Ramp up	Gain of forward path blocks. CP/VCO nonlinearity (see text).	F2–F3
		CP mismatch from steps (ii) and (iii).	F1–F3
(iv)	Hold mode	LF/CP leakage. Excessive constant phase offsets in forward path.	F3–F4

Equations in ramp down mode (see Figs. 1 and 2): Using an approximation for Zf ($Zf = C$), and assuming that PLLREF is always at twice the frequency of PLLFB, the following equation can be derived relating the change in oscillator output frequency to the external reference signal:

$$\Delta f_{OSC} \propto \Delta V_C = \frac{N_{EXTREF}}{2} \cdot \frac{-I_{CH}}{C \cdot f_{EXTREF}}$$

where Δf_{OSC} is the change in the oscillator output frequency, f_{EXTREF} is the frequency of EXTREF, I_{CH} is the current supplied by the CP structures, and N_{EXTREF} is the number of cycles that the input signal is applied for. Note that equations in the ramp up mode are identical with the exception that the direction of current flow from the loop filter is reversed. The procedure used to obtain the relationship between Δf_{OSC} and ΔF_{EXTREF} will be applicable to any $Zf(s)$ usually incorporated in a CP-PLL. It is important to note that in the final equation I_{CH} is a function of the CP circuitry, and is known by design. Δf_{OSC} will be related to the VCO input voltage and the K_{VCO} (the gain of the VCO in MHz/V or rad/s/V) which will be known by design. N_{EXTREF} and f_{EXTREF} can be accurately controlled.

Thus, a measure of the forward path gain of the PLL blocks, related to a precise time difference at the input, can be obtained. Furthermore, it is possible to map the measured frequency value to desired responses.

Conclusion: A non-invasive BIST method for CP-PLLs has been presented. The test approach is intended to augment the commonly-used FLT, and targets significant PLL sub-block characteristics that have direct impact on the short-term transient operation of the PLL. Furthermore, the test can be realised using simple hardware and results can be mapped directly to design specifications.

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M.J. Burbidge and A.M. Richardson (*Centre for Microsystems Engineering, Faculty of Applied Sciences, Lancaster University, LA1 4YR, United Kingdom*)

E-mail: m.burbidge@lancaster.ac.uk

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Soft-switching boost chopper for diode bridge power factor correction

B. Han and S. Moon

A new soft-switching boost chopper, which can be utilised for diode-bridge power factor correction, is presented. The soft-switching cell is composed of two switch-diode pairs linked by an inductor and a capacitor in parallel. The soft-switching scheme is verified by means of PSPICE simulation and prototype experiment.

Introduction: To improve the power factor in single-phase diode bridge, the boost chopper has been utilised widely. Much research