Radial Tunnel Diodes based on InP/InGaAs Core-Shell Nanowires

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We report on the fabrication and characterization of radial tunnel diodes based on InP(n+)/InGaAs(p+) core-shell nanowires, where the effect of Zn-dopant precursor flow on the electrical properties of the devices is evaluated. Selective and local etching of the InGaAs shell is employed to access the nanowire core in the contact process. Devices with an n^+-p doping profile show normal diode rectification, whereas n^+-p^+ junctions exhibit typical tunnel diode characteristics with peak-to-valley current ratios up to 14 at room temperature and 100 at 4.2 K. A maximum peak current density of 28 A/cm^2 and reverse current density of 7.3 kA/cm^2 at V_{SD}=-0.5 V are extracted at room temperature after normalization with the effective junction area.

KEYWORDS: Heterostructure, Tunnel diode, Esaki diode, Nanowire, Core-shell, InP, InGaAs.

Tunnel diodes [1] are characterized by negative differential resistance (NDR) in the forward bias direction and zero bias reverse breakdown. Because of this particular current-voltage characteristic, combined with the very fast operation of tunnel diodes, they have been proposed for use in various RF microwave applications such as amplifiers and oscillators [2-4]

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and are used in multi-junction solar cells [5-7]. In recent years, they have also attracted particular attention as building blocks for low power electronics. It is theoretically possible to obtain subthreshold swings steeper than the thermal limit of 60mV/decade at room temperature by fabricating transistors based on gated diodes with a p-i-n doping profile [8-10]. Recent developments in growth of epitaxial nanowires allow fabrication of nanowire electronic devices based on lattice mismatched semiconductor materials in axial and radial geometries [11-14]. Amongst these structures, nanowires based on radial heterojunctions are particularly attractive for field-effect transistor research due to the possibility of employing a wrap-gate [15], and for cylindrical multi-junction solar cells [16-19] where they provide separate paths for light and charge collection [20-22].

In this paper, we demonstrate the fabrication and electrical characterization of radial tunnel diodes based on InP(*n*+)/InGaAs(*p*+) core-shell nanowires. The effect of InGaAs shell doping concentration on the electrical properties of a series of fabricated devices is investigated. It is found that an NDR region appears under forward voltage bias for nanowires grown with higher Zn-dopant precursor flows. Esaki characteristics with peak-to-valley current ratios (PVCR) up to 14 are observed in the forward bias region at room temperature. Decreasing the temperature leads to a noticeable increase of the PVCR, with a highest value of 100 observed at liquid helium temperature.

The nanowires were grown from nano-imprint lithography (NIL) defined Au particles inside holes of a 20 nm thick SiN_x mask deposited on (111) B InP substrates. The NIL pattern has a period of 400 nm with aligned columns of Au particles, where each column is slightly offset. The imprint process was carried out on 2" wafers with an Obducat AB developed process that uses an intermediate polymer stamp (IPS) and soft press technology [23]. Before Au deposition the SiN_x was dry etched to expose the InP surface under the Au particle. The remaining SiN_x acted as a growth mask and prevented parasitic growth on the substrate

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surface. The growth experiments were carried out in a horizontal flow, low pressure, metal-organic vapour phase epitaxy (MOVPE) reactor with a total flow of 6 l/min. The precursors used for growth were trimethylindium (TMIn), trimethylgallium (TMGa), arsine (AsH_3), phosphine (PH_3), hydrogen sulfide (H_2S), and diethylzinc (DEZn). Hydrogen chloride (HCl) was used to impede radial growth while H_2 was used as the carrier gas [24]. The InP/InGaAs core-shell nanowire structure was fabricated in two steps [25]. Firstly, the InP core was grown at a temperature of 395 °C using molar fractions: $\chi_{TMIn} = 8.2\times10^{-6}$, $\chi_{PH3} = 18.5\times10^{-3}$, $\chi_{H2S} = 6.7\times10^{-6}$ and $\chi_{HCl} = 1.0\times10^{-5}$. After the core growth, the nanowire samples were removed from the MOVPE reactor and the Au alloy particle was removed by wet etching using H_2SO_4:H_2O (1:10) and KI:I_2:H_2O (4 g:1 g:40 mL) solutions at room temperature [26]. A second MOVPE step was used to grow an InGaAs shell on the InP nanowire cores at a growth temperature of 600 °C with $\chi_{TMGa} = 1.9\times10^{-5}$, $\chi_{TMIn} = 1.2\times10^{-5}$ and $\chi_{AsH3} = 2.2\times10^{-3}$. The amount of DEZn was varied in a series from $\chi_{DEZn} = 0.16\times10^{-5}$ to 4.6×10^{-5}. Since the Au particle had been removed from the tip of the nanowires, axial growth was limited and most of the InGaAs material deposited on the nanowire sidewalls (Figure 1a and 1b).

After growth, the nanowires were broken off and transferred from the growth substrate to heavily *n*-doped silicon substrates capped with 100 nm thick SiO_2. Single nanowire tunnel diodes were processed by fabricating drain and source metal contacts to the core and to the InGaAs shell of selected nanowires using electron beam lithography (EBL) and thermal evaporation.

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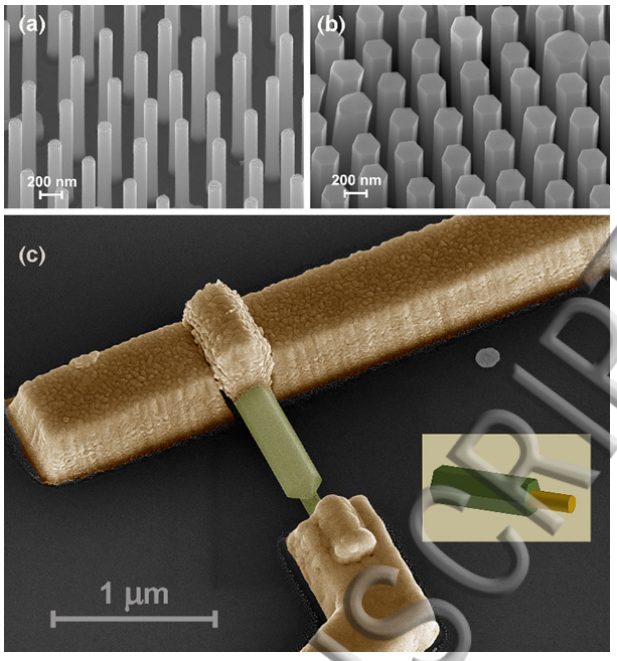

Figure 1: (a) As grown InP nanowires after removing the Au particle. (b) InP/InGaAs Core-shell nanowires. (c) The fabricated InP/InGaAs radial tunnel diode with two electrical contacts on the core and the shell of the nanowire. The inset shows a schematic of the nanowire after selective etching of the InGaAs shell.

Contact to the nanowire core was achieved by selective etching of the InGaAs shell at one end of selected nanowires using EBL and wet chemical etching. Subsequent to an oxygen plasma ashing of the exposed area, wet chemical etching was used to remove the InGaAs shell from the entire contact area. The etchant solution offering the best observed selectively and etch depth was [27]: A=H_2SO_4:H_2O_2:H_2O (ratio of 1:1:8) and B=$C_6H_8O_7$:H_2O (ratio of 1:1). The two components A and B were prepared and mixed at room temperature immediately before use with the amount of solution B being equal to the amount of hydrogen peroxide in solution A. The wet etching creates a necessary undercut preventing an electrical short-circuit between the source and drain contacts. Metallization was done by thermal evaporation of Ti/Au (20/250 nm) to obtain the electrical contacts to the InP core. The InGaAs shell contact was defined in another EBL step followed by thermal evaporation of 20 nm Pd and 300 nm Au. Prior to shell contact metallization, the exposed nanowire contact areas were etched with

buffered HF for 15 s to remove the native oxide. Figure 1c shows an SEM micrograph of a fabricated device.

In order to investigate the room temperature band-to-band tunnelling (BTBT) mechanism in InP/InGaAs core-shell nanowires individual devices were electrically characterised in darkness and under vacuum conditions. A minimum of ten functioning devices were simultaneously fabricated from the corresponding wafer for each of the quoted flow rates. The data given herein corresponds to typical device parameters for each group. A liquid helium environment was used for the temperature dependent measurements. In all measurements the drain voltage, V_{SD}, was applied to the InGaAs shell while the *n* segment, InP core, was fixed at ground potential. In this set of experiments, three groups of nanowires with different Zn precursor flow during the shell growth were studied and a correlated distribution of electrical properties was observed from devices in the same doping groups. In order to elucidate the physical mechanism of the deduced *I-V* curves, a simulated band structure of an InP/InGaAs heterostructure is illustrated in Figure 2a. The band structure was calculated using Bandprof with an assumed doping concentration of 10^{19} cm^{-3} on either side of the junction [28].

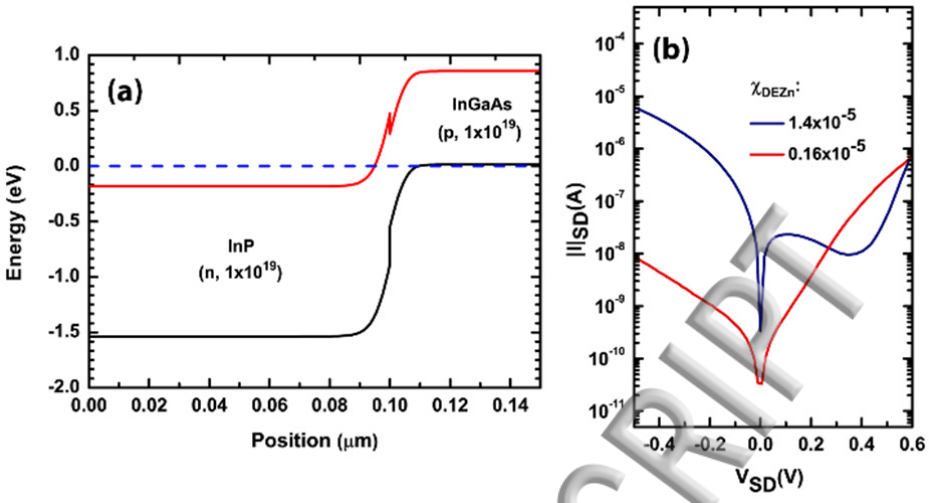

Figure 2: (a) Room temperature equilibrium band structure of the InP(n++)/InGaAs(p++) tunnel diode, with assumed n=p= 1×10^{19} doping concentration on either side of the junction.(b) Output characteristics of two devices with χ_{DEZn} of 0.16×10^{-5} and 1.4×10^{-5}. An obvious increase in tunnelling properties by increasing the applied χ_{DEZn} can be seen.

Figure 2b shows room temperature *I-V* characteristics of two representative devices with different χ_{DEZn} applied during the growth process. Nanowires fabricated from a sample grown with low χ_{DEZn} (0.16×10^{-5}), exhibit rectifying diode characteristics with rectification ratios of $\sim10^2$ at ±0.5 V. An ideality factor of 2.26 is extracted for this device at biases where the diffusion current component dominates. This number is higher than that of an ideal *p-n* junction (η=1), which we attribute to the high *n*-doping in the InP core leading to carrier recombination across the depletion region via trap assisted states.

Increasing the DEZn flow during the growth results in nanowires that show typical tunnel diode behaviour with a clear NDR region under forward bias. The blue curve in Figure 2b shows the *I-V* characteristics of a nanowire grown with $\chi_{DEZn} = 1.4\times10^{-5}$. The nanowire device itemised here had maximum observed peak and reverse current densities of 28 A/cm^2 and 7.3 kA/cm^2 (at V_{SD}=-0.5V) normalised to the effective tunnelling junction area as estimated from SEM measurements. Although the BTBT can clearly be attributed to the

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increased doping of the InGaAs shell, further studies are needed to determine the precise doping concentration of the materials.

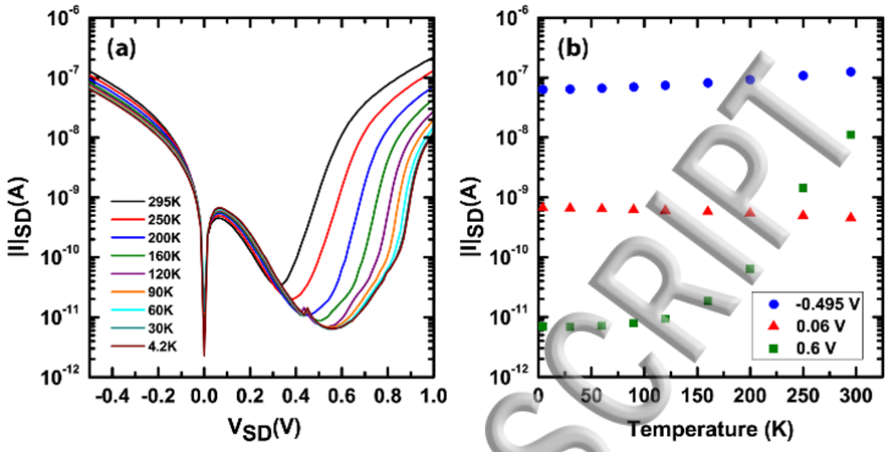

Figure 3: (a) Current-voltage characteristic of an InP/InGaAs tunnel diode at different temperatures ranging from 4.2 K to 295 K. (b) Absolute current versus temperature at selected biases of -0.495 V, 0.06 V and 0.6 V.

Nanowires grown with even higher Zn precursor flow, χ_{DEZn} of 4.6×10^{-5}, showed improved PVCRs, however at the expense of lower diode and BTBT currents. Figure 3a and 3b show the detailed temperature dependent output characteristics of a device with the highest observed PVCR ($\chi_{DEZn} = 4.6\times10^{-5}$). As shown by the black curve in the Figure 3a, at room temperature a peak current density of 0.39 A/cm^2 is measured at a voltage of Vp= 0.06 V. At slightly higher voltages, direct band-to-band tunnelling current vanishes, resulting in an observed valley current density of 0.029 A/cm^2 and a PVCR of 14. Moreover, the current in this region fits well to the theoretical model for direct band-to-band tunnelling which dominates at low biases (Figure 4):

$$I_{BTBT} = I_P \left(\frac{V}{V_P}\right) exp\left(1 - \frac{V}{V_P}\right) \quad (1)$$

where I_{BTBT} is the band-to-band tunnelling current, V_{SD} is the voltage across the heterojunction and I_P and V_P are the peak current and peak voltage, respectively.

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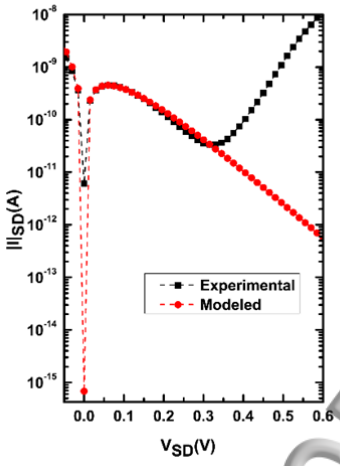

Figure 4: Room temperature band-to-band tunnelling at small biases. Black squares illustrate the absolute current versus bias for an InP/InGaAs radial tunnel diode with 4.6×10^{-5} χ_{DEZn} during the shell growth. Red circles represent the data predicted by modelling.

Unlike conventional diodes, in which the current flow is blocked up to the point known as the reverse breakdown voltage, the onset voltage of the reverse breakdown in a tunnel junction becomes zero due to the high dopant concentrations on either side of the junction. As shown in the Figure 3, under reverse bias conditions the increased overlap between valence band states in the *p*-region and available conduction band states in the *n*-region leads to a significant tunnelling current flow through the junction. The small decrease in reverse current with temperature shown in Figures 3a and 3b is due to an increase in series resistances at increasingly negative voltage values as well as the small change in the band gap. The peak current in the forward direction increases with reducing temperature despite an increased band gap (Figure 3b). This can be attributed to the decreased thermal spread of the Fermi function at low temperatures, implying that more energy states can contribute to the tunnelling process [29]. In contrast to the peak current, the peak voltage value is insensitive to

temperature as it is defined by the position of the Fermi levels on both sides far from the junction [30].

Increasing the bias beyond the tunnelling current peak results in a decrease in interband tunnelling due to the decreased overlap between electron and hole states in the *n* and *p* regions, manifesting in the observed NDR region in the forward bias characteristic. The direct BTBT current thus drops and eventually falls to a minimum known as the valley current where tunnelling via midgap defect states dominates. It is worth noting that in a degenerately-doped tunnel junction often only a small fraction of the valley current is due to the conventional *p-n* junction current. Instead, the dominating current is typically the so-called *excess* current, generally caused by indirect electron tunnelling via energy states located in the forbidden energy gap. These local energy levels are introduced by crystal defects, dislocations or donor and acceptor impurities during the junction fabrication. It is well known that degenerately-doped semiconductors are associated with exponential extensions of both conduction and valence band-edge tails into the forbidden energy gap, producing a range of available energy levels for tunnelling [31]. Figure 3a indicates that the excess current is strongly temperature dependent, which is the expected behaviour for tunnelling via mid-gap trap states.

The green curve in Figure 3b shows the variation of the excess current with temperature at a source-drain bias of 0.6 V. The excess current decreases rapidly with falling temperature, and as a result, the PVCR increases from 14 at room temperature to 100 at liquid helium temperature. These high PVCR's represent very low excess current at the junction resulting from epitaxial growth of a small cross-section, low defect interface in this sample.

TABLE I: Currents and PVCR for the InP(n+)/InGaAs(p+) radial tunnel diode at room temperature.

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DEZn Molar fraction		295K $\lvert J_R \rvert_{(V=-0.5\ V)}$ A/cm^2	J_P A/cm^2	J_V A/cm^2	PVCR
0.16×10^{-5}	Device A	7.7	--	--	--
	Device B	20	--	--	--
	Device C	43	--	--	--
1.4×10^{-5}	Device A	7300	28.6	11.3	2.5
	Device B	5600	9	2	4.5
	Device C	6400	12.5	8	1.5
4.6×10^{-5}	Device A	112	0.39	0.0286	14
	Device B	330	0.5	0.06	8
	Device C	343	2	0.2	10

At sufficiently high voltages (>0.4 V), the current is dominated by thermal diffusion of electrons from the conduction band on the InP side to the conduction band on the InGaAs side across the barrier formed at the heterointerface. This current component is also strongly temperature dependent as shown in Figure 3a. Table I provides a summary of the extracted properties for the devices discussed here together with other example nanowire devices from each different DEZn molar fraction group.

What is immediately clear in table I is the influence of higher Zn doping on devices characteristics. The nanowires grown with the high χ_{DEZn} of 4.6×10^{-5} show lower current density with higher PVCR compared to those grown with the χ_{DEZn} of 1.4×10^{-5}. This may be explained by the fact that incorporation of Zn into the InGaAs crystal lattice first increases with increasing precursor molar fraction and then at some point decreases, resulting in lower hole concentration and consequently, lower tunnelling currents [32].

Further, a large diffusion coefficient has been reported for Zn in the presence of a heavily doped n-type material [33]. Specifically, the increase in the free electron concentration and Fermi level in the crystal increases the thermal equilibrium concentration of negatively charged group III vacancies [34]. Zn diffusion into the n-type InP layer therefore alters the interface between the two materials, widening the depletion region and consequently increasing the potential barrier and the reducing tunnelling probability.

In conclusion, we have demonstrated radial tunnel diodes based on InP/InGaAs core-shell nanowires. With increasing χ_{DEZn} flows during the InGaAs shell growth a transition in junction properties was observed, from rectifying *p-n* junctions to tunnel diodes. Nanowire junctions grown with even higher χ_{DEZn} flows showed PVCR up to 14 at room temperature, and 100 at liquid helium temperature, at the expense of reduced current levels. A relatively high PVCR in this material system indicates the possibility of a low defect state density close to the heterointerface, which makes this material system attractive for various electronic and photonic applications. Furthermore, it proposes use for the study of the physics of the radial tunnel diode structures and the epitaxial growth processes necessary to realise high quality heterojunctions.

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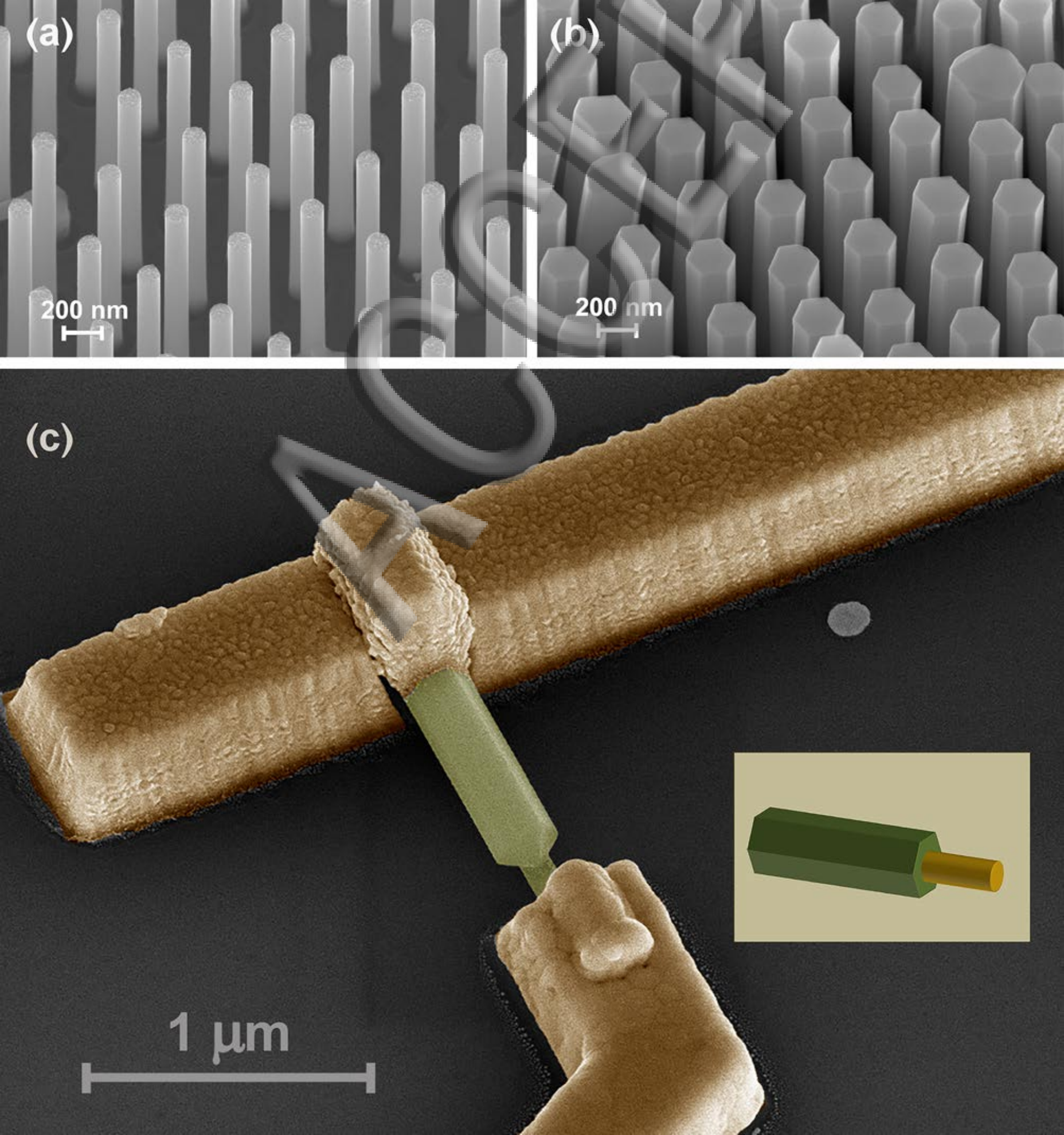
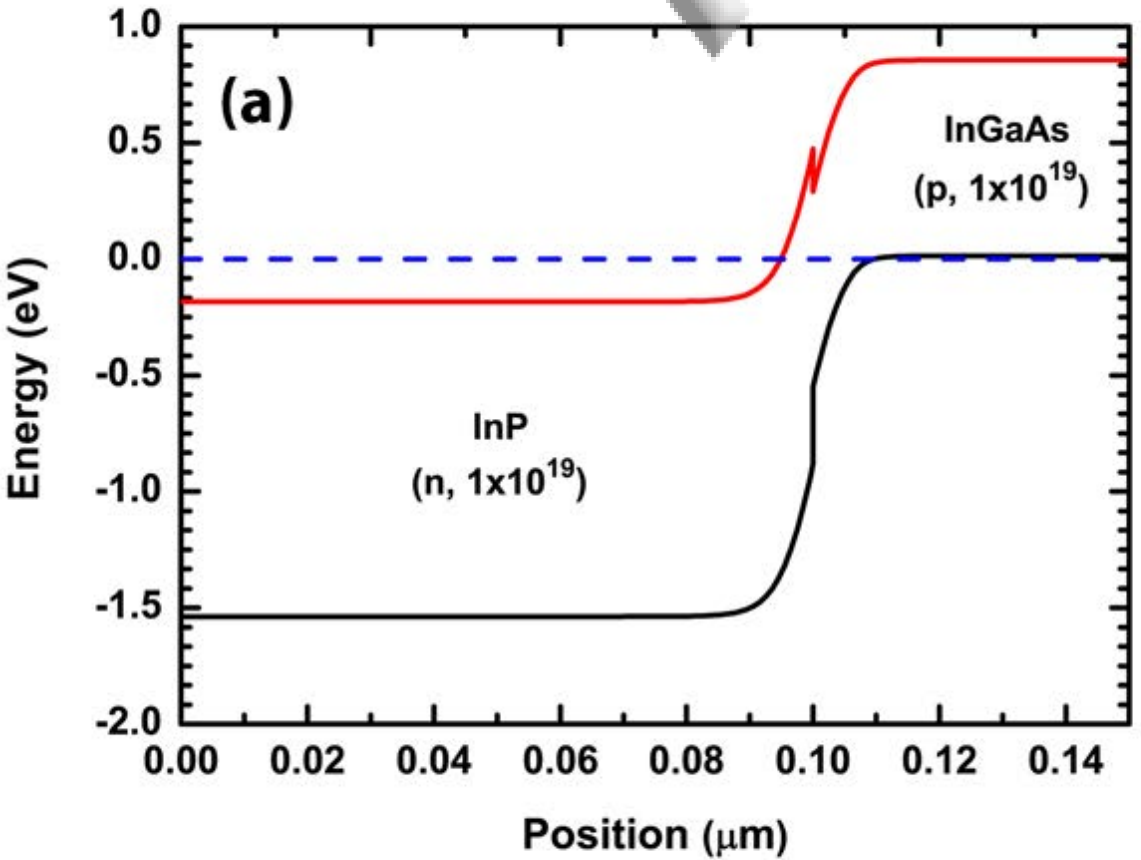
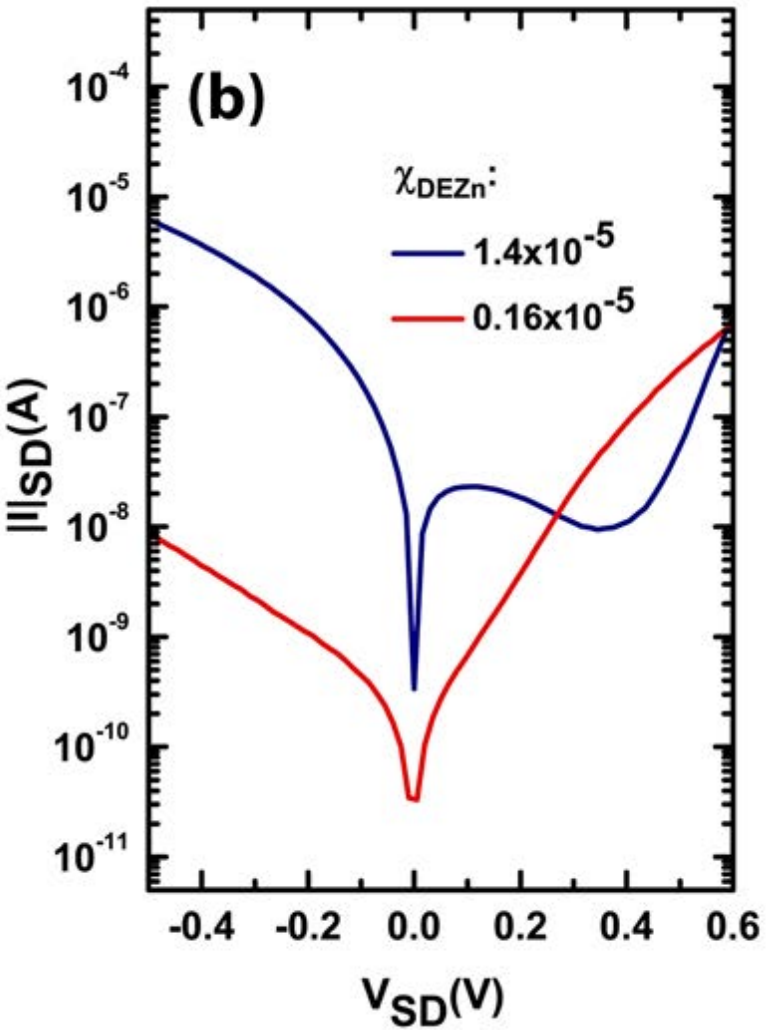
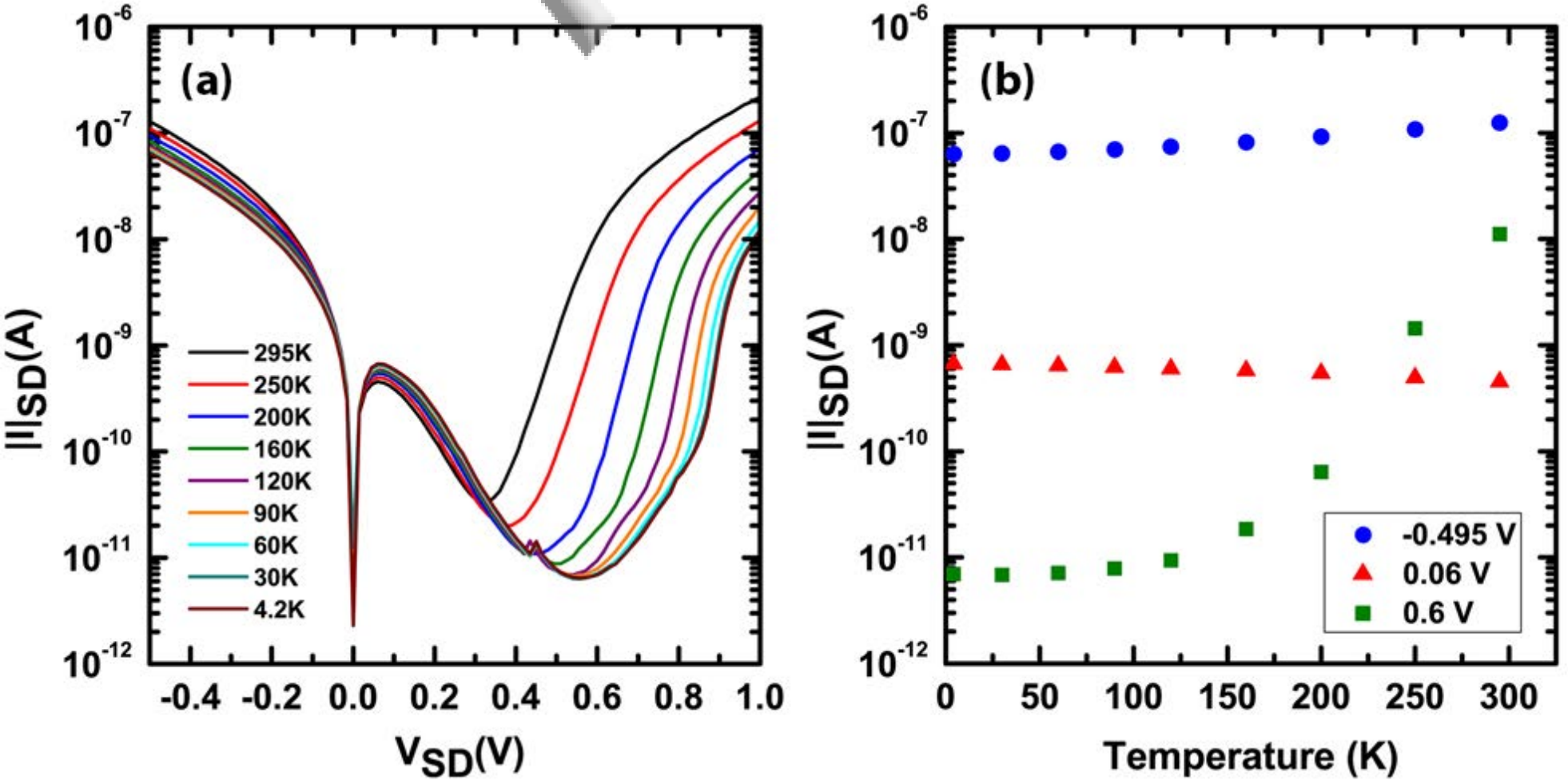
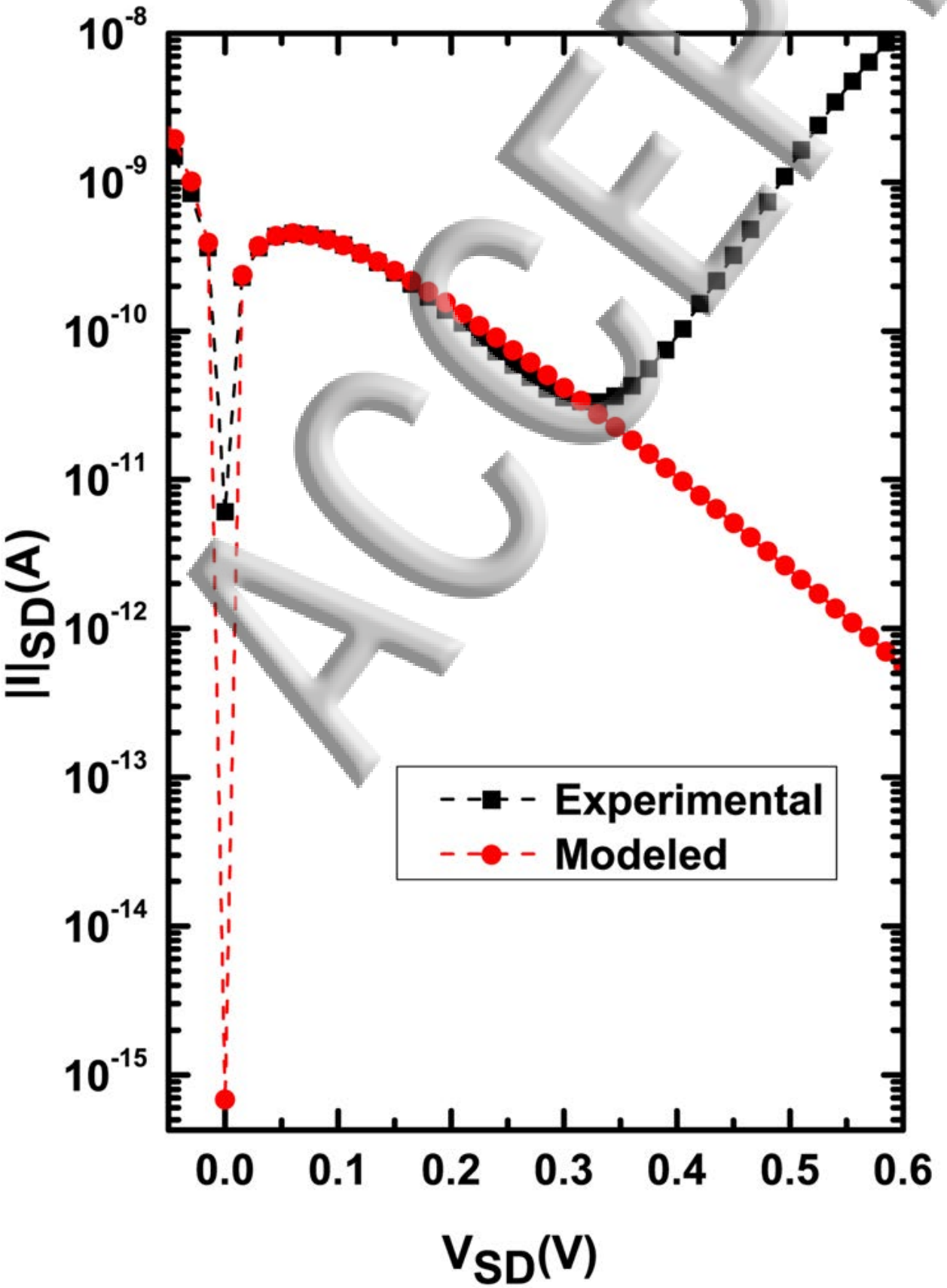

(a)
200 nm
(b)
200 nm
(c)
1 µm


(a)
InGaAs
(p, 1x10^19)
InP
(n, 1x10^19)
Energy (eV)
Position (μm)
1.0
0.5
0.0
-0.5
-1.0
-1.5
-2.0
0.00
0.02
0.04
0.06
0.08
0.10
0.12
0.14


(b)
χDEZn:
1.4x10^-5
0.16x10^-5
|I|SD(A)
VSD(V)
10^-4
10^-5
10^-6
10^-7
10^-8
10^-9
10^-10
10^-11
-0.4
-0.2
0.0
0.2
0.4
0.6


(a)
10^{-6}
10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
10^{-12}
$|I|_{SD}$(A)
295K
250K
200K
160K
120K
90K
60K
30K
4.2K
-0.4 -0.2 0.0 0.2 0.4 0.6 0.8 1.0
V_{SD}(V)
(b)
10^{-6}
10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
10^{-12}
$|I|_{SD}$(A)
-0.495 V
0.06 V
0.6 V
0 50 100 150 200 250 300
Temperature (K)


10^{-8}
10^{-9}
10^{-10}
10^{-11}
10^{-12}
10^{-13}
10^{-14}
10^{-15}
$|I|_{SD}(A)$
0.0
0.1
0.2
0.3
0.4
0.5
0.6
$V_{SD}(V)$
Experimental
Modeled