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Issue 244

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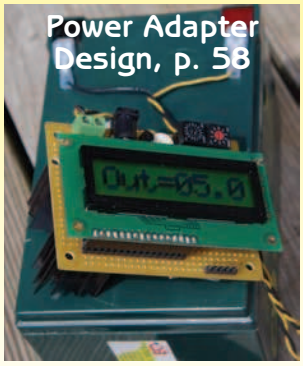

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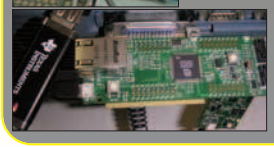

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GPIB Screen Saver
Sylvain Davaine
France

by Matt Oppenheim (United Kingdom)

PVDF Phased-Array Analog Front End

Need a board to test algorithms for CDMA signal transmission and processing? You can employ an array of broadband receivers using thin polyvinylidene fluoride (PVDF) sheets as the transducers. Here you learn about the analog electronics required to condition the analog signals for digitization and the subsequent transmission line implementation.

My supervisor appeared at the lab door pulling a large trolley. "This is the single-channel confabulator I made for my PhD," he beamed, showering a pile of valves, wires, and dust onto the floor. "Make it portable, battery-powered, and scale it up to eight channels," he instructed, disappearing behind the growing mound of antiquated technology. As he disappeared he muttered: "It's summer vacation, so I'm off for three months. Have fun!"

In this article, I present an implementation of an array of broadband acoustic receivers using thin polyvinylidene fluoride (PVDF) sheets as the transducers. The board is intended for testing algorithms used in code division multiple access (CDMA) signal transmission and processing. The final board is shown in Photo 1.

What is CDMA? Imagine that you are in a crowded room. Someone shouts loudly from one side to the other. You'll hear and understand him. But if several people start shouting, then the messages will become garbled. What if everyone else is whispering a different message at the same pitch, all together, all at the same time? Furthermore, if they are whispering in a language that you understand, and everyone else is talking in a foreign language, you will probably catch the faint message that you are interested in. Rather than dominate a single frequency, the signal is transmitted over a broad range of frequencies, but at very low amplitude. This means that regular narrow-band transmission is not interfered with by CDMA, nor does it block the signal.

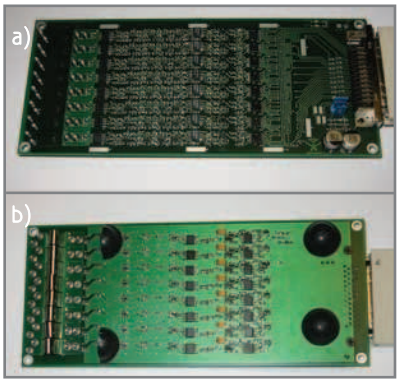

Photo 1—The eight-channel phased-array PVDF board. The top layer (a) houses the transducers. The bottom layer (b) houses most of the electronics and almost all of the analog circuitry. The board is four layers with a dedicated ground and power layer. All components are hand soldered!

This article focuses on the analog electronics required to condition the analog signals for digitization by a 16-bit analog-to-digital converter (ADC) and the subsequent transmission line implementation to enable communication with the processing platform. I'll cover design issues and board layout considerations. The board is being used by a fellow Lancaster University student, Mohammed Alloulah, for his PhD research pertaining to signal processing algorithms using an FPGA.

TRANSDUCERS

The PVDF sheets look and handle remarkably like a small piece of a Kit Kat wrapper, and that's precisely what I used for testing the film mounting. PVDF film is a piezoelectric material. When the film is hit with ultrasound in a frequency range of about 10 to 100 kHz, a tiny current of a few picoamps is produced by the film.

So how do you mount what is basically a conductive plastic film? If you try soldering on leads, you quickly end up with a melted puddle of smoking plastic. We tried using conductive epoxy to stick the film to PCB pads, but found that the supposedly conductive epoxy wasn't (conductive, that is, no matter what the can says).

The most reliable method we found is to sandwich the film between two PCBs—the main board and a clamp board. Slivers of conductive tape are placed between the PVDF film and the pads on the boards. Then the assembly is bolted together using M1.6 thread screws. Getting the film to curve into a hemi-cylindrical shape requires some geometry calculations so that the mounting pads are the correct distance apart for the film to curve naturally into the required shape.

Figure 1 shows the PVDF mounting arrangement. The channel spacing of 8 mm is a requirement of the signal-processing

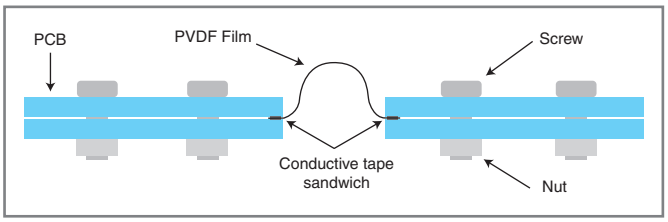

Figure 1—This is the PVDF mounting arrangement.[1] (Source: Mike Hazas)

algorithms implemented on the FPGA board that processes the final signals produced by the receiver board. These algorithms are beyond the scope of this article. The clamp PCBs are attached using two bolts, because with only one bolt they are free to rotate out of position.

ANALOG SIGNAL CONDITIONING

As you would expect, when the transducer produces a current, the first stage of the signal-conditioning chain is a current-to-voltage converter. With such a tiny current to amplify, the input current offset and bias of the op-amp are critical. I settled on the OPA129UB manufactured by Texas Instruments, which is billed as "ultra-low bias current." This is quoted as ±30 fA! The noise figure of any amplification chain depends critically on the first stage, so I used the best part that I could find.

You will notice the "T" arrangement of resistors in Figure 2 around the current-to-voltage converter. This allows much lower values of resistors to be used compared with using a single resistor. I needed the equivalent of at least a gigaohm and wanted to be able to try higher values. The disadvantage of this arrangement (nothing is free!) is that the offset voltage is amplified by the same factor by which you are reducing the equivalent single resistor. So long as this offset does not cause the output signal to approach the voltage rails, this is not a problem as the output voltage signal from the converter is decoupled through a capacitor, which eliminates the offset.

To give your tiny signal the best chance of survival, the layout of components and tracks for the input to this op-amp are critical. The pinout for the OPA129UB is optimized to allow for placing guard traces around the inputs. These guard traces are connected to the "substrate" pin of the amplifier at a single point, which is grounded. Normally, just having a ground plane under the traces is considered sufficient to guard the input lines from interference, but as the input signals are so tiny, I implemented the whole "belt and braces" approach of guard traces and ground plane. The guard traces are connected to the ground plane as close to each end of the traces as practical.

Next, the signal is filtered to remove unwanted high frequencies. Phase information is critical for the final signal processing. So a Bessel filter is used since this does not alter the

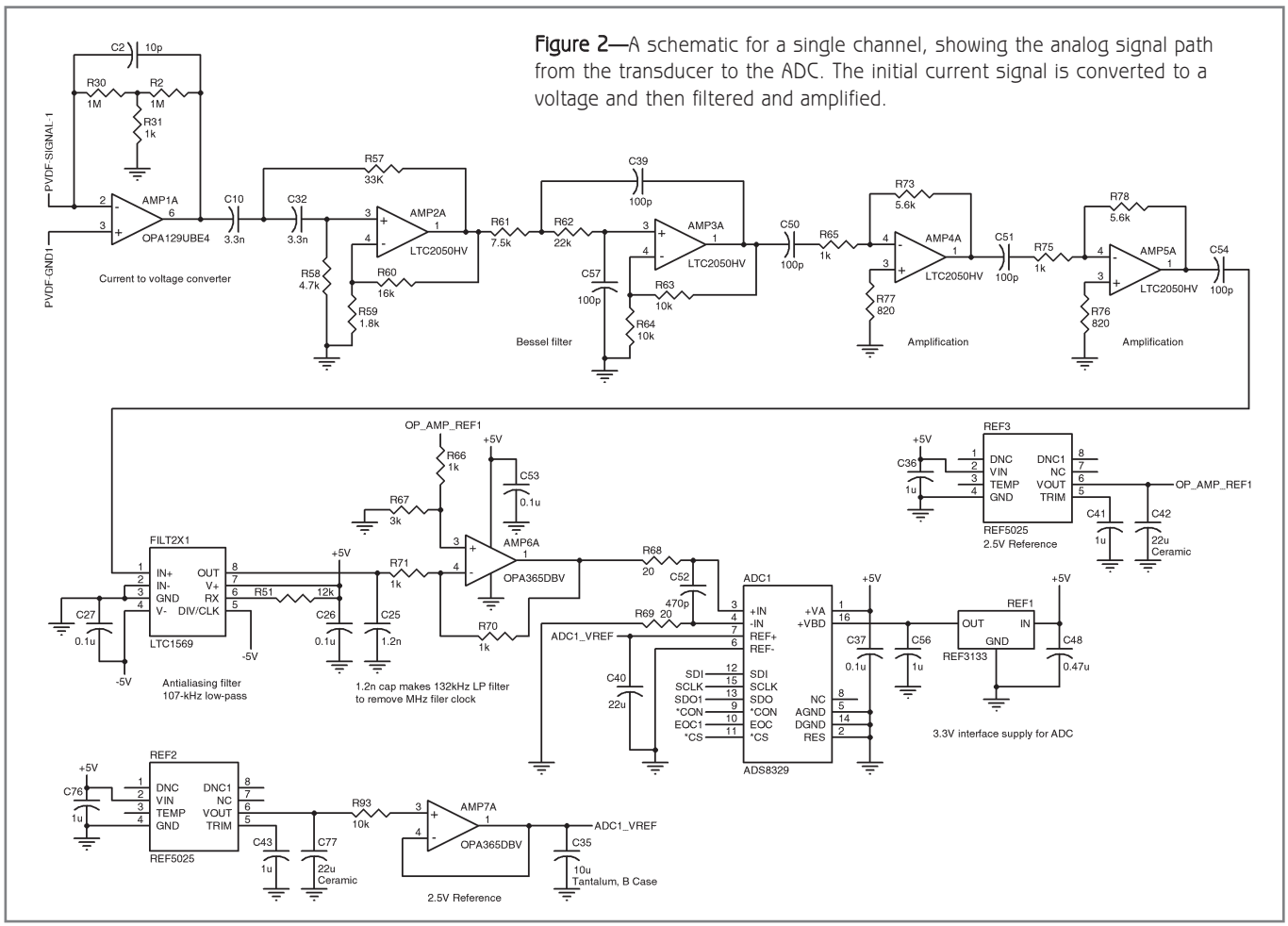

Figure 2—A schematic for a single channel, showing the analog signal path from the transducer to the ADC. The initial current signal is converted to a voltage and then filtered and amplified.

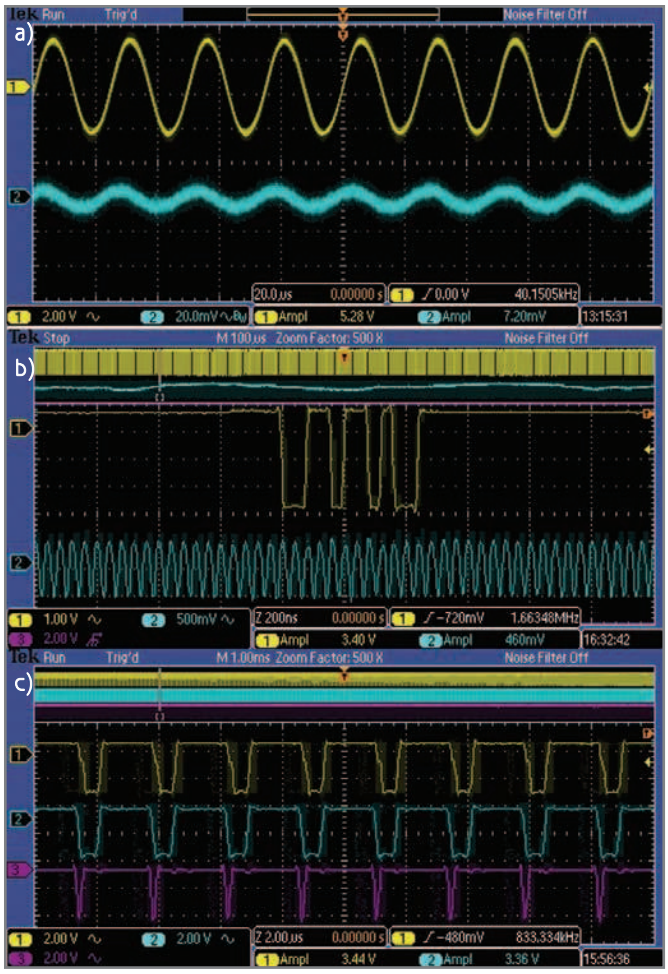

Photo 2—Oscilloscope screen grabs. a—Here you see the test signal after amplification and filtering with the signal immediately after the current-to-voltage conversion. b—This is SPI data from one of the ADCs alongside the SPI clock. c—These are SPI control signals (SDI, !CS, bottom !CON).

phase across the bandwidth of the signal. This is implemented using two Linear Technology LTC2050HV op-amps (AMP2A and AMP3A in Figure 2). Throughout the design, I used single op-amp packages for two reasons. The first was that there is a potential for cross-feed between the op-amp stages in a multiple package. The second was layout space restrictions. I needed each stage to fit into the 8-mm spacing of the PVDF films, which made for some tight routing! Still, it all worked out in the end. I used precision resistors throughout the filters to maintain consistent characteristics across the separate channels.

After the filtering are two stages of amplification (AMP5A and AMP6A in Figure 2). The original design had a single stage. Initial testing indicated that to get good signal amplitude for the following stages, the single stage might approach the gain-pass bandwidth limits of the op-amp. I could have stuck with a single stage and found an op-amp with a higher gain bandwidth, but I settled on staying with the op-amps I knew and having two stages of gain instead. It was a tradeoff, as it is always best to reduce the component count in a design to save space, power, and cost.

I used the classic inverting amplifier configuration since this reduces the component count compared to noninverting. With the noninverting configuration, the input needs to be tied to ground using a resistor; otherwise, the output can have a large voltage offset. To further eliminate the possibility of DC offset, I coupled the stages using a capacitor. I may seem a little paranoid, but what is an extra capacitor between friends? Having the capacitor between each stage also allows for the subsequent stages to be easily isolated during debugging: simply lift the capacitor with some desoldering tweezers (in the unlikely event that the circuit does not perform flawlessly first time).

Photo 2a shows the amplified and filtered output from the final op-amp stage and the output from the first op-amp—the current-to-voltage converter. Note that the amplitude scales differ by a factor of 100. The signals generated from the current-to-voltage converter are tiny! As can be seen, the op-amp amplification and filtering cleans up the signal nicely. The test signal was generated using a 40-kHz piezoelectric transducer connected to a function generator.

ANALOG-TO-DIGITAL CONVERSION

To provide further attenuation for out-of-band frequencies and to ensure that no aliasing occurs, a Linear Technology LTC1569 filter chip is configured as a low-pass filter. This is a versatile tenth-order filter chip in an eight-pin package. The filter cutoff frequency is set using a single external resistor. Refer to the datasheet for details. Linear Technology supplies its own free FilterCAD software to help you with filter design. Naturally, the results use their own range of filter components. C25 in Figure 2 removes the high-frequency (megahertz range) clock noise from the filter's output.

The analog-to-digital conversion circuitry was designed by Mohammed Alloulah in an attempt to limit the damage to his project because I designed the instrumentation that his future thesis depends on. A 16-bit Texas Instruments ADS8329 is used by each channel to convert the conditioned analog signal to digital. An ADC is only as good as the reference voltage used to compare your precious signal to, so a separate voltage-reference IC is used to produce the reference voltage for each ADC (REF2 in Figure 2). This reference voltage is further stabilized using a Texas Instruments OPA365 op-amp (AMP7A in Figure 2). This is implemented to overcome the transient noise that results from the loading effect taking place during conversion—an inherent effect from the architecture of the successive-approximation converter.

Details of this layout and configuration were worked out after spending a lot of time watching a man wearing a cowboy hat explaining the optimum design and layout configuration in Texas Instruments's educational online video series. Even the type and ESR rating of the capacitors that load the output from the reference have a measurable effect when working at 16-bit resolution (C35 in Figure 2). Basically, I copied their design and component recommendations!

The ADC only draws a small current. Since this is a 3-V part and the rest of the board uses ±5-V supply rails, a Texas Instruments REF3133 voltage reference powers each ADC. This adds a further layer of isolation between the ADC and the power supply circuitry. The part does not explicitly require a smoothing capacitor on the VOUT line, but I added

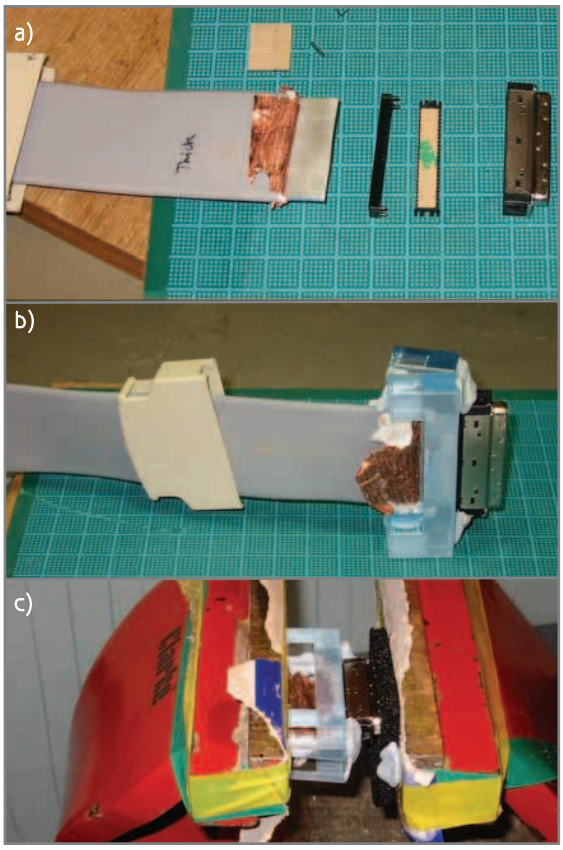

Photo 3—The transmission cable assembly. a—Take a look at the shielded ribbon cable and connector components. b—The connector is ready to press fit. c—I used a vise to press-fit the connector.

one for extra decoupling.

Photo 2b shows the digital data from one of the SPI lines. The lower trace shows a 25-MHz SPI clock signal. Due to the bandwidth limitation of the scope, this does not appear as a nice square wave. Photo 2c shows the other digital control signals for the ADCs generated by the FPGA. Because these are much lower frequency than the clock line, the scope has the bandwidth to display them as square waves.

DIGITAL INTERFACE

It's all analog under the skin! I wanted as fast an SPI as practical to connect the receiver board to a Xilinx Virtex II FPGA development board. Luckily, the communication science lab is adjacent to mine, so I was able to consult the professionals for advice on transmission-line design. As Robert Lacoste often mentions in his excellent "The Darker Side" column, it's all about impedance matching. I chose shielded ribbon cable for the transmission line as it is relatively straightforward to work with and butcher (I use that word accurately) into connectors. Also, I could order a single meter of this cable from my regular supplier, rather than having to purchase an entire reel.

Shielded cable is required, since unshielded cable with a 25-MHz signal pulsing along it acts like an antenna. I don't think the folks using the lab's indoor positioning systems would appreciate having to compete with a homemade transmitter!

With eight channels of SPI coming from the board, and timing control signals going into it, I needed a lot of signal lines. Naturally, I also needed to fit them all into a small enough footprint to not require widening the board since this would result in having to rethink the housing.

The 3M MDR range of connectors seemed suitable for the job as they have a small enough footprint for my board and all of the required genders of connectors are available from my usual online supplier. These connectors are available in both solder cup and insulation displacement connectors (IDC). IDC style has the advantage over solder cups of being much faster to assemble. Naturally, the manufacturer's recommended assembly tool cost a ridiculous amount of money. After carefully perusing the assembly instructions, I figured out a way to press fit all of the parts together using a vise, a pair of simple homemade jigs, and copious amounts of blue tack and insulation tape. I have put details of this assembly technique onto my website. Photo 3 shows the cable and connector being assembled. Photo 4 is the completed cable and connector. This method proved to be straightforward and reliable. I used the lab laser cutter to cut the 10-mm plastic jigs used to press-fit the assembly together. As always, no one was more surprised than I was when it all worked!

The only disadvantage of my cable assembly is that the shielded casing is not available for 50-way flat ribbon cable. I got around this by modifying the round cable-shielded casing with the judicious use of a hacksaw and file. The type of casing I wanted is made for just about any other width of cable!

From the datasheet, the characteristic impedance of the ribbon cable is 50 Ω. Signals originating from the ADC and going to the FPGA are impedance matched using a 50-Ω resistor. Signals coming from the FPGA to the ADC were terminated using a 50-Ω resistor in series with a 0.1-µF capacitor. The theory behind these termination techniques can be found in Ron Schmitt's 2002 book titled *Electromagnetics Explained*.

To eliminate cross-feed between the rapidly switching digital lines, I grounded a wire in between each signal wire on the ribbon cable. If the signals were differential, I would have used a twisted-pair configuration, but SPI signals are not differential.

I built a board that plugs onto the Xilinx development board to allow my cable to connect with the signal pins on the FPGA. This has impedance-matching resistors for the signals that originate from the FPGA going to my receiver board. Photo 4 shows the breakout board mounted on the Xilinx development board. Because all of the signals on the Xilinx board are digital, it is not necessary to add external shielding to this board to protect it from interference. However, having digital pins switching quickly acts as a transmitting antenna, so it would be necessary to case the board for a commercial product to comply with emission standards.

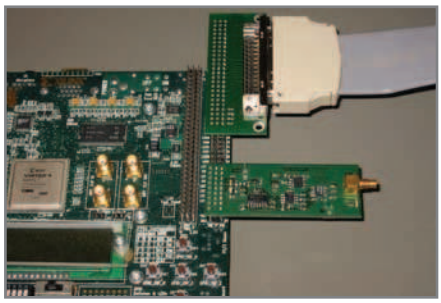

Photo 4—The breakout board and DAC

The output characteristics for the SPI clock line from the FPGA are critical for the interface to work. As always, read the datasheet carefully! We had to play around with the setting for the current limit of the pin to get life from the SPI bus.

CASING & PCB LAYOUT

I found a range of conductive plastic cases rated for EMC protection. The big advantage over using a metal case is the ease with which they can be machined. It's always a good idea to start looking at cases as early on as practical. The case dimensions and mounting arrangement act as major constraints on your PCB layout and dimensions.

I used CadSoft Computer's Eagle v5.6 for the schematic capture and PCB layout. I didn't touch the autorouter and don't advise anyone to do so. I used four layers with a layer dedicated to ground. Optimizing the ground return path is critical to analog design. I did not use separate analog and digital ground layers. I used a separate lobe of ground for each of the analog channels and connected them to a large unbroken area of ground under the digital connector using a neck placed under the ADCs.

I fit each channel into the width of the PVDF film transducer—8 mm. Routing is 90% component layout. It is a false economy to start laying down track until you have every part for the block that you are working on in an optimum position. This took some time, but like many engineers, I find PCB layout engrossing.

Once I had a single channel completed, I found a user language program (ULP) called "duplicate board" that allows a completed block of layout

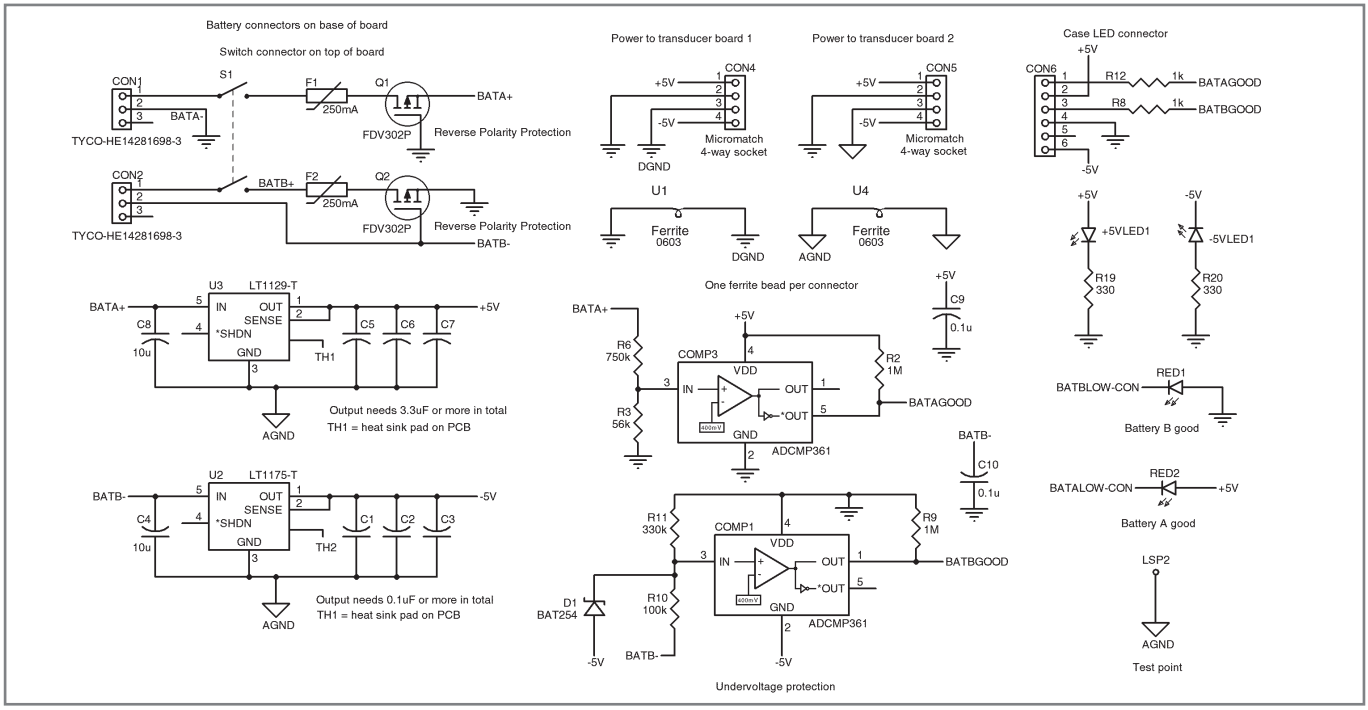

Figure 3—The schematic for the lithium battery power board (±5 V)

to be duplicated with a little fiddling. Look on the Eagle user group notice board for details.

DAC BOARD

We also designed a daughterboard for the FPGA board that enables the FPGA to produce an analog signal. This was originally designed to enable the testing of fancy transmission algorithms beyond the scope of this article. Here we used it for re-creating the test signals that are received by the receiver board as a quick check that everything works. Schematics and a board layout are also included on the *Circuit Cellar* FTP site.

POWER SUPPLY

Any ripple or noise on the power lines reduces the chances of maintaining signal resolution through the amplifier and filter stages and compromise the workable range of the 16-bit ADC. Rechargeable lithium batteries are chosen as the power source along with quality Linear Technology linear regulators to produce the ±5-V power rails. Using batteries has the strong advantage of producing an output free of high-frequency ripple.

I added some low-battery-voltage indicators using Analog Devices ADCMP361 comparators. These have a built-in voltage reference. Trying to work out how to hook one up to the negative supply battery and the –5-V output rail to indicate when the battery voltage was flagging took a little figuring!

Capacitance is your friend when it comes to smoothing the supply lines. Batteries can react in the kilohertz range to changes in load. Capacitors can react in the megahertz range. This means that a capacitor attached directly to the supply pins of each IC provides a little power supply adjacent to the chip that can react at the same frequency that the chip is operating at. Extra capacitors adjacent to the power board connectors on the main board further add to this decoupling of the battery supply from the instantaneous demands of the circuitry. At the relatively low frequencies that this board works, capacitor type and placement is not as critical as when working at high frequencies**.**

I initially used some ribbon cable IDC connectors to bring the power to the main board and doubled up on each pin in order not to exceed the maximum allowed current draw through the sockets. Although this particular set of connectors is excellent for digital signals, I went for a more robust and larger Tyco 0.1″ IDC connectors on the board revision, as they have much larger pins, which gives a tighter connection with a complete overkill of current rating. I checked that I could obtain the connectors from more than one local supplier. While you can often drop a replacement amplifier into a design without having to alter any of the layout, connectors are a pain to replace as they usually have a unique footprint. Figure 3 depicts the power supply's circuitry and layout.

BOARD SUCCESS

The board successfully amplified, filtered, and digitized the signals received by all eight transducers. Clamping the foils is excessively fiddly as it relies on an operator to accurately place the transducers. A more consistent system of transducer clamping needs to be found if the device is ever scaled up.

The transmission cable termination method proved affordable and reliable, showing I do not need to invest in the connector manufacturer's expensive crimping tools for low-volume production. I proved that it is possible to populate and hand-solder a ridiculously complex board. The cost to my sanity may have been excessive, though!

Author's note: MDR Cable assembly notes are available on my website: http://sites.google.com/site/hardwaremonkey/home/cable-assembly. Mohammed Alloulah made a substantial contribution to this design during his ongoing PhD research on signal processing, especially with filter design and ADC circuitry. I hope that the final circuit will contribute to his thesis.

Matt Oppenheim (matt.oppenheim@ gmail.com) holds an MSc in Mechatronic Systems Engineering from Lancaster University. He splits his time working offshore as a Chief Geophysicist for Polarcus onboard seismic survey ships and as a Research Assistant at InfoLab21, Lancaster University. Matt's first love is analog technology, but he can be persuaded to work on digital projects as well. In his spare time, Matt enjoys cycling and drawing cartoons.

PROJECT FILES

To download the project files, go to ftp://ftp.circuitcellar.com/pub/Circuit_Cellar/2010/244.

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