Ultralow Temperature On-chip Magnetic Refrigeration

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***Abstract*—Recent experiments have shown that adiabatic demagnetization refrigerators can be miniaturized and integrated with small electronic devices to reach on-chip electron temperatures below 1 mK [1]—[4]. Magnetic cooling with an external refrigeration stage can also achieve similar temperatures for samples with very low contact resistances [5]. Alongside the possibility of studying electronic properties of devices and materials in a new regime, the ability to cool far below 10 mK will have practical benefits for quantum technologies, metrological standards and sensors.**

On-chip magnetic cooling has so far been applied to a small range of devices. For the technique to become widely applicable, more work is needed to understand the heat flows between materials and the thermal subsystems at the micro- and nano-meter scale. On-chip cooling provides new ways to measure thermal properties such as electron-phonon coupling and boundary resistances [6]. Here we review the state-of-the-art in on-chip magnetic cooling and discuss recent progress towards making the technique more broadly applicable.

Keywords— Electronics cooling, miniature-scale refrigeration system, cryogenic electronics.

I. Introduction

It has been a longstanding challenge to reach electron temperatures below a few millikelvin in micro- and nano-scale devices and materials. Electrons in some bulk materials can be cooled to ~1 mK with advanced dilution refrigerators [7] and to microkelvin temperatures using additional demagnetization refrigeration [8]. However, the tiny heat capacity and poor thermal couplings of small electronic systems have made it challenging to reach on-chip electron temperatures even < 4 mK with the same techniques [9]—[12].

In recent work, it has been possible to significantly improve the thermal coupling between magnetic refrigerants and electronic devices so that sub-millikelvin, on-chip electron temperatures can now be achieved by magnetic cooling stages operating in a dilution refrigerator. The magnetic cooling can either be on-chip [6], off-chip [5] or both [2], [4]. In the demonstration of *off-chip* magnetic cooling [5], the sample is a 2D electron gas in a semiconductor chip. The chip is immersed in liquid ^{3}He to thermalise the electrical connections and the contact resistance of the device is very low (< 1 Ω) to provide effective cooling. In most examples of *on-chip* cooling to-date, the sample has been a Coulomb blockade thermometer (CBT) with high (~ kΩ) contact resistance and metal refrigerant integrated into the device structure. To help reach temperatures below 1 mK, the substrate and electrical contacts of the CBTs are also cooled by separate magnetic refrigeration stages [2], [4]. However, it is not clear whether cooling both the substrate and the contacts is necessary.

This paper summarises the practical implementation of on-chip magnetic cooling and recent results, outlines recent progress to develop a better understanding of on-chip heat flows and cooling at low- and sub-millikelvin temperatures, and discusses the challenge of making the technique more broadly applicable.

II. On-chip magnetic cooling

The basic principle of on-chip magnetic cooling is to incorporate a magnetic refrigerant, such as copper or indium, onto the surface of a device, and in close thermal contact with an electronic system of interest. When the refrigerant is a metal, a low-resistance electrical connection provides good thermal contact through electronic heat conduction.

Both the refrigerant and the cooled system need to be sufficiently isolated from their environment for the cooling power of the refrigerant to overcome any incoming heat. The dominant, intrinsic heat input will usually come from lattice vibrations. The strength of electron-phonon coupling typically depends on T^5 [13] and becomes extremely weak below ~ 10 mK. In this regime, the temperature of electrons in a material can effectively decouple from the temperature of phonons. This allows the temperature of an electronic system to be reduced by magnetic cooling while the temperature of its host lattice, and even the lattice of the magnetic refrigerant, can be at significantly higher temperatures.

A. Adiabatic demagnetization refrigeration

Demagnetization refrigeration is a single-shot cooling technique that works by manipulating the magnetic moments of electron or nuclear spins in a refrigerant material [14]. Initially, a large magnetic field B_i, typically ~ 10 T, is applied and the material is pre-cooled to a starting temperature T_i. For an appropriate choice of material and T_i, the entropy of the spin bath is significantly reduced. The magnetic field is then lowered to a final field B_f and, if the change is slow and the material is well isolated to make this process nearly isentropic, the temperature of the spin bath will reduce to a final temperature T_f. The temperature of conduction electrons and phonons in the material will be higher than the spin bath but they will still be cooled to some extent. In the case of a perfectly isentropic demagnetization, the final temperature of the spins is given by $T_f = T_i B_f / B_i$. In practice, T_f cannot be made arbitrarily small because the heat capacity of the spin bath would vanish. The choice of final field is often a trade-off between the lowest temperature achieved after demagnetization and the subsequent rate of warming.

B. Coulomb blockade thermometry

Most demonstrations of on-chip, demagnetization cooling to-date have incorporated a nuclear paramagnetic refrigerant, either copper or indium, into the structure of a Coulomb blockade thermometer. CBTs can be operated as primary or

TABLE I. SUMMARY OF REPORTED DEMONSTRATIONS OF ON-CHIP CBT MAGNETIC COOLING

CBT Type	Refrigeration scheme	B_i (T)	B_f (T)	T_i (mK)	T_f (mK)	T_{hold} (mK)	t_{hold}	Ref.
jCBT	On-chip (Cu)	5.0	0.1	≈ 9	4.5	< 5	1200 s	[1]
jCBT	On-chip (In)	12.8	0.04	≈ 16	3.2	< 4	~ 1 hour	[18]
gCBT	On-chip (Cu)	8.0	1.2	≈ 6	1.1	< 2	2000 s	[6]
jCBT	On-chip (Cu)	6.75	0.1	≈ 7	≤ 1.0	< 2	500 s	[6]
jCBT	On-chip (In) and off-chip (In & Cu)	12.0	0.1	13	0.42	< 0.7	85 hours	[2]
gCBT	On-chip (Cu) and off-chip (Cu)	9.0	≈ 0.05	≈ 9	0.22	< 0.3	27 hours	[4]

secondary thermometers of their internal electron temperature [15], [16]. They are typically sensitive over a ~ 1 decade range but, through variations in design, have been demonstrated to work below 1 mK [2], [4] and up to ≈ 60 K [17].

A CBT is formed by a chain of metal islands connected by tunnel junctions of ~ 10 kΩ resistance. It is common to connect many chains in parallel to reduce the total resistance of the CBT and improve accuracy. The capacitance of each island must be small enough so they begin to exhibit Coulomb blockade in the temperature range of interest. The blockade strengthens with decreasing temperature and can be overcome by an applied bias voltage. This leads to a temperature-dependent peak in resistance around zero bias. The width of the peak is a primary thermometer of electron temperature and its height is a secondary thermometer [15], [16].

To operate CBTs below 1 mK, it has been necessary to find ways to lower the island charging energy by increasing island capacitance. In a standard CBT, the capacitance of each island is dominated by the capacitance of its tunnel junctions. To increase capacitance, the islands are covered with a thin, dielectric material and a grounded metal gate. This design has been used to lower the operating temperature of a CBT into the microkelvin range [4], [6]. Because the island capacitance is dominated by the gate, the device has been called a "gate CBT" (gCBT) [6]. Conversely, a CBT where the junction capacitance dominates can be called a "junction CBT" (jCBT).

C. On-chip magnetic cooling results

Table 1 summarizes reported examples of magnetic cooling of CBTs obtained by different groups. The experiments use different CBT types (jCBT and gCBT), different refrigerant materials (copper and indium), and different refrigeration schemes (on-chip only or on-chip combined with some off-chip magnetic cooling).

Results in table 1 are obtained with a range of initial temperatures T_i and magnetic fields B_i depending on the experimental setup. The values of final temperature T_f are the lowest electron temperature measured immediately following demagnetization. The subsequent warm-up is characterized by a hold time t_{hold}, during which the electron temperature remains below the specified "hold temperature" T_{hold}. The choice of T_{hold} is somewhat arbitrary, but typically the warm-up is characterised by an extended period of slow change followed by an abrupt warming and so the hold time is not very sensitive to the exact value of T_{hold}.

Sub-millikelvin electron temperatures in table 1 are only conclusively demonstrated when on-chip magnetic cooling is combined off-chip magnetic cooling of the chip substrate and all electrical contacts using significant amounts (~mmol to ~mol) of off-chip refrigerant [2], [4]. Without this, it has not yet been possible to cool below 1 mK, even when a device is pre-cooled to ≈ 6 mK [6].

D. Thermal modelling of on-chip magnetic cooling

Reference [6] explores the limits of magnetic cooling with refrigerant only on-chip, and predicts flows of heat in this comparatively simple refrigeration scheme. In [6], the measured electron temperature T_e of two CBTs (one gCBT and one jCBT) during pre-cooling, demagnetization and warm-up is compared to a first-principles thermal model. The model predicts the dynamics of the thermal subsystems inside a single refrigerant island using theoretical expressions, literature values of material parameters, and measured values of the dilution fridge temperature T_{MXC}, which is assumed to be equal to the temperature of the sample holder T_h.

Two model parameters are determined by fitting to pre-cool data over ~ 100 ks: the total thermal boundary (Kapitza) resistance R_{pp} between the island phonons and the sample holder, and the background heat leak Q_0 into the island. The value of R_{pp} determines the initial rate of pre-cooling after magnetization to B_i. Conversely, Q_0 determines the saturation value of T_e after a long duration of pre-cooling. The fitted heat leak is $Q_0 = 0.1$ fW for both the jCBT and the gCBT. The fitted values of R_{pp} are 1.5×10^{-2} K^4m^2/W for the jCBT and 0.8×10^{-2} K^4m^2/W for the gCBT [6]. Both R_{pp} are consistent with literature values for multiple metal/semiconductor interfaces at the relevant temperature [19]. The factor of ≈ 2 difference between the R_{pp} values is consistent with the device structures: the gCBT islands are covered with a grounded metal gate, doubling the contact area with the T_h bath and roughly a halving of R_{pp}.

The demagnetization and warm-up of two CBTs is compared to the thermal model with no fitted parameters except those obtained from the pre-cool data [6]. The model reproduces the cooling and subsequent warm-up of both CBTs with good accuracy. The gCBT base temperature and hold time are correct to within 10%. The model also predicts the temperature of nuclear spins T_n and phonons T_p in the refrigerant, which are not measured in the experiment. The results suggest that electrons in the CBTs suddenly warm at the end of the hold time when incoming heat from phonons in the refrigerant overwhelms the electronic heat capacity. Phonon heating increases during the warm-up period because the fridge temperature rises by several millikelvin over ~ 1 ks during this time, likely a result of eddy-current heating during demagnetization.

Electron-phonon coupling is found to limit both the base temperature and the hold time: the difference between T_p and T_e is much more important than the value of R_{pp} in determining performance. Nonetheless, the extra gate on the gCBT, while helping to lower its operating range, is found to be detrimental to cooling because of the associated reduction in R_{pp}. The jCBT studied in similar conditions likely reached lower temperatures but this could not be confirmed because its operating range only extended down to ≈ 1 mK [6].

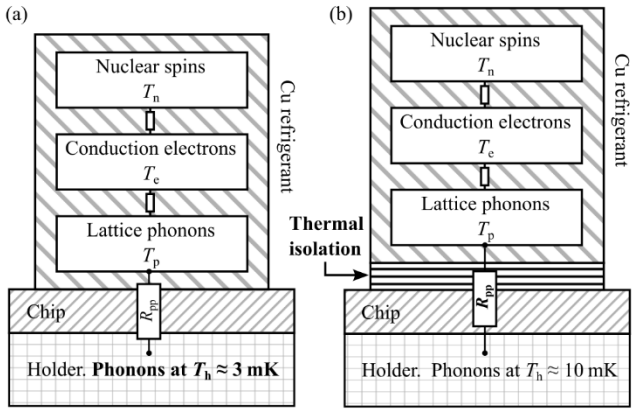

Fig. 1. Schematic device structures for on-chip magnetic cooling to sub-millikelvin electron temperature T_e. (a) and (b) show islands of magnetic refrigerant, typical volume ~10 nmol, on the surface of a chip. Adiabatic demagnetization reduces the temperature T_n of the nuclear spin bath, which is coupled to conduction electrons in the refrigerant. The dominant thermal coupling of the island is to the sample holder at temperature T_h, via the chip. The thermal resistance of this path R_{pp} is dominated by a series of thermal boundary resistances between different materials. For the devices studied in [6], it is predicted that temperatures significantly below 1 mK could be reached by either (a) cooling the sample holder to $T_h \leq 3$ mK, or (b) increasing the total thermal resistance R_{pp} between the island and the chip by two orders of magnitude.

Heating through electrical contacts is expected to be so low that it is neglected in the thermal model. It is predicted that the contact resistance could be as low as 50 Ω before significantly impacting performance, provided the contacts are kept at the base temperature of the dilution fridge [6].

E. Future developments

Thermal modelling of on-chip magnetic cooling, as described above, suggests two possible ways to reach sub-millikelvin electron temperatures without adding multiple, external refrigeration stages [6]. These possibilities are outlined in Fig. 1. The first, shown in Fig. 1(a), is to improve cooling of the sample holder to maintain a reasonably low phonon temperature ≤ 3 mK. This could be done by improving the resilience of the dilution refrigerator to changing magnetic fields or by adding one external demagnetization stage to cool the chip. A temperature $T_h = 3$ mK should be sufficient to maintain electron temperatures below 200 μK for ~ 10 ks using the CBTs in [6]. The second possibility, shown in Fig. 1(b), is to significantly increase the Kapitza resistance between the refrigerant and the chip. An increase of two orders of magnitude would allow the CBTs studied in [6] to reach electron temperatures below 1 mK, even if the chip holder can only be cooled to ≈ 10 mK. The value of R_{pp} could be increased by inserting multiple thin layers of different materials between the refrigerant and the chip, each contributing an additional thermal boundary resistance. The contact area of the refrigerant could also be decreased.

III. Conclusions

Multiple groups have used on-chip magnetic cooling to obtain low- and sub-millikelvin electron temperatures. The latter have only been reached in conjunction with bulk magnetic cooling of the chip and electrical contacts but thermal modelling suggests that better chip cooling alone may be sufficient. Improving thermal isolation by engineering higher thermal boundary resistances could also improve performance. Ultimately, applying magnetic cooling to arbitrary electronic devices will require careful design of the on-chip thermal environment, to physically separate the refrigerant and device while maintaining good mutual thermal contact and effective isolation from the warm environment.

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