Loop-Shaping Control Design for a New Modular Integrated On-Board EV Charger with RHP Zero Compensation

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Abstract

This paper presents the control design of a new modular integrated on-board charger (MIOBC) for electric vehicle (EV) applications. Unlike traditional EV systems with a single high-voltage (HV) battery, charger, and motor controller, the proposed MIOBC modularises both the battery and power converters, enhancing safety, controllability, and fault-ride-through (FRT) capability. Integrating the traction inverter with the on-board charger (OBC) reduces system size and weight while enabling seamless operation in three modes: charging, acceleration, and deceleration. The MIOBC employs single-stage Cuk-based converter topologies as submodules (SMs), which provide continuous input and output currents, handle a wide range of input voltages, and produce low electromagnetic interference (EMI). To address control challenges posed by right-half-plane (RHP) zeros in Cuk converters, loop-shaping techniques are applied using proportional-integral (PI), proportional-resonant (PR), and lead-lag compensators. These methods ensure sufficient phase margin (PM) and gain margin (GM) for robust, stable performance within the desired bandwidth (BW). This paper details the operating principles, controller design, and efficiency analysis. A 3 kW prototype was tested using Lancaster University's Formula Student (FS) racing car, demonstrating not only the robustness of the control strategy under partial faults in battery segments but also confirming the MIOBC system's ability to achieve a tested peak efficiency of 94.8% across a range of output powers.

1 Introduction

The worldwide measures towards reducing greenhouse gas emissions (GHGs), known to cause irreversible climate change, have increased interest in electric vehicles (EVs) as an alternative to internal combustion engine (ICE) cars in the transportation industry [1]. This will motivate the governments to invest more in the EV sector on both industrial and research levels [2].

The most common propulsion systems for EVs consist of a single high-voltage (HV) battery connected to a DC link, followed by a motor controller and an electric motor (DC or AC), as shown in Fig. 1a [3]. The motor controller, also known as the traction inverter, controls the power flow from the HV battery to the electric motor. Off-board or on-board battery chargers (OBCs) with unidirectional or bidirectional power flow can be used to charge the HV battery. The OBC system can charge EVs directly from the utility grid at a lower cost and complexity compared to the bulky and expensive off-board battery chargers [4, 5]. However, the limited space in EVs affects the power output of OBCs and the driving range of the vehicles. One practical solution is integrating the power electronics components from the propulsion system's traction inverter into the OBC, as shown in Fig. 1b. Such topology is known as "traction inverter-integrated OBC" and can improve the power density and efficiency of the OBC system.

The HV battery poses a significant challenge to the development of EVs and transition from ICEs due to several reasons [6]. As the primary source of propulsion energy for the EV, the HV battery contributes substantially to its bulk, volume, and cost. Moreover, it is the most hazardous component of EVs, requiring specialised personnel for maintenance, troubleshooting, and assembly procedures [7].

Most EV models, such as Mustang Mach-E, Polestar 2, Tesla Cybertruck, Mercedes-Benz EQC, and Audi e-tron GT, rely on a single HV battery box composed of multiple battery packs connected in series and parallel. Connecting many battery packs in series to increase total voltage can decrease the battery system's efficiency and significantly shorten its lifespan [7]. Discrepancies in cell composition

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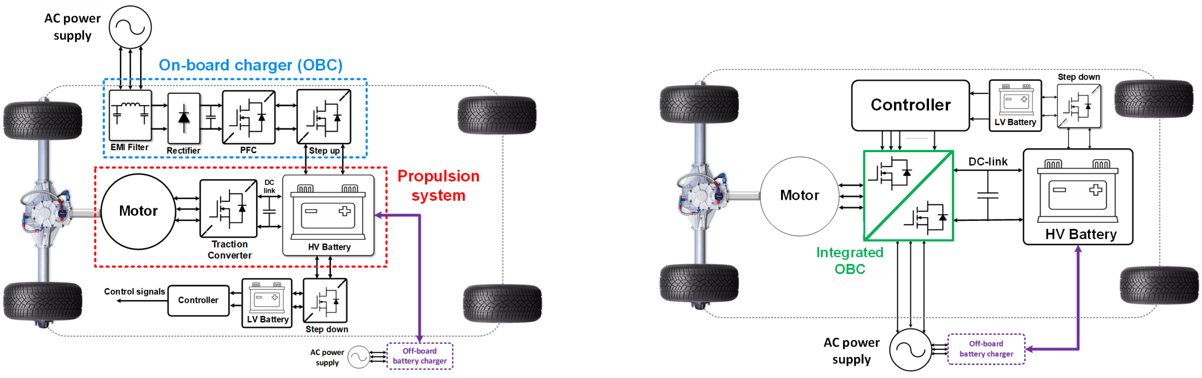


(a) Conventional OBCs

(b) Traction inverter-integrated OBCs

Figure 1: EV charging systems

and leakage currents among series-connected cells may lead to unequal voltage distribution and state of charge (SoC), thereby reducing the EV's potential range. Moreover, increasing the number and voltage of battery packs can pose potential hazards to maintenance personnel and users. However, from the electric motor's perspective, increasing the operating voltage to the range of 600 V-800 V is preferred. It enhances continuous power and accelerating torque while maintaining low motor current, reducing the size of power cables [6, 7].

Modularising the battery and power converter systems helps to decouple the battery voltage from the motor controller [8]. By dividing the HV battery into groups, each with a lower voltage, potential hazards are reduced, and fault ride-through (FRT) capability is enhanced. This modular approach allows for improved SoC monitoring and control, as each module is managed individually (see Fig. 2). If a fault occurs in one module, the Battery Management System (BMS) can isolate it, allowing the EV to continue operating at reduced power until repairs are made, thus increasing reliability and reducing customer concerns [9]. Additionally, modular power converters can operate at lower voltages and currents with higher switching frequencies, reducing stress on semiconductor devices and improving system efficiency by using components with lower on-resistance and forward voltages [10].

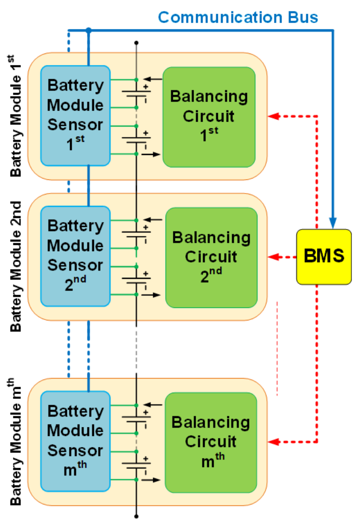


Figure 2: Modularised battery system with BMS

Non-isolated and isolated modular topologies have been reported in the literature, where the output sides of the power modules can be connected in parallel to increase the total power [11], [12, 13, 14, 15, 16, 17]. Interleave boost or buck-boost converter, dual-active-bride (DAB) converter, resonant DAB converter, and phase-shift full-bridge (PSFB) converter are the most common topologies used in modularised battery chargers [11], [13], [16, 17, 18].

The first attempt introduced the bidirectional interleaved buck-boost converter as the building block for high-power modular architecture for automotive applications [13]. This non-isolated system is suitable for modular DC-DC converters, and hence, it requires a second stage if an AC electric machine is used. Although interleaved topologies offer lower maintenance and cost, they suffer from current and voltage stresses on semiconductors. DAB converters, especially LLC resonant DABs, are the most popular topologies used in modularised structures for EV applications [16, 17, 18]. A three-phase modular converter rated at 10.5 kW is presented in [16], where several two-stage modules are connected in parallel per phase. The two-stage module comprises a diode rectifier for power factor correction (PFC) and a boost converter operating at 90 kHz. An isolated half-bridge LLC resonant converter with a diode bridge at the secondary side is used as the DC-DC stage. During charging, one side of the converter is connected to a single-phase AC voltage source while the other side is connected to the HV batteries. Although this modular topology offers high efficiency and less complexity, the presence of an output filter inductor has added to its overall size and weight. In addition, bidirectional power flow is not provided. In [17], a 20 kW modularised battery charger is presented, where the input side of the LLC resonant DAB converter is connected to the three-phase voltage through a three-phase boost PFC to increase the power density. A three-phase 22 kW converter is presented in [11], where each phase comprises a diode bridge and an interleaved boost converter. Two parallel-connected isolated full-bridge LLC converters with diode bridges at the secondary side are used in this topology in the DC-DC stage. However, uncontrollably large component tolerances in the two resonant tanks lead to unequal current sharing, among the primary issues with parallel LLC converters used in modular topologies. An efficient three-phase 22 kW modular single-stage topology is developed in [12]. Each phase of this topology is rated at 7.2 kW and is comprised of a full-bridge switch operated as a full-wave rectifier connected to an AC link followed by an isolated full-bridge DAB converter. High efficiency, high power density, and proper current sharing are among the advantages of this single-stage topology. However, when connected to the single-phase grid, an external power decoupling circuit is needed to absorb the second-harmonic component.

This paper introduces a new modular integrated on-board charger (MIOBC) system that integrates the traction inverter (motor drive) with the OBC to enhance power density, efficiency, and functionality. This integration allows the proposed MIOBC to operate seamlessly in three distinct modes: (i) charging (ii) driving (aaceleration), and (iii) regenerative braking (acceleration). The MIOBC employs single-stage Cuk-based converters as submodules (SMs), which offer several advantages over traditional two-stage topologies. These include continuous input and output currents, smooth operation, and reduced electromagnetic interference (EMI). Additionally, the single-stage design eliminates the need for a separate PFC stage and bulky DC-link capacitors, helping to meet the power density targets outlined by the U.S. Drive Partnership. To ensure safety and functionality, galvanic isolation is achieved through the integration of high-frequency transformers, in compliance with IEC 61851 safety standards for EV charging systems, which mandate isolation between the grid and the vehicle to prevent leakage currents and ensure user protection. A key challenge with Cuk-based converters is the presence of inherent right-half-plane (RHP) zeros, which complicate control design and stability. To address this, a loop-shaping control strategy has been developed. This strategy shapes the frequency response of the control system to meet specific performance criteria, including sufficient phase margin (PM), gain margin (GM), and desired bandwidth (BW). By carefully tuning the control loop, the proposed approach ensures precise dynamic behaviour across the three operating modes, even under partial faults in battery segments.

The rest of the paper is organised as follows: Section 2 provides a detailed description of the proposed MIOBC topology. The Cuk SM's modes of operations, namley inverter and rectifier operations, and small-signal AC analysis are presented in 3 and 4, respectively. The controller design for driving, braking, and charging modes, along with the loop-shaping techniques used to mitigate the challenges of RHP zeros, is presented in Section 5. The modulation strategy and the efficiency analysis of the proposed MIOBC are discussed in Section 6 and Section 7, respectively. Section 8 highlights the experimental validation, detailing the system's performance and fault tolerance across various modes. Finally, conclusions and future work directions are provided in Section 9.

2 MIOBC Topology

Fig. 3a illustrates the three-phase layout of the proposed MIOBC. The system employs single-stage isolated Cuk-based converter SMs shown in Fig. 3b as the power stage. The single-stage design of the Cuk SMs enhances power density by eliminating the need for a separate PFC stage and bulky DC-link capacitors. Additionally, the inclusion of two capacitors in series with the primary and secondary sides of the HF transformer blocks DC currents through the transformer. This design reduces transformer size while ensuring galvanic isolation. The HF transformer provides the necessary isolation to comply with

IEC 61851 safety standards, which mandate isolation between the grid and the EV to protect users and prevent leakage currents.

The integration of the traction inverter (motor drive) into the MIOBC further enhances functionality. This integration enables the MIOBC to operate in three distinct modes: (i) charging the battery cells, (ii) driving the permanent magnet synchronous motor (PMSM), and (iii) redirecting kinetic energy from the EV during regenerative braking back to the batteries. Transitions between these modes are managed using three-phase single-pole double-throw (SPDT) relays (SW_{abc}), which allow for smooth and efficient mode changes.

Each battery segment is connected to three Cuk-based SMs, one from each of the three phases (a, b, and c). This three-phase interconnection enables balanced power delivery and ensures that second-order (2ω) ripple components naturally cancel out. As a result, each battery segment receives smooth DC current without the need for additional filtering. A formal mathematical proof of this ripple cancellation is provided in the Appendix.

The total number of battery packs in the system is given by $n = p \times m$, where p denotes the number of battery packs connected in series within each segment (each consisting of c parallel-connected cells), and m represents the total number of battery segments in the system.

In the modular architecture, the Cuk SMs are connected in series to form the three-phase structure. Within each phase, the SMs collectively generate the required output currents and voltages. These three-phase currents $i_j(t)$ and voltages $v_j(t)$ are represented as follows:

$$\begin{cases} i_j(t) = I_o \sin(\omega t + \varphi_j + \gamma) \\ v_j(t) = \sum_{k=1}^{m} v_{o_{k_j}}(t) = V_o \sin(\omega t + \varphi_j + \delta) \end{cases} \tag{1}$$

, where $\varphi_j = \{0, -\frac{2\pi}{3}, \frac{2\pi}{3}\}$ and $k = 1 : m$. Here, $v_{o_{k_j}}$ represents the output voltage of the k^{th} SM in phase j, and δ, γ, and ω represents the phase angle, current angle, and angular frequency, respectively. $v_{o_{k_j}}$ itself represents the output voltage of the k^{th} SM in each phase and is calculated from:

$$v_{o_{k_j}} = \frac{v_j}{\sum_{k=1}^{m} V_{in_k}} V_{in_k} \tag{2}$$

The voltage of the k^{th} battery segment (V_{in_k}) and its nominal value ($V^*_{in_k}$) are calculated as:

$$\begin{cases} V_{in_k} = \sum_{i=1}^{p} V_{k_i} \\ V^*_{in_k} = p \times V^*_p \end{cases} \tag{3}$$

, where V^*_p denotes the nominal voltage of a single battery pack and depends on the SoC.

The output current of the k^{th} battery segment can be approximated as:

$$I_k \approx \frac{3 V_o I_o \cos(\delta - \gamma)}{2m V_{in_k} \eta_{SM}} \tag{4}$$

, with η_{SM} representing the efficiency of the Cuk SMs.

The modular design ensures independent control and operation for each phase, enabling FRT operation by isolating faulty segments while maintaining functionality in the remaining modules.

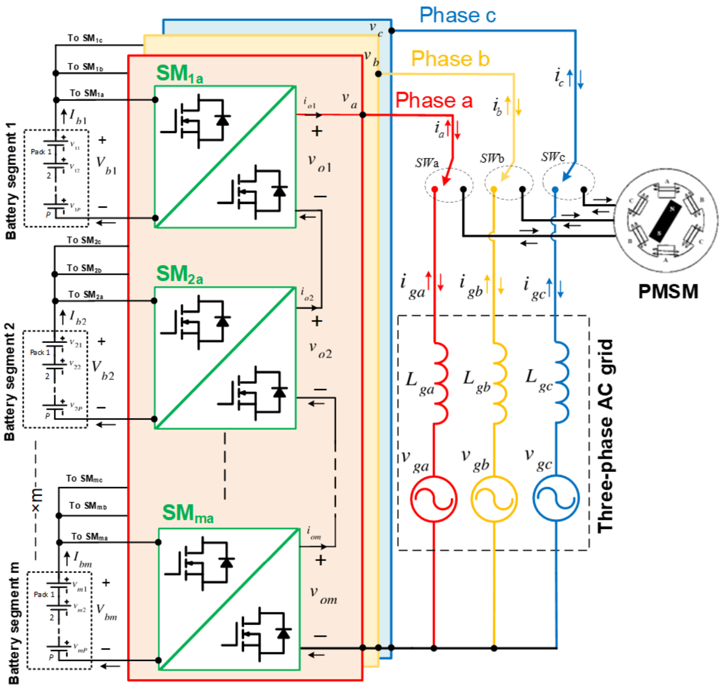
3 Cuk SMs' Modes of Operation

The operational principles of the Cuk-based SM in different operating modes are presented here. The proposed MIOBC can operate in both DC-AC inverter mode (when power flows from the EV batteries to the PMSM) and AC-DC rectifier mode (when the batteries are charged from the AC grid or during regenerative braking).

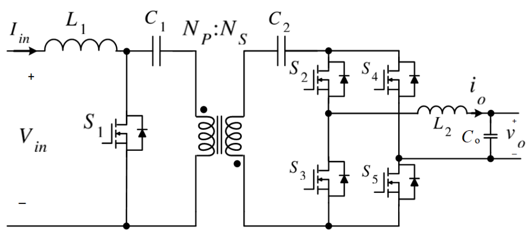
3.1 Inverter Operation

As a DC-AC inverter, the SM converts the constant DC power from the batteries to the variable voltage and frequency AC power suitable for driving the PMSM.

Fig. 4 depicts the switching operation of the Cuk-based SM inverter in the positive half-cycle of the output voltage v_o. The parameters defining the switching and activation times are denoted as t_s and t_{ON}, respectively. In Fig. 4a, switches S_1, S_2, and S_5 are in the ON-state within the time interval ($0 \leq t < t_{\mathrm{ON}}$). This results in a drop in the capacitor voltages v_{C_1} and v_{C_2}, accompanied by a rise in



(a) Three-phase layout



(b) Single-stage isolated Cuk-based SM

Figure 3: The proposed MIOBC

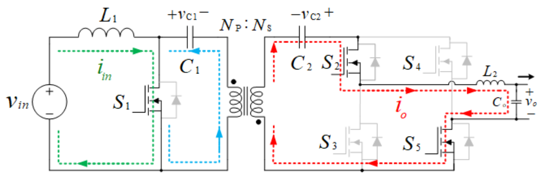
the input current i_{in} and output current i_o. Moving forward to Fig. 4b, all switches except S_5 are in the OFF-state within the time interval $(t_{\mathrm{ON}} \leq t < t_s)$. This leads to a decrease in both i_{in} and i_o, while v_{C_1} and v_{C_2} experience an increase. The main waveforms of the SM during these three states are illustrated in Fig. 4c, with $N = N_s/N_p$ being the turns ratio of the HF transformer.

For the negative half-cycle of v_o, switches S_3 and S_4 are in the ON-state instead of S_2 and S_5 to charge the inductors L_1 and L_2. In the second interval, all the switches except S_3 are in the OFF-state within the time interval $(t_{\mathrm{ON}} \leq t < t_s)$, discharging L_1 and L_2 into C_1 and C_2, and the output capacitor C_o.

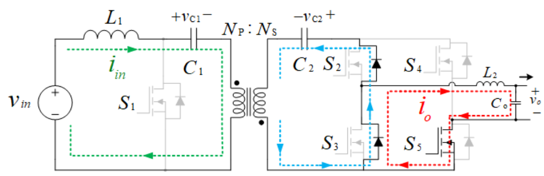
3.2 Rectifier Operation

Fig. 5 shows the rectifier operation of the SM when the battery packs are charged from the AC grid or the PMSM (now operating as a permanent magnet synchronous generator (PMSG)). During regenerative braking, the SM converter acts as an AC-DC rectifier. It captures the kinetic energy generated during braking and converts it into DC power, which is then fed back into the batteries. In the charging mode, the SM converter functions as an AC-DC rectifier as well, converting the AC power from the mains supply into DC power suitable for charging the batteries.

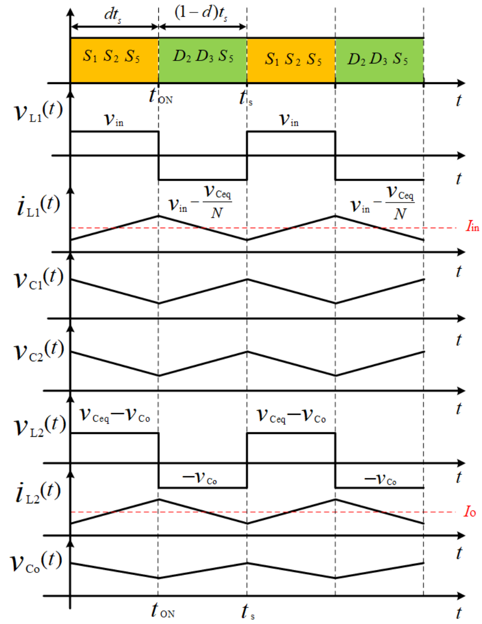
As can be seen in Fig. 5, the input and output currents i_{in} and i_o reverse their normal direction when the Cuk SM is operating as a rectifier. In Fig. 5a, where $(0 \leq t < t_{\mathrm{ON}})$ and v_o is positive, S_2 and S_3 are in ON-state. As a result, C_1 and C_2 discharge into L_1, increasing i_{in}. The inductor L_2 is also being charged by C_o, increasing i_o. During $(t_{\mathrm{ON}} \leq t < t_s)$, all switches are in the OFF-state as shown in Fig. 5b. This results in i_{in} and i_o decreasing, while the voltages v_{C_1} and v_{C_2} increase. The main waveforms of the SM during these three states are illustrated in Fig. 5c.



(a) ON-state (t_{ON})



(b) OFF-state ($t_{\mathrm{OFF}} = t_s - t_{\mathrm{ON}}$)



(c) Key waveforms for the positive half-cycle

Figure 4: Inverter operation of the Cuk-based SM in the positive half-cycle $v_o > 0$

For the negative half-cycle of v_o, switches S_4 and S_5 are in the ON-state instead of S_2 and S_3, where $(0 \leq t < t_{\mathrm{ON}})$. In the second interval, where $(t_{\mathrm{ON}} \leq t < t_s)$, the current closes its path through the diodes D_3 and D_4 in the secondary side to L_2 into the capacitors C_1 and C_2.

4 Small-signal AC analysis

The dynamic behaviour of the Cuk converter can be accurately modelled using the state-space representation. Small-signal AC analysis further refines this model by linearising the system around its operating point. It enables deriving the transfer functions required for designing the necessary control loops for the efficient operation of the MIOBC topology.

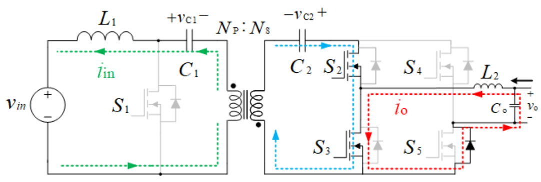
Fig. 6 illustrates the equivalent circuits of the Cuk-based SM during its ON and OFF states. The voltages across the two capacitors C_1 and C_2 increase and decrease simultaneously. Therefore, they can be considered as a single state. The equivalent capacitor C_{eq} and its voltage $v_{C_{eq}}$ are defined as:

$$\begin{cases} C_{eq} = \dfrac{C_1 C_2}{C_1 + N^2 C_2} \\ v_{C_{eq}}(t) = N v_{C_1}(t) + v_{C_2}(t) \end{cases} \tag{5}$$

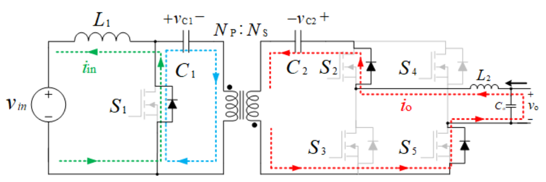
This simplifies the analysis and control design of the Cuk converter by reducing the number of states that need to be considered. In addition, an ideal transformer was used in the equivalent circuits of the Cuk SMs primarily to simplify the analysis of the transfer functions.

The presence of equivalent series resistances (ESRs) in Fig. 6 affects the overall efficiency of the converter and must be taken into consideration. ESR_1, ESR_2, and ESR_o are the ESRs associated with the passive components L_1, L_2, C_{eq}, and C_o, respectively.

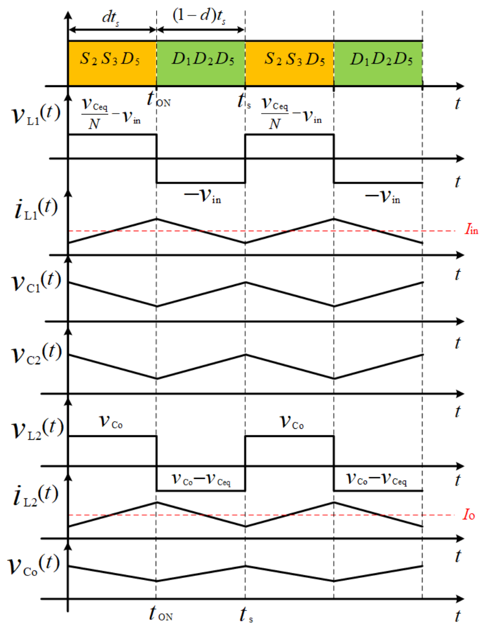
The state-space representation for the Cuk-based SM for each switching state (i = ON, OFF) is expressed as follows:



(a) ON-state (t_{ON})

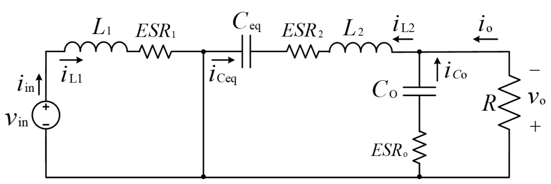


(b) OFF-state ($t_{OFF} = t_s - t_{ON}$)

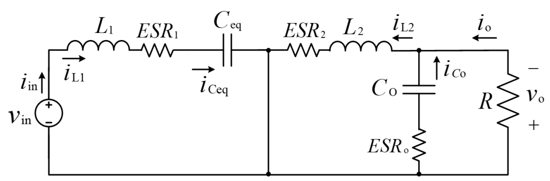


(c) Key waveforms for the positive half-cycle

Figure 5: Rectifier operation of the Cuk-based SM in the positive half-cycle $v_o > 0$



(a) ON-state (t_{ON})



(b) OFF-state ($t_{OFF} = t_s - t_{ON}$)

Figure 6: Equivalent circuits of the Cuk SM

$$\dot{x}(t) = A_i x(t) + B_i u(t), \qquad y(t) = C_i x(t) \tag{6}$$

where $x(t)$, $u(t)$, and $y(t)$ are the state, input, and output vectors, respectively.

Let R' and R'' be defined as:

$$\begin{cases} R' := ESR_o\, R + ESR_2\, R + ESR_2\, ESR_o, \\ R'' := R + ESR_o. \end{cases} \tag{7}$$

The state vector is defined as:

$$x(t) = \begin{bmatrix} i_{L_1}(t) & v_{C_{eq}}(t) & i_{L_2}(t) & v_{C_o}(t) \end{bmatrix}^{\mathrm{T}}. \tag{8}$$

In the proposed MIOBC, each SM features two primary ports, denoted as v_{in} and v_o, which are connected respectively to the battery segment and to the grid or motor-side circuit, depending on the operating mode. For traction or discharging operation (battery powering the motor or grid), v_{in} serves as the input port (battery segment voltage), while v_o is the output port (supplying inverte or grid interface). Conversely, during charging operation (grid or charger replenishing the battery), v_o functions as the input port (receiving power from the grid or external charger), and v_{in} is the output port (charging the battery segment). For consistency and without loss of generality, the following state-space analysis defines the input vector as $u(t) = v_{in}(t)$ and the output as $y(t) = v_o(t)$, where $v_o(t)$ is the output voltage across the load terminals (including the effect of ESR_o), extracted from the state vector as:

$$v_o(t) = C_i x(t) = \frac{ESR_o R}{R''} i_{L_2}(t) + \frac{R}{R''} v_{C_o}(t) \tag{9}$$

The system, input, and output matrices A_i, B_i, and C_i are given by:

$$A_{\mathrm{ON}} = \begin{bmatrix} \frac{-ESR_1}{L_1} & 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{C_{eq}} & 0 \\ 0 & \frac{1}{L_2} & \frac{-R'}{L_2 R''} & \frac{-R}{L_2 R''} \\ 0 & 0 & \frac{R}{C_o R''} & \frac{-1}{C_o R''} \end{bmatrix} \tag{10}$$

$$B_{\mathrm{ON}} = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{11}$$

$$C_{\mathrm{ON}} = \begin{bmatrix} 0 & 0 & \frac{ESR_o R}{R''} & \frac{R}{R''} \end{bmatrix} \tag{12}$$

$$A_{\mathrm{OFF}} = \begin{bmatrix} \frac{-ESR_1}{L_1} & \frac{-1}{L_1} & 0 & 0 \\ \frac{1}{C_{eq}} & 0 & 0 & 0 \\ 0 & 0 & \frac{-R'}{L_2 R''} & \frac{-R}{L_2 R''} \\ 0 & 0 & \frac{R}{C_o R''} & \frac{-1}{C_o R''} \end{bmatrix} \tag{13}$$

$$B_{\mathrm{OFF}} = B_{\mathrm{ON}} \tag{14}$$

$$C_{\mathrm{OFF}} = C_{\mathrm{ON}} \tag{15}$$

Under the small-signal AC assumption, the line-to-control transfer function $G_d(s)$, which describes the relationship between small variations in the duty cycle ratio $d(t)$ and the resulting small variations in the output voltage $v_o(t)$, is derived as shown in Eq. (20). The derivation of $G_d(s)$ begins with the continuous-time state-space representation of the converter in both ON and OFF switching states. These are defined by matrices $A_{\mathrm{ON}}, B_{\mathrm{ON}}, C_{\mathrm{ON}}$ and $A_{\mathrm{OFF}}, B_{\mathrm{OFF}}, C_{\mathrm{OFF}}$, respectively, as presented in Eqs. (10)–(15). To obtain a unified dynamic model over a complete switching cycle, the system matrices are averaged using the nominal steady-state duty cycle D, based on the state-space averaging technique [19]:

$$\begin{cases} A_{\mathrm{avg}} = D \cdot A_{\mathrm{ON}} + (1 - D) \cdot A_{\mathrm{OFF}}, \\ B_{\mathrm{avg}} = D \cdot B_{\mathrm{ON}} + (1 - D) \cdot B_{\mathrm{OFF}}, \end{cases} \tag{16}$$

where A_{avg} and B_{avg} are the duty-cycle-averaged system and input matrices. Introducing small perturbations $x(t) = X + \tilde{x}(t)$, $u(t) = U + \tilde{u}(t)$, and $d(t) = D + \tilde{d}(t)$ about the steady-state (X, U, D), and linearizing with respect to the duty cycle, the small-signal model becomes:

$$\begin{aligned} \frac{d\tilde{x}(t)}{dt} &= A_{\mathrm{avg}}\, \tilde{x}(t) + B_{\mathrm{avg}}\, \tilde{u}(t) \\ &\quad + \left[\frac{\partial A_{\mathrm{avg}}}{\partial d}\bigg|_{X,U,D} X + \frac{\partial B_{\mathrm{avg}}}{\partial d}\bigg|_{X,U,D} U \right] \tilde{d}(t) \end{aligned} \tag{17}$$

Here, the derivatives with respect to the duty cycle are given by $\frac{\partial A_{\text{avg}}}{\partial d} = A_{\text{ON}} - A_{\text{OFF}}$ and $\frac{\partial B_{\text{avg}}}{\partial d} = B_{\text{ON}} - B_{\text{OFF}}$, in accordance with the state-space averaging method [19]. The term in brackets captures the system's sensitivity to variations in duty cycle, with all derivatives evaluated at the DC operating point. $X = [I_{L_1}, V_{C_{eq}}, I_{L_2}, V_{C_o}]^{\text{T}}$ and U are the steady-state values of the state and input vectors, respectively, as determined by solving the large-signal equations of the converter for the specified duty cycle D, input voltage V_{in}, and load R. Specifically, I_{L_1} and I_{L_2} are the DC inductor currents, and $V_{C_{eq}}$ and V_{C_o} are the DC capacitor voltages at steady state. The output equation is similarly linearized as $\tilde{y}(t) = C_{\text{ON}}\tilde{x}(t)$. Applying the Laplace transform, the transfer function from duty cycle perturbation to output voltage is:

$$\begin{aligned} G_d(s) = \frac{\tilde{v}_o(s)}{\tilde{d}(s)} &= C_{\text{ON}} \left(sI - A_{\text{avg}}\right)^{-1} \\ &\times \left[\left.\frac{\partial A_{\text{avg}}}{\partial d}\right|_{X,U,D} X + \left.\frac{\partial B_{\text{avg}}}{\partial d}\right|_{X,U,D} U \right] \end{aligned} \tag{18}$$

This formulation makes explicit that the coefficients in $G_d(s)$ are determined by evaluating the derivatives of the averaged matrices at the steady-state operating point, in accordance with the standard small-signal modelling methodology for power converters [20].

It should be noted that the small-signal transfer function from duty cycle to output voltage, $G_d(s)$, is extracted using the output matrix C_{ON} in (12). To obtain the small-signal transfer function from duty cycle to output current, $G_{di}(s) = \tilde{i}_o(s)/\tilde{d}(s)$, the same state-space framework can be utilized with the output matrix redefined as

$$C_{i,\text{ON}} = \begin{bmatrix} 0 & 0 & \frac{ESR_o}{R''} & \frac{1}{R''} \end{bmatrix} \tag{19}$$

There are two right-half-plane (RHP) zeros and one left-half-plane (LHP) zero in the Cuk-based SM's transfer function $G_d(s)$ in (20). The LHP zero can be disregarded since its frequency is substantially higher than both the LHP poles and the RHP zeros. By neglecting this LHP zero, the complexity of the loop-shaping control design process can be reduced without sacrificing system stability or performance. The value of the output capacitor C_o is also deliberately chosen to be substantially smaller than that of other passive components due to the inherently low output ripple current of the Cuk converter. Consequently, the pole associated with the capacitor C_o in the denominator of the transfer function $G_d(s)$ can also be neglected. Such simplifications further simplify the control design process without compromising its accuracy.

$$\begin{aligned} G_d(s) = \frac{\tilde{v}_o(s)}{\tilde{d}(s)} &= \frac{-RR''\left(1 + s(C_o ESR_o)\right)}{\Delta} \cdot \\ &\Big[-s^2\left(V_{C_{eq}} C_{eq} L_1\right) + s\Big(DL_1(I_{L_1} + I_{L_2}) - C_{eq} ESR_1 V_{C_o}\Big) - V_{C_{eq}} D(1-D) - V_{C_o}(1-D) + ESR_1 D(I_{L_1} + I_{L_2}) \Big] \end{aligned} \tag{20}$$

$$\begin{aligned} \Delta := {} & s^4\Big[C_{eq} C_o L_1 L_2 \left(R''\right)^2\Big] + s^3\Big[C_{eq} C_o ESR_1 L_2 \left(R''\right)^2 + C_{eq} L_1 L_2 R'' + C_{eq} C_o L_1 R'' R'\Big] \\ & + s^2\Big[C_o L_2 \left(R''\right)^2 (1-D)^2 + C_o L_1 D^2 \left(R''\right)^2 + C_{eq} ESR_1 R''(L_2 + C_o)R' + C_{eq} L_1 (R^2 + R')\Big] \\ & + s\Big[L_2 R''(1-D)^2 + C_{eq} ESR_1 (R^2 + R') + C_o ESR_1 D^2 \left(R''\right)^2 + L_1 D^2 R'' + C_{eq} R'' R'(1-D)^2\Big] \\ & + (1-D)^2 R' + R^2(1-D)^2 + ESR_1 D^2 R''. \end{aligned} \tag{21}$$

Therefore, $G_d(s)$ can be simplified as:

$$\begin{aligned} G_d(s) &\cong G_{d_o} \frac{(1 - \frac{s}{\omega_{Z_1}})(1 - \frac{s}{\omega_{Z_2}})}{(1 + \frac{s}{\omega_{P_1}})(1 + \frac{s}{\omega_{P_2}})(1 + \frac{s}{\omega_{P_3}})} \\ &\cong G_{d_o} \frac{k_d(s - \omega_{Z_1})(s - \omega_{Z_2})}{(s + \omega_{P_1})(s + \omega_{P_2})(s + \omega_{P_3})} \end{aligned} \tag{22}$$

where the gain at low frequencies is defined by $G_{d_o} = {V_o}^2/V_{in}$.

The dominant zeros ω_{Z_1} and ω_{Z_2} in Eq. (22) correspond to the roots of the cubic numerator polynomial $N(s)$ of Eq. (20):

$$\begin{aligned} N(s) = & -RR''\,(1 + sC_oESR_o)\Big[-s^2(V_{C_{eq}}C_{eq}L_1) \\ & + s\,(DL_1(I_{L_1}+I_{L_2}) - C_{eq}ESR_1V_{C_o}) - V_{C_o}(1-D) \\ & - V_{C_{eq}}D(1-D) + ESR_1D(I_{L_1}+I_{L_2})\Big] \end{aligned} \tag{23}$$

Expanding this, the numerator becomes a cubic polynomial in s:

$$N(s) = \alpha_3 s^3 + \alpha_2 s^2 + \alpha_1 s + \alpha_0 \tag{24}$$

After neglecting the highest-frequency LHP zero (as discussed above), these dominant zeros can be well approximated as the roots of the reduced quadratic:

$$\omega_{Z_{1,2}} = \frac{-\alpha_1 \pm \sqrt{\alpha_1^2 - 4\alpha_2\alpha_0}}{2\alpha_2} \tag{25}$$

The coefficients α_2, α_1, and α_0 are functions of the converter's inductances, capacitances, ESRs, duty cycle D, and the DC steady-state values of the state variables.

Similarly, the poles ω_{P_1}, ω_{P_2}, and ω_{P_3} are the roots of the cubic denominator polynomial:

$$\Delta(s) \approx \beta_3 s^3 + \beta_2 s^2 + \beta_1 s + \beta_0, \tag{26}$$

where the coefficients β_i can be extracted from Eq. (19) and are likewise functions of the converter's parameters and operating point. These roots determine the system's dynamic response and may be computed analytically or numerically.

A generic Bode plot of the transfer function $G_d(s)$ linearised around $D = 0.5$ is displayed in Fig. 7. One notable characteristic observed in the Bode plot of $G_d(s)$ is the zero-pole cancellation phenomenon at high frequencies. This causes the gain of the transfer function to decrease by 20 dB per decade beyond the cut-off frequency f_c, rather than the steeper roll-off that would be expected in the absence of this cancellation. This effect can be mathematically understood from the transfer function structure, where a closely spaced zero and pole at high frequency simplify the system's frequency response:

$$\frac{s - \omega_Z}{s - \omega_P} \approx 1 \qquad \text{when} \quad \omega_Z \approx \omega_P \tag{27}$$

Despite this simplification in the gain response, the phase behaviour remains fundamentally altered by the presence of two RHP zeros and three LHP poles. Each RHP zero introduces a phase lag of $-90°$, and each LHP pole also contributes $-90°$, so the cumulative phase shift theoretically approaches $-450°$ at high frequencies:

$$\text{Phase lag at high frequency: } 2 \times (-90°) + 3 \times (-90°) = -450° \tag{28}$$

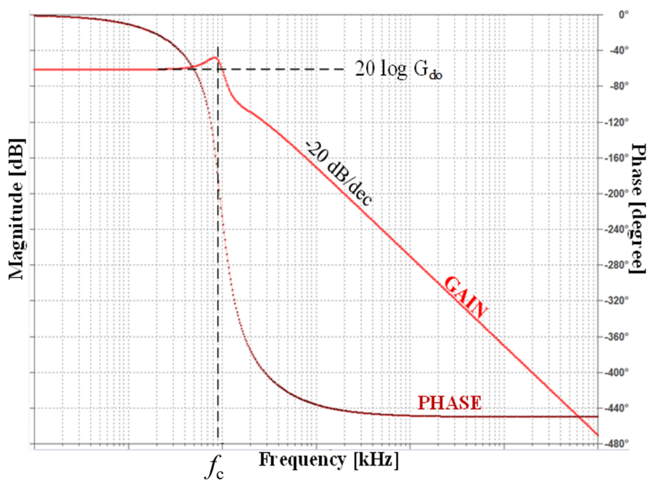


Figure 7: A generic Bode plot of the small-signal transfer function $G_d(s)$

Such complex phase behaviour can significantly complicate control design, especially where PM and stability are critical considerations. To address these challenges, strategies such as loop-shaping, phase compensation, and the use of lead-lag compensators are implemented in this paper to restore phase margin and ensure robust closed-loop stability.

5 Control Strategy for MIOBC Operation

Fig. 8 illustrates the configuration of the EV equipped with acceleration, charging, and regenerative braking modes. In acceleration or driving mode (red arrows), the electrical power flows from the HV battery box to the motor to drive the vehicle. In the regenerative braking mode (blue arrows), the motor operates as a generator to convert kinetic energy into electrical energy during deceleration or braking. This electrical energy is then fed back to the HV battery box for storage. In the charging mode (brown arrows), the power flow is from the AC grid to the HV batteries.

To regulate the operation of the proposed MIOBC topology, two distinct control systems are presented:

1. **Driving/Braking mode controller:** This controller generates the appropriate stator voltages for the PMSM, enabling the EV to achieve the desired velocity profile in both driving and braking modes.

2. **Charging mode controller:** When the AC grid is connected to the outputs of the series-connected SMs for charging the batteries, this controller is activated. It controls the charging current, ensuring efficient and safe power transfer from the AC grid to the battery packs.

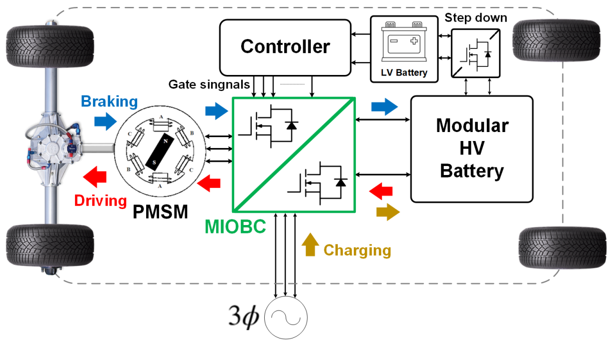


Figure 8: EV equipped with driving, charging, and regenerative braking modes

The following subsections outline the two controllers and detail the key steps for fine-tuning their gains using the loop-shaping technique. This methodology is crucial for optimising the control system's performance, ensuring responsiveness, precision, and stability in regulating the MIOBC's operation across its various modes.

5.1 Control Design for Driving and Braking Modes (DRBR Controller)

Fig. 9 illustrates the block diagram of the DRBR controller. This controller uses the reference velocity profile v^* as an input and generates the appropriate stator voltages for the PMSM, managing the operation of the EV during acceleration, constant speed, and regenerative braking (deceleration). The EV gradually accelerates from zero to its maximum speed during the period t_a. Subsequently, during t_c, the EV maintains its speed at the maximum steady level. Finally, the regenerative braking mode is activated during t_d, allowing the EV to decelerate while simultaneously returning kinetic energy to the battery cells.

As shown in Fig. 9, the outer-loop PI controller $G_{pi\omega}(s)$ compares the desired mechanical speed ${\omega_m}^*$ with the actual speed of the PMSM. Any discrepancy between the two speeds generates a speed error, which is then used by the controller to adjust the desired electromagnetic torque ${T_e}^*$ accordingly. Given the relationship between the electromagnetic torque T_e and the q-axis current I_q for a PMSM, the desired value of this current I_q^* is extracted as:

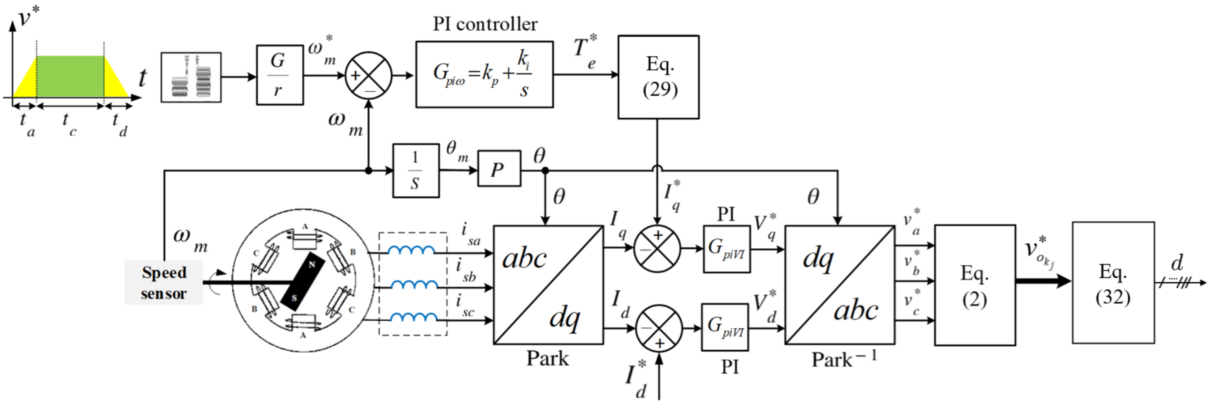


Figure 9: DRBR controller

$$I_q^* = \frac{4}{3P}\left(\frac{T_e{}^*}{\phi_r}\right), \tag{29}$$

where ϕ_r is the rotor magnetic flux linkage (in Wb) and P is the number of pole pairs of the PMSM. In this control scheme, the reference component on the d-axis of the stator current $I_d{}^*$ is maintained at 0 Amperes, which means that there is no current flow along the d-axis.

Although torque control is typically used in EVs, speed control was selected in this paper due to its direct compatibility with the MIOBC topology, simplified driver input interpretation, and energy management considerations. As discussed above, the outer speed loop generates a torque reference, which is then regulated by inner current control loops, ensuring smooth operation.

5.2 Loop Shaping and Gain Optimisation for DRBR Controller

The two PI controllers $G_{piVI}(s)$ shown in Fig. 9 are used to regulate the d- and q-axis currents, generating the PMSM stator voltage references v_a^*, v_b^*, and v_c^*. Given the complexity introduced by the RHP zeros of the Cuk-based SMs, designing the inner loop controllers' gains can be challenging [21]. A straightforward loop-shaping method for fine-tuning the inner loop controller gains is used in this paper.

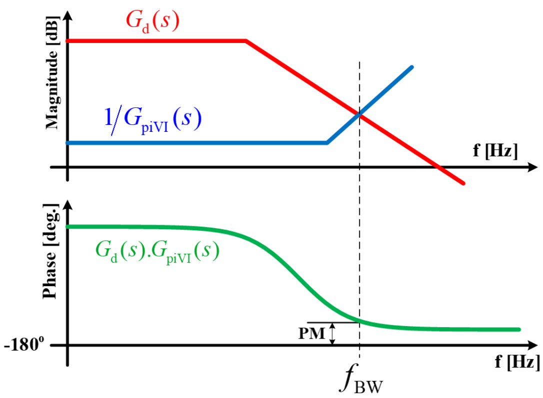
PM and GM are selected as control objectives to stabilise the inner loop through the gains of the PI controllers [22]. Fig. 10a illustrates the process of determining the loop BW, which is the frequency at which the loop gain equals unity. This frequency is found by intersecting the Bode plots of the transfer function $G_d(s)$ and the reciprocal of the PI controller $G_{piVI}(s)$. The gains of $G_{piVI}(s)$ are then adjusted so that its Bode plot coincides with $G_d(s)$ at the intended BW frequency. In the simulation results shown in Fig. 11a, the gains of $G_{piVI}(s)$ are chosen as $k_{p_1} = 0.1$ and $k_i = 5$ to achieve a phase margin of 45°.

To further enhance the stability of the MIOBC, a lead-lag compensator $G_{c_1}(s) = k_{c_1}(s + \omega_{z_{c_1}})/(s + \omega_{p_{c_1}})$ is also employed to add extra phase margin at the inner loop bandwidth and mitigate the influence of the SM's RHP zeros. Fig. 10b shows how this compensator adjusts the loop gain. In Fig. 11b, the simulation results for the inner loop gain and phase are displayed after the lead-lag compensator $G_{c_1}(s) = 4(s + 5000)/(s + 10000)$ is incorporated. These results demonstrate how the compensator impacts the gain and phase characteristics of the inner loop, ultimately enhancing stability.

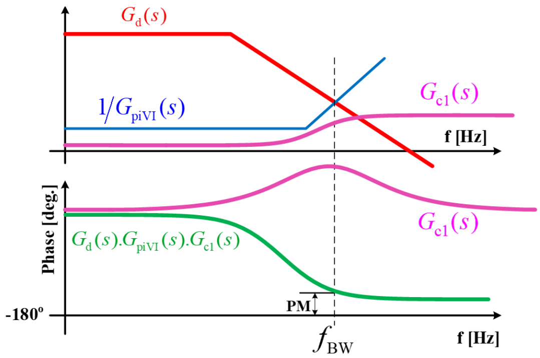
Unlike the current controllers, the speed controller tuning does not require explicit loop-shaping with respect to the plant's RHP zeros. The tuning of the outer-loop speed PI controller (i.e., $G_{pi\omega}(s) = k_{p,\omega} + \frac{k_{i,\omega}}{s}$) is carried out according to standard practices for cascaded speed-current control of PMSM drives. Since the speed loop dynamics are significantly slower than the inner current loop, the gains of $G_{pi\omega}(s)$ are selected to provide an adequate compromise between transient response (rise time and overshoot) and steady-state accuracy. Specifically, the proportional and integral gains ($k_{p,\omega}$, $k_{i,\omega}$) are initially determined based on the PMSM model parameters and refined via trial-and-error in simulation, ensuring stable and robust vehicle speed tracking throughout both motoring and regenerative braking phases:

$$k_{p,\omega} = \frac{J}{K_t}\omega_{c,\omega}, \qquad k_{i,\omega} = \frac{B}{K_t}\omega_{c,\omega} \tag{30}$$

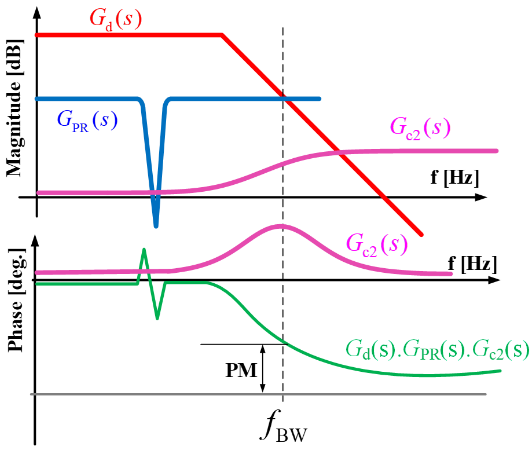
with J and B being the motor's inertia and friction, K_t the torque constant, and $\omega_{c,\omega}$ the desired closed-loop speed bandwidth.



(a) Bode plots for DRBR mode (Using PI controller)



(b) Bode plots for DRBR mode (Using PI controller and lead-lag compensator)



(c) Bode plots for charging mode (Using PR controller and lead-lag compensator)

Figure 10: Bode plots for inner loop shaping method concept

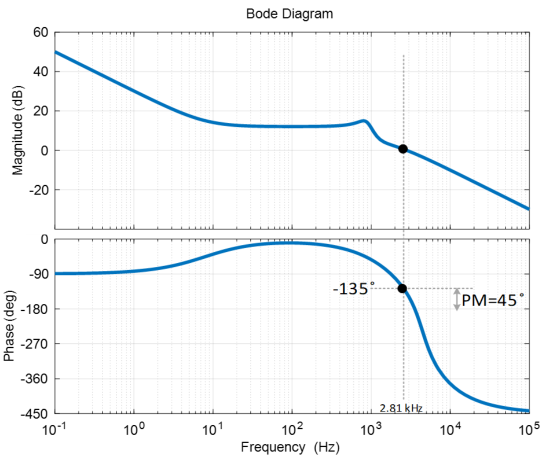
5.3 Control Design for Charging Mode (Charging Controller)

When the charging power for the battery segments is supplied from the three-phase AC grid, the PMSM is disconnected via SW_{abc}. In this configuration, the current and voltage frequencies are fixed at the grid frequency of f_o =50 Hz. To regulate the power flow and ensure efficient charging, a PR controller is used. The transfer function $G_{PR}(s)$ of the PR controller is designed to have a large gain at the grid frequency f_o, without the need for phase/angle measurements. By adjusting the gains k_{p_2}, k_r, and the natural frequency $\omega_o = 2\pi f_o$, the PR controller can effectively adjust the charging process.

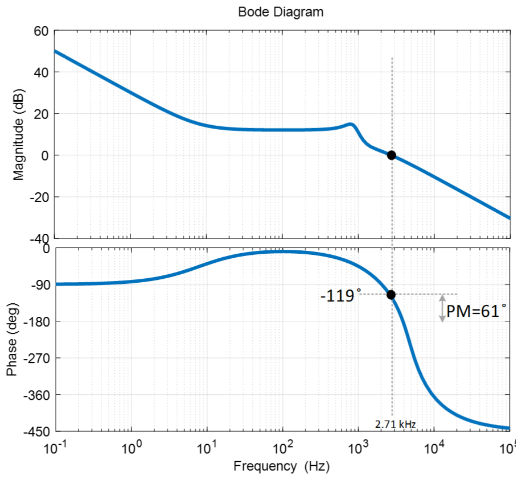
Fig. 12 depicts the control loop for phase a during the charging mode, utilizing the PR controller. The desired charging power is used to compute the reference current ${i_g}^* = {i_o}^*$. This current determines the amount of current required from the AC grid to achieve the desired charging power $P_{ch}^* = \dfrac{3v_g^* i_g^*}{2}$ for the battery segments.

5.4 Loop Shaping and Gain Optimisation for Charging Controller

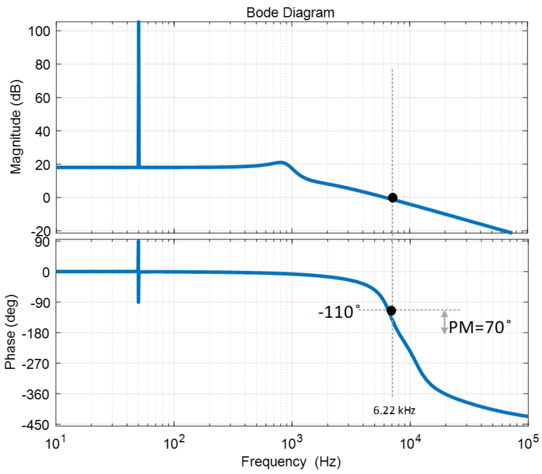
Fig. 10c illustrates how the gains of the charging mode controller are adjusted similarly to those of the DRBR controller. However, the PR controller's Bode plot differs from that of the PI controller used in the DRBR controller. Fig. 11c shows the simulation results for the loop gain and phase with a lead-lag compensator and the PR controller set at $k_{p_2} = 2$ and $k_r = 8$. These results demonstrate how the lead-lag compensator $G_{c_2}(s) = 2(s+1000)/(s+6000)$ and the PR controller affect the gain and phase characteristics of the charging mode controller.



(a) Bode plots for DRBR mode (Using PI controller)



(b) Bode plots for DRBR mode (Using PI controller and lead-lag compensator)



(c) Bode plots for charging mode (Using PR controller and lead-lag compensator)

Figure 11: MATLAB/simulation results for the inner loop shaping method using different controllers

6 Modulation strategy

In the Cuk-based SM, the modulation strategy is crucial for generating the desired output voltages and ensuring efficient operation. The core of this modulation strategy is the duty cycle ratio $d(t)$, which represents the proportion of time the switch is activated relative t_{ON} to the total switching period t_s. Mathematically, this is expressed as:

$$d(t) = \frac{t_{\mathrm{ON}}}{t_s} \tag{31}$$

To achieve the desired output voltage of the k^{th} SM in each phase j as defined in Eq. (2), the duty cycle ratio is determined by the following relationship:

$$d(t) = \frac{\left|v^*_{o_{k_j}}\right|}{\left|v^*_{o_{k_j}}\right| + Nv_{in}} \tag{32}$$

where $v^*_{o_{k_j}}$ is the output voltage reference generated by the inner current control loops, and v_{in} is the instantaneous input voltage to the SM.

This formulation directly links the output of the control system (i.e., the reference voltage $v^*_{o_{k_j}}$, generated via d-q axis PI controllers and frame transformations as shown in the control block diagram in Fig. 9) to the switching command for each Cuk SM. The result is that the output of each SM accurately tracks its assigned reference, as required by the overall converter control objectives.

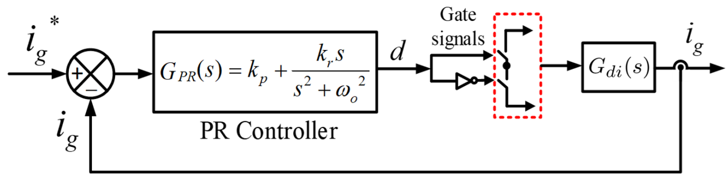


Figure 12: PR controller $G_{PR}(s)$ for phase a during charging mode

The modulation process is visually represented in Fig. 13, which includes three subfigures. The first subplot shows the duty cycle $d(t)$, which varies based on the desired output voltage and input conditions. The second subplot illustrates the sawtooth waveform used as the carrier signal for generating the PWM signal. The third subplot displays the resultant PWM signal, which is compared against the sawtooth waveform to determine the switching instants.

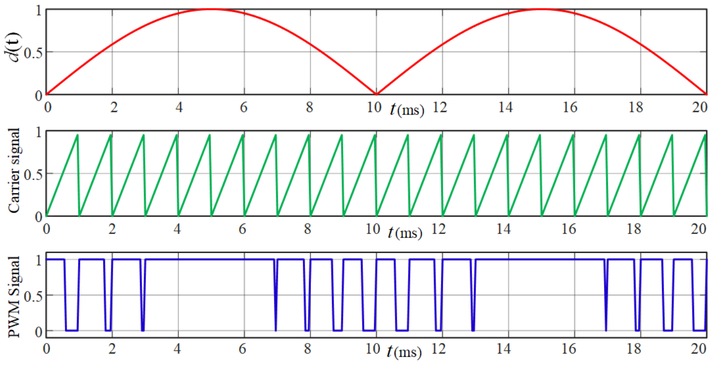


Figure 13: Modulation strategy

7 Efficiency analysis

Mathematical analysis needs to be performed to determine the efficiency of the MIOBC topology. The total power loss associated with the semiconductor devices (i.e., switches and diodes) is the sum of the conduction and switching losses and can be approximated as:

$$P_{\text{total (loss)}} \approx P_{\text{Cond. (loss)}} + P_{\text{Sw. (loss)}} \tag{33}$$

, where the conduction losses and switching losses are calculated from (34) and (35), respectively:

$$\begin{aligned} P_{\text{Cond. (loss)}} = {} & 3mR_{\text{ON}} I^2_{S_1(\text{rms})} \\ & + 12mR_{\text{ON}} I^2_{S_2(\text{rms})} + 12m\bar{I}_{D_3} V_{DF} \end{aligned} \tag{34}$$

$$P_{\text{Sw. (loss)}} = \frac{3V_{in}\bar{I}_{S_1}}{2}(t_{\text{ON}} + t_{\text{OFF}}) + \frac{12V_o\bar{I}_{S_2}}{2}(t_{\text{ON}} + t_{\text{OFF}}) \tag{35}$$

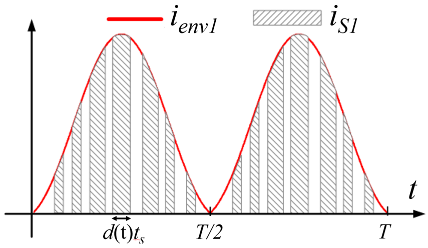
, with V_{DF} and m being the forward voltage of the diodes and the number of segments. t_{on} and t_{off} are available from the datasheet of the semiconductor devices (i.e., switches, diodes).

It is important to know the current flow through the switches to assess the efficiency of the proposed MIOBC. The waveforms shown in Fig. 14 are extracted from simulations and used to calculate the root mean square (RMS) and average values of the currents passing the semiconductor devices.

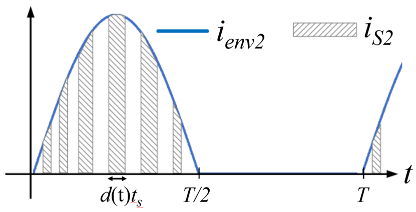
Fig. 14a illustrates the current flowing through the input side switch S_1 over one switching period. When S_1 is ON, it chops the envelope current i_{env_1}. The calculation of this current involves several factors and considerations. Specifically, it depends on the duty cycle of the switch S_1, the input and output currents and the HF transformer transfer ratio as:

$$i_{env_1}(t) = i_{in}(t) + N\,|i_o(t)| = \frac{N\,|i_o(t)|}{1 - d(t)} \tag{36}$$

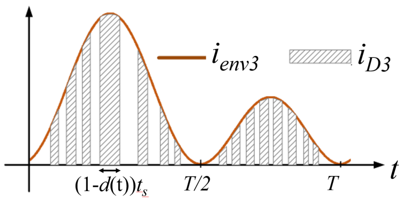
The rms value of the current passing through in S_1 can be calculated as:



(a) Primary side switch S_1



(b) Secondary side switch S_2



(c) Diode D_3

Figure 14: Current waveforms of the semiconductor devices

$$\begin{aligned} I^2_{S_1(\mathrm{rms})} &= \frac{1}{T/2}\int_0^{\frac{T}{2}} \left(i_{S_1}(t)\right)^2 \mathrm{d}t = \frac{1}{T/2}\int_0^{\frac{T}{2}} \left(i_{\mathrm{env}_1}(t)\right)^2 d(t)\,\mathrm{d}t \\ &= \frac{N^2V_o^2I_o^2}{24\pi V_{\mathrm{in}}^2}\left(\frac{NV_{\mathrm{in}}}{V_o}+9\pi\right) \end{aligned} \tag{37}$$

, where $V_{in} = \sum_1^m V_{in_k}$.
The average value of the current passing through in S_1 is calculated as:

$$\bar{I}_{S_1} = \frac{1}{T/2}\int_0^{T/2} i_{S_1}(t)\,\mathrm{d}t = \frac{1}{T/2}\int_0^{T/2} i_{env_1}(t)d(t)\,\mathrm{d}t = \frac{I_oV_o}{2NV_{in}} \tag{38}$$

Fig. 14b depicts the current flow through switch S_2. When this switch is in the ON state, it chops the flow of the envelope current i_{env_2}. Since the input current i_{in} is always positive, the current flowing through the body diode of switch S_1 is zero. In addition, due to the design and operation of the SM circuit, the currents flowing through the output side switches S_2, S_3, S_4, and S_5 are symmetric. This means that the analysis can focus on a single switch for the secondary side, and the results can be multiplied by four to account for all switches. The envelope current i_{env_2} associated with S_2 is estimated by:

$$i_{env_2}(t) = i_o(t) \tag{39}$$

The rms value average values of the current passing through S_2 can be calculated as (40) and (41), respectively:

$$\begin{aligned} {I^2}_{S_2(rms)} &= \frac{1}{T}\int_0^{\frac{T}{2}} \left(i_{S_2}(t)\right)^2 \mathrm{d}t = \int_0^{\frac{T}{2}} \left(i_{env_2}(t)\right)^2 d(t)\,\mathrm{d}t \\ &= \frac{I_o^2}{2\pi}\left[\pi(a+\frac{1}{2})^2 + 2(a)^3(\tan^{-1}(\frac{1}{\sqrt{(a-1)^2}} - \frac{\pi}{2})) - 2(a)\right] \end{aligned} \tag{40}$$

$$\begin{aligned} \bar{I}_{S_2} &= \frac{1}{T}\int_0^{T/2} i_{S_2}(t)\,\mathrm{d}t = \frac{1}{T}\int_0^{T/2} i_{env_2}(t)d(t)\,\mathrm{d}t \\ &= \frac{I_o}{2\pi}\left[\frac{2a^2(\frac{\pi}{2} - \tan^{-1}(\frac{1}{\sqrt{(a-1)^2}}))}{\sqrt{(a-1)^2}} - a\pi + 2\right] \end{aligned} \tag{41}$$

, where $a = \dfrac{NV_{in}}{V_o}$.

Fig. 14c illustrates the current flow through diode D_3. The same currents (same amplitude but with different phases) flow through the output body diodes of switches S_2, S_4, and S_5. Therefore, the analysis can focus on a single device, and the results can be multiplied by four to account for all switches. When switch S_1 is OFF, diode D_3 conducts and carries the envelope current i_{env_3}. The calculation of i_{env_3} involves considering the duty cycle of S_1 and the characteristics of the SM circuit, including the HF transformer transfer ratio N as well as the input and output currents as follows:

$$i_{env_3}(t) = \frac{i_{in}(t)}{2N} + \frac{i_o(t)}{2} = \frac{1}{2}\left(\frac{i_o(t)}{1-d(t)}\right) \tag{42}$$

The rms and average values of the current passing through D_3 are calculated as (43) and (44), respectively:

$$\begin{aligned} I^2_{D_3(\text{rms})} &= \frac{1}{T}\int_0^T \left(i_{D_3}(t)\right)^2 \,\mathrm{d}t = \frac{1}{T}\int_0^{\frac{T}{2}} \left(i_{\text{env}_3}(t)\right)^2 (1-d(t))\,\mathrm{d}t \\ &= \frac{NV_{\text{in}}I_o^2}{8V_o} \end{aligned} \tag{43}$$

$$\bar{I}_{D_3} = \frac{1}{T}\int_0^T i_{D_3}(t)\,\mathrm{d}t = \frac{1}{T}\int_0^T i_{env3}(t)(1-d(t))\,\mathrm{d}t = \frac{I}{\pi} \tag{44}$$

Finally, the MIOBC efficiency η is estimated by:

$$\eta \approx \frac{V_o I_o}{V_o I_o + \frac{2}{3}P_{\text{tot(loss)}}} \tag{45}$$

The MATLAB simulation results depicted in Fig. 15 illustrate the efficiency of the MIOBC as defined in (45). These results are obtained for a range of continuous power and SM numbers. As the number of battery segments increases, the ON-resistance and forward voltages of the semiconductor devices decrease, leading to reduced losses in the devices. Consequently, the efficiency of the MIOBC tends to increase. This is because a larger number of segments allows for better distribution of power and reduces the load on individual devices. However, beyond a certain threshold (which in this work is six segments), the efficiency begins to decrease. This is due to the noticeable increase in the number of devices required to accommodate the additional segments. Very high power levels can also lead to increased conduction and switching losses in semiconductor devices.

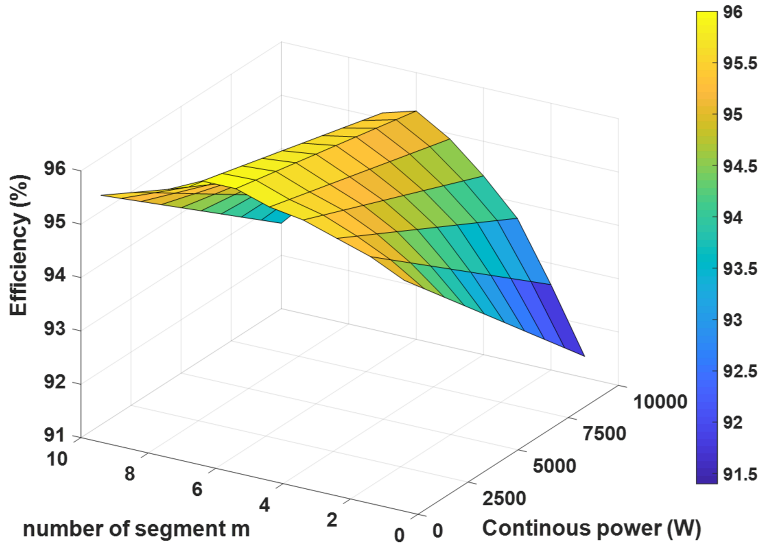


Figure 15: Simulation results of MIOBC efficiency

8 Experimental Verification

This section presents the experimental set-up and the results across three operation modes, namely driving, regenerative braking, and charging.

8.1 Experimental set-up

The overall layout of the experimental set-up is shown in Fig. 16a. The MIOBC, along with its control, measurement circuits, and HV box, was mounted externally and connected to the PMSM via long HV cables. Rear wheels were lifted, and mechanical brakes were applied to simulate load torque from air drag and friction [23]. Fig. 16b shows an isolated Cuk SM converter used in the MIOBC. This converter features series-connected capacitors with the HF transformer to block DC currents.

(a) Overall layout (b) Cuk-based SM

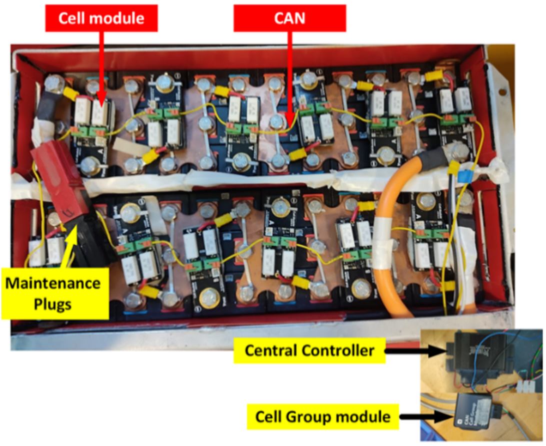
Figure 16: Experimental set-up

The transformer is compact due to the modular design of the MIOBC. Passive components of the Cuk-based SMs, listed in Table 1, were selected to keep voltage and current ripples within 10% of peak values at the switching frequency.

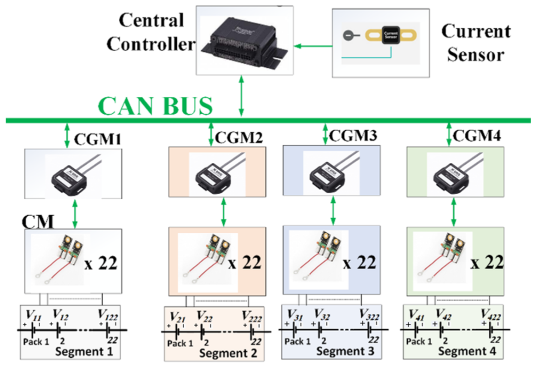
Table 1: System Parameter Values

Parameter	Value
Switching frequency	$f_s = 20$ kHz
Inductors	$L_1 = L_2 = 1$ mH
Capacitors	$C_1 = C_2 = 20\ \mu F$
Turns' ratio	$N = 2$
Output capacitor	$C_o = 1\ \mu F$
Motor type	PMSM
PMSM peak power	68 kW
PMSM maximum current	200 A (2 min.)
PMSM maximum speed	6000 rpm
PMSM maximum torque	140 N.m
PMSM efficiency	92-98%
PMSM inductances	$L_d/L_q = 125/130\ \mu H$
Internal phase resistance at $25^{\circ}C$	$120\ m\Omega$
Motor number of poles	10
Wheel radius	$r = 30\ cm$
Gearbox ratio	$G = 2.5$
Battery cell	Li-ion Li8P25RT
Battery pack (8 cells)	3.6 V, 20.4 Ah
Battery Segment	$p = 22$ packs
Number of Segments	$m = 4$ segments

The battery box layout, as shown in Fig. 17a, consists of battery packs each containing 8 Li-ion cells (3.6 V, 20.4 Ah) connected in parallel. These packs are arranged in series to form battery segments, with a total of 4 segments in the system. For safety, 160 A EET protection fuses are used. Fig. 17b illustrates the BMS, which comprises a central controller (EMUS G1), 4 Cell Group Modules (CGMs), 88 individual Cell Modules (CMs), and a current sensor. The CGMs gather data from the CMs, which monitor the voltage, temperature, and current of the battery segments. This data is transmitted to the central controller via a CAN bus. The central controller oversees that the system's voltages, currents, and temperatures remain within safe limits, alerting the driver or activating safety measures if anomalies are detected. Additionally, the LV control circuits manage the vehicle's power state, process pedal inputs, display information on the dashboard, and conduct monitoring and safety functions.



(a) Physical layout



(b) BMS control

Figure 17: HV battery box

8.2 Experimental results

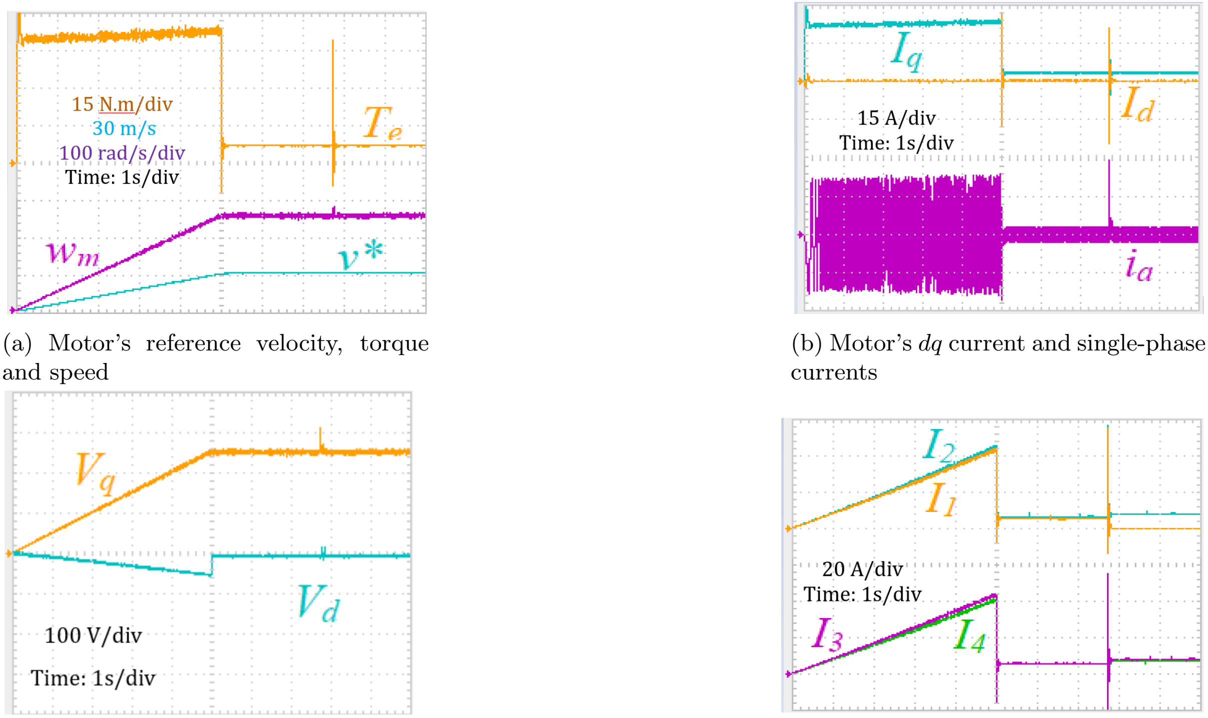
8.2.1 Driving mode

The experimental results under driving mode with a partial fault occurring at around $t = 7.5$ s in one of the battery segments are depicted in Fig. 18. The accelerator pedal transmits the reference speed signal v^* to the DSP, causing the car's linear speed to increase from zero to a maximum of 30 m/s (108 km/h) in approximately 5 seconds. To mimic the partial fault, the first battery segment was disconnected. As a result of this partial fault, the electromagnetic torque T_e shown in Fig. 18a and dq-axis currents and voltages of the PMSM in Fig. 18b and Fig. 18c are impacted. However, they are quickly restored to their intended values, thanks to the implemented controller. Regarding the segment currents of the battery, the current through the first segment drops to zero at $t = 7.5$ s, as shown in Fig. 18d. To compensate for the failure of the first segment, the current through the unaffected segments (i.e., I_2, I_3, and I_4) increases. Therefore, even in the event of a segment becoming disconnected, the batteries are still capable of powering the motor at the same level. This demonstrates the robustness and fault tolerance of the MIOBC system, ensuring uninterrupted operation and maintaining performance even in the presence of faults in individual battery segments.

8.2.2 Regenerative braking mode

The brake pedal initiates the braking mode, causing the car to decelerate from its maximum speed to a stop in about 5 seconds, as shown in Fig. 19a. In Fig. 19b, the dq currents I_d and I_q are displayed. During braking, the d-axis current remains close to zero, while the q-axis current reverses direction, applying a negative braking torque when the driver applies the brake pedal. This negative braking torque T_e is plotted alongside the motor speed in Fig. 19a.

Fig. 19c shows how the phase voltage v_a, as well as dq voltages V_d and V_q, are reduced as the PMSM operates in generator mode (PMSG) during braking, supplying power to the battery segments. The battery segments' currents are displayed in Fig. 19d. These currents change direction during the



(a) Motor's reference velocity, torque and speed

(b) Motor's dq current and single-phase currents

(c) Motor's dq voltage

(d) Batteries' currents

Figure 18: Experimental results during driving mode under partial fault in the first battery segment in phase "a"

deceleration stage. Subsequently, to charge the batteries, electricity moves from the PMSM, which is now functioning as a PMSG, to the battery segments.

Fig. 19e displays the first SM's single-phase equivalent capacitor voltage $v_{C_{eq_{a_1}}}$ and the first SM's single-phase output voltage $v_{o_{a_1}}$. Lastly, the first SM's single-phase input current $I_{in_{a_1}}$ and its duty cycle d_{a_1} are depicted in Fig. 19f.

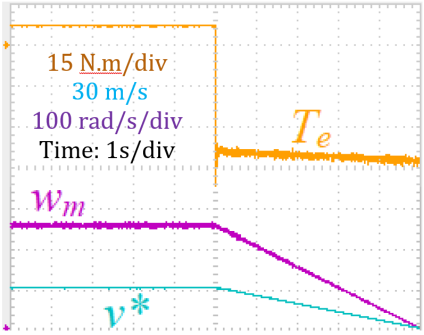
8.2.3 Charging mode

In the charging mode, the MIOBC topology is disconnected from the PMSM and its terminals are connected to the AC grid via the switches SW_{abc} (in Fig. 3a). The battery packs are charged by the AC grid, and the Cuk SM functions as an AC-DC converter. The maximum charging power is 3 kW, with each SM providing 250 W of power. The definitions of the input and output will be inverted because the power is moving through the MIOBC from the grid to the batteries. During this mode, the DC voltages of the battery segments were measured as $V_{in_1} = 79.2$ V, $V_{in_2} = 77$ V, $V_{in_3} = 74.8$ V, and $V_{in_4} = 78.32$ V. The values of the battery currents are inversely proportional to their voltages.

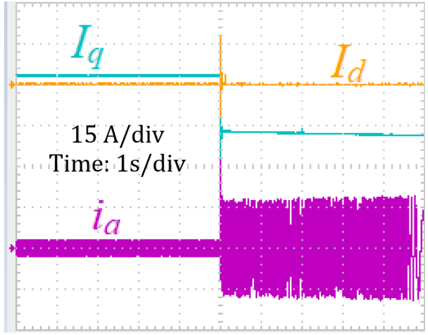
To evaluate the performance of the controllers in the event of a partial fault during the charging mode, the first battery segment was disconnected at $t = 0.2$ s (after 10 grid cycles). The experimental results for the grid current ($i_a = i_{g_a}$) and the phase-specific individual voltages ($v_{o_{1_a}}$, $v_{o_{2_a}}$, $v_{o_{3_a}}$, and $v_{o_{4_a}}$) of the SM are shown in Fig. 20. The charging power is almost 2.8 kW and the grid voltage peaks at 311 V. Two distinct PR controllers are employed.

In the experimental results displayed in Fig. 20a and Fig. 20b, it is observed that the grid current i_a and the individual voltages of the SM ($v_{o_{1_a}}$, $v_{o_{2_a}}$, $v_{o_{3_a}}$, and $v_{o_{4_a}}$), and v_{o_4a}) take about 3-4 cycles (0.06-0.08 s) to return to their desired values when using the first PR controller G_{PR_1}. This controller targets a large phase margin (PM $\approx$ 60 deg) and low bandwidth (BW $\approx$ 300 Hz). In the second test, the BW is increased by using the second PR controller G_{PR_2}, which has a larger k_p, but at the cost of a narrower phase margin (PM $\approx$ 38 deg, BW $\approx$ 1000 Hz). Both the grid current and the individual voltages of the SM can return to their desired values relatively faster than with the first controller, as demonstrated in Fig. 20c and Fig. 20d.

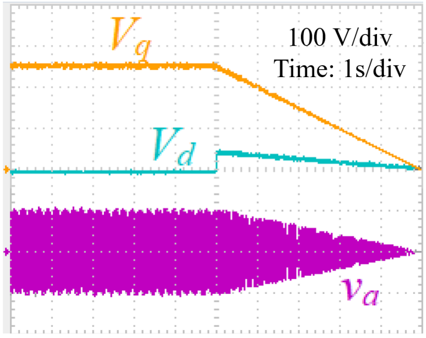
The grid current waveform i_a in Fig. 20a shows a significant overshoot that could potentially trip the circuit breaker. While the first controller G_{PR_1} achieves a higher PM, which enhances system



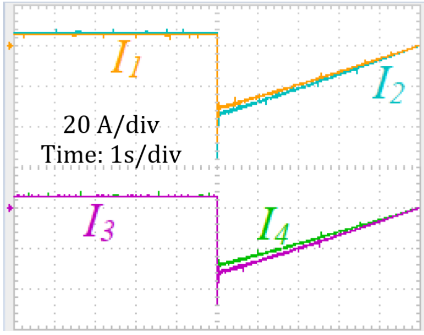
(a) Motor's reference velocity, torque and speed



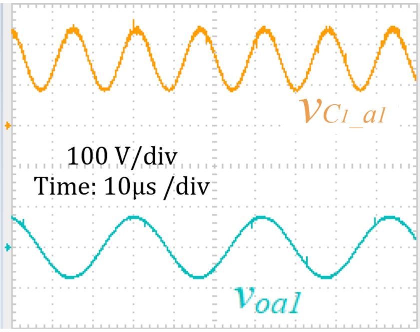
(b) Motor's dq and single-phase currents



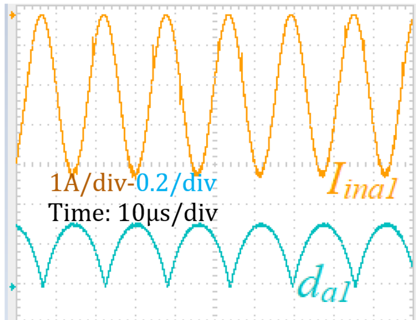
(c) Motor's dq and single-phase voltages



(d) Batteries' currents



(e) First SM's single-phase equivalent capacitor voltage and output voltage



(f) First SM's single-phase input current and duty cycle

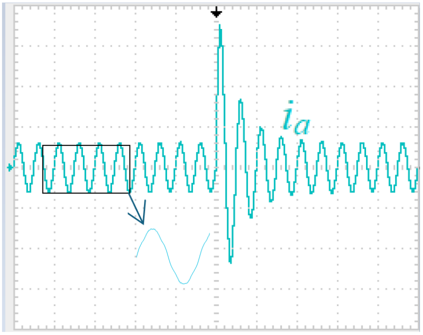
Figure 19: Experimental results during regenerative braking mode

stability, the issue primarily arises from the smaller BW. This limited BW can lead to elevated switching transients that may damage the power switches of the SMs. This problem can be addressed by tuning the controller's gains. Higher gains boost the BW and reduce the PM, thereby enhancing the controller's speed but compromising the system's stability and power quality. Therefore, tuning the controller's gains involves a delicate balance: increasing the controller's responsiveness improves dynamic performance but at the expense of stability and power quality. Thus, there is an inherent trade-off between enhancing the controller's speed and maintaining the stability and power quality of the system.

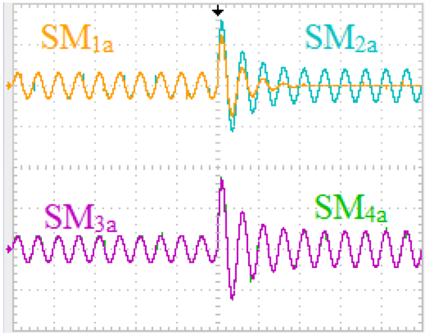
8.2.4 HF transformer validation and snubber protection

To experimentally validate the high-frequency transformer behaviour and assess the effectiveness of the snubber protection, the transformer used in each Cuk-based SM is modelled and tested.

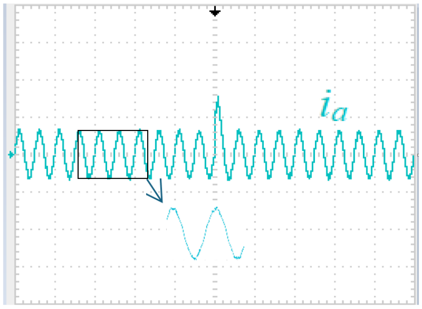
Nanocrystalline cores (F1AH0897, Hitachi Finemet type FT-3KM) were used in the transformer construction. Small-signal frequency domain models (open-circuit and short-circuit) were extracted using a vector network analyser, and the transfer functions were derived accordingly. The resulting Bode plots confirm expected magnetic behaviour, and the key parameters were estimated as follows: leakage inductance $L_p \approx 0.9$ μH, magnetising inductance$L_m \approx 2$ mH, and winding resistances $R_p \approx R_s \approx$ 107 mΩ. These indicate that the leakage is less than 1% of the magnetising inductance, significantly



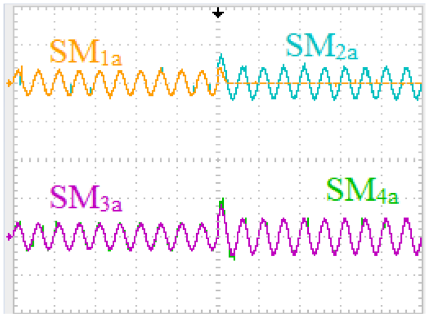
(a) Grid current using G_{PR_1}



(b) SM individual voltages of phase "a" using G_{PR_1}



(c) Grid current using G_{PR_2}



(d) SM individual voltages of phase "a" using G_{PR_2}

Figure 20: Experimental results during charging mode under partial fault in the first battery segment in phase a

minimising voltage spike potential. Nevertheless, to provide additional damping for high-frequency transients, an RC snubber circuit ($R_{\mathrm{SNUB}} = 3$ kΩ, $C_{\mathrm{SNUB}} = 12$ pF) was connected across each primary switch. Additionally, the power switches were carefully selected with adequate voltage ratings and switching energy tolerances to withstand worst-case transient conditions, including those potentially caused by transformer leakage inductance and parasitic ringing.

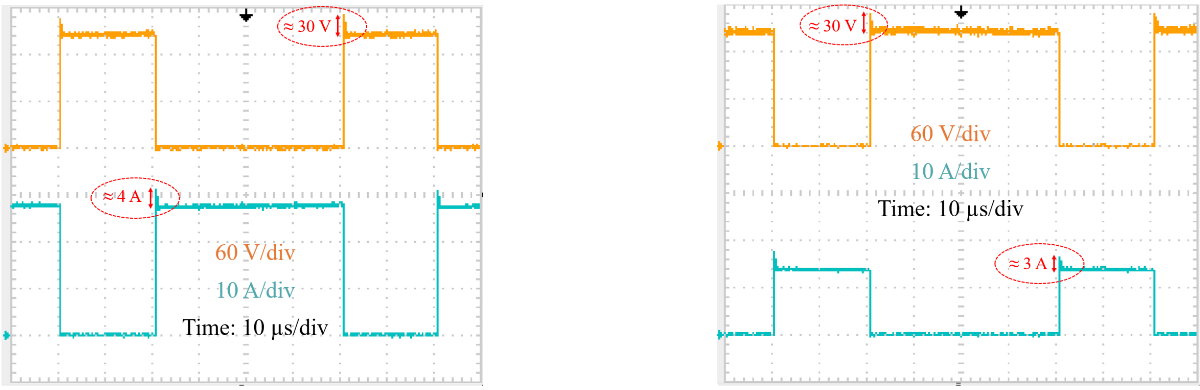
The effectiveness of this protection strategy is confirmed by the switching waveforms shown in Fig. 21. The voltage and current transitions of the primary and secondary switches demonstrate clean edges, with no overshoot or ringing, thus validating the transformer and snubber design in real operating conditions.

8.2.5 Power rating and component sizing

The power rating of the proposed MIOBC topology is directly influenced by the mechanical demands of the EVs. As illustrated in Fig. 22 (from the driving mode), point P_1 corresponds to the condition of maximum mechanical power, $P = T_e \cdot \omega_m$, occurring during rapid acceleration. This results in peak current draw from the battery segments, requiring that the semiconductor devices in the Cuk-based SMs be rated for short-duration high currents (e.g., 40 A). In contrast, point P_2 represents steady cruising operation, where devices must safely handle rated continuous currents (e.g., >5 A).

Each SM employs FDL100N50F MOSFETs, which are rated for 500 V and 100 A, allowing them to safely withstand the peak segment voltage (88 V, based on 22 packs × 4.0 V per Li-ion cell) and the maximum observed current during acceleration. The continuous current capability ensures reliable operation under normal driving and charging conditions.

Although active thermal management (cooling) is not implemented in this study, the devices were selected with a high factor of safety. Specifically, the combined rating across 12 devices (e.g., 3 phases × 4 segments) is 60 kW, while the actual system peak power is only 15 kW. This yields a safety factor of 4, which ensures robustness during consecutive acceleration and braking cycles. All passive components were also selected to accommodate the same voltage and current stresses.



(a) Voltage and current across the primary side switch

(b) Voltage and current across one ofthe secondary side switches

Figure 21: Voltage and current profiles across the primary and secondary side switches.

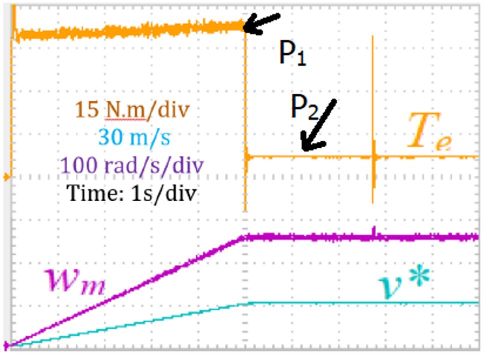


Figure 22: Mechanical power profile: P_1 indicates peak power during acceleration; P_2 corresponds to steady-state operation.

8.2.6 Experimental efficiency results

Fig. 23 illustrates the measured efficiency of the MIOBC system as a function of the power drawn from the AC grid. The results show a clear trend of increasing efficiency with rising output power, reaching a peak value of 94.8%. This improvement is primarily attributed to the higher ratio of output power to fixed losses, which include gate driver power consumption, semiconductor switching losses, and core magnetising losses in the HF transformers. At lower power levels, these fixed losses are proportionally more significant, reducing overall efficiency. However, as power increases, the relative impact of these losses diminishes.

9 Conclusion

This paper presented the control strategies and operational validation of a novel MIOBC topology for EV applications, covering driving (acceleration), regenerative braking (deceleration), and charging modes. The proposed topology significantly reduces the overall weight and size of the OBC by integrating charging functionality into the traction inverter, while also improving FRT capability through its modular structure. The system employs isolated, single-stage, bidirectional Cuk-based converters as SMs, chosen for their high efficiency, continuous input and output current characteristics, and inherent PFC. To achieve robust performance across all modes of operation, loop-shaping control techniques, including PI, PR, and lead-lag compensators, addressed challenges such as the presence of RHP zeros in Cuk converters. Experimental validation on an electric FS racing car demonstrated the system's effectiveness. During driving mode, the vehicle successfully accelerated from 0 to 30 m/s (108 km/h) in approximately 5 seconds, with smooth transitions in torque and current profiles and minimal ripple in phase currents and voltages. Regenerative braking tests confirmed the system's ability to reverse q-axis current to efficiently convert mechanical energy into electrical energy, charging the battery segments. In charging mode, the

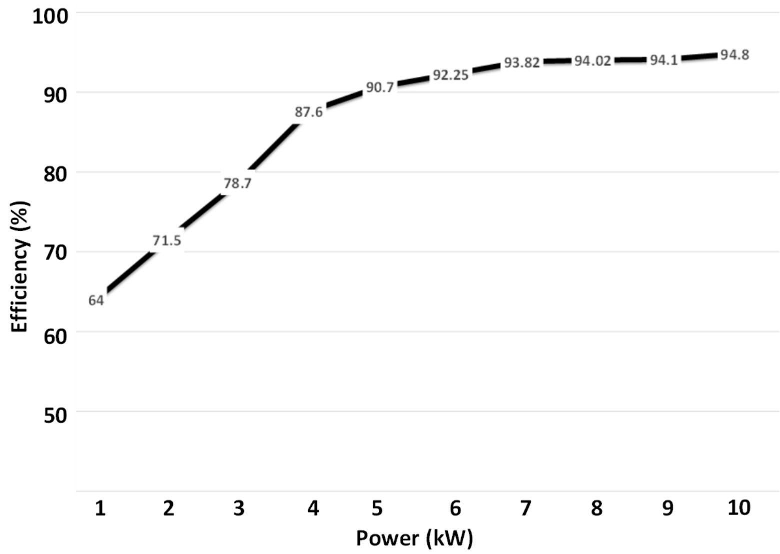


Figure 23: The tested efficiency of the MIOBC system

MIOBC achieved up to 3 kW charging power, maintaining stable operation even under partial faults. The system's robustness was further validated under partial fault scenarios, such as the disconnection of a battery segment. It maintained stable operation by redistributing the load among the remaining segments, ensuring uninterrupted performance. The use of PR controllers with varying BWs demonstrated a trade-off between dynamic response and stability. A lower-BW PR controller enhanced stability at the cost of slower recovery, while a higher-BW controller improved responsiveness with slightly reduced PMs. Measured efficiency results were also presented, showing that the MIOBC achieves a peak efficiency of 94.8% during grid-based charging. The trend confirms that efficiency increases with output power due to the decreasing relative impact of fixed losses, and the experimental data aligns closely with theoretical expectations. Future work could explore the design of advanced controllers that eliminate the need for a trade-off between dynamic response and stability, further optimising system performance. Additionally, these concepts could be expanded to other EV platforms to explore their broader applicability.

Acknowledgment

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Appendix

Proof of Ripple Cancellation in Three-Phase Battery Interfacing:

Single-phase power converters are known to introduce low-frequency (2ω) power ripple into the DC link, which can degrade battery performance and lifespan. In contrast, the proposed MIOBC topology connects each battery segment to three SMs, each interfaced with a different phase of a balanced three-phase AC source. This configuration leads to inherent cancellation of the second-harmonic power ripple.

Single-phase case: Consider a single-phase AC source with voltage and current:

$$v_{ac}(t) = V_m \sin(\omega t), \quad i_{ac}(t) = I_m \sin(\omega t - \phi) \tag{A.1}$$

The instantaneous power is:

$$\begin{cases} p_{1\phi}(t) = v_{ac}(t) \cdot i_{ac}(t) = V_m I_m \sin(\omega t)\sin(\omega t - \phi) \\ \qquad = \underbrace{\frac{V_m I_m}{2}\cos(\phi)}_{\text{DC}} - \underbrace{\frac{V_m I_m}{2}\cos(2\omega t - \phi)}_{2\omega \text{ ripple}} \end{cases} \tag{A.2}$$

This results in a constant (DC) component and a ripple term at 2ω.

Three-phase case: For a balanced three-phase system:

$$\begin{cases} v_a(t) = V\cos(\omega t), & i_a(t) = I\cos(\omega t - \phi) \\ v_b(t) = V\cos\left(\omega t - \frac{2\pi}{3}\right), & i_b(t) = I\cos\left(\omega t - \frac{2\pi}{3} - \phi\right) \\ v_c(t) = V\cos\left(\omega t + \frac{2\pi}{3}\right), & i_c(t) = I\cos\left(\omega t + \frac{2\pi}{3} - \phi\right) \end{cases} \tag{A.3}$$

The instantaneous power for each phase is:

$$\begin{cases} p_a(t) = \frac{VI}{2}\left[\cos(\phi) + \cos(2\omega t - \phi)\right] \\ p_b(t) = \frac{VI}{2}\left[\cos(\phi) + \cos\left(2\omega t - \frac{4\pi}{3} - \phi\right)\right] \\ p_c(t) = \frac{VI}{2}\left[\cos(\phi) + \cos\left(2\omega t + \frac{4\pi}{3} - \phi\right)\right] \end{cases} \tag{A.4}$$

Summing all three phases results in:

$$\begin{cases} p_{3\phi}(t) = p_a(t) + p_b(t) + p_c(t) = \frac{VI}{2}\left[3\cos(\phi)\right] \\ \qquad + \frac{VI}{2}[\cos(2\omega t - \phi) + \cos(2\omega t - \frac{4\pi}{3} - \phi) \\ \qquad + \cos(2\omega t + \frac{4\pi}{3} - \phi)] = \frac{3VI}{2}\cos(\phi) \\ \quad + \frac{VI}{2} \cdot \underbrace{\left[\cos A + \cos\left(A - \frac{4\pi}{3}\right) + \cos\left(A + \frac{4\pi}{3}\right)\right]}_{=0} \end{cases}, \tag{A.5}$$

where $A = 2\omega t - \phi$.

The sum of three cosine waves 120° apart is zero. Therefore:

$$p_{3\phi}(t) = \frac{3VI}{2}\cos(\phi) \tag{A.6}$$

This shows that the total instantaneous power is constant. Therefore, in a balanced three-phase MIOBC system, the battery is not subjected to 2ω ripple, significantly improving power quality and battery longevity.

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