Low Power Electronics and Thermal Management for the Cryogenic Temperature Regime

George Charles Ridgard, MPhys (Hons)

Physics Department

Lancaster University

Supervisors: Professor Jonathan Prance and Professor Viktor Tsepelin

A thesis submitted for the degree of

Doctor of Philosophy

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Abstract

Understanding how power dissipation affects the local temperature distribution is key when conducting sensitive experiments at low temperature. This thesis develops strategies for reducing the power consumption of electronics at cryogenic temperatures and for managing the thermal gradients created by the dissipated power. First, the low temperature characterisation of low threshold Field Effect Transistors devices is shown, to assess their suitability for low supply voltage cryogenic circuits. Secondly, the *in situ* testing of resistors is used to optimise two differential amplifiers for gain, power consumption, and bandwidth. Finally, results from both experiments lead to the demonstration of a novel way of reducing supply voltages in low temperature electronics, 'cryogenic threshold engineering'. This is the use of FETs with negative room temperature thresholds, that move close to zero once cooled to low temperatures. This technique was demonstrated in a common source amplifier. Both theory, simulation and experiment showed a factor of 8 improvement in efficiency from 295K to 4K. In this thesis a setup designed to mimic a quantum computing was thermally investigated at milli-kelvin temperatures. This involved monitoring the copper mount, interposer, PCB, and internal IC temperature as a function of power dissipated in the IC. A experiment was performed to show aluminium wirebonds can act as superconducting heat switches between hot and cold devices in the same setup. Voltage noise thermometry with the cross-correlation technique was demonstrated inside the IC. This was demonstrated to work in the range 300 mK to

8 K. At 500 mK the benchmark error was 5%. Also, expression for the relative error of the cross-correlation measurement is derived. Finally, a technique to speed up cross-correlation, frequency averaging, is demonstrated in room temperature resistors. Then it is applied to a literature example to demonstrate its application in reducing the uncertainty in noise thermometry.

Declaration

I declare that the work presented in this thesis is, to the best of my knowledge and belief, original and my own work. The material has not been submitted, either in whole or in part, for a degree at this, or any other university. This thesis does not exceed the maximum permitted word length of 80,000 words including appendices and footnotes, but excluding the bibliography. A rough estimate of the word count is:

29535 (errors:2)

George Charles Ridgard

Acknowledgements

The undertaking of a PhD is often thought to be a lonely endeavor; while at times this is true, this sentiment ignores how much support and advice is needed throughout this process. My primary source of support and encouragement throughout my PhD has been my supervisor Jonathan Prance. His relentless encouragement, experimental knowhow and theoretical grounding have been guiding lights for me. For this I will always be grateful. To my deputy supervisor Viktor, I also thank for his advice and for allowing me to teach the 3rd year cryogenic physics lab. I learned lots during that time, and came to feel part of the Lancaster tradition in excellence in cryogenics. Another colossal influence on my work has been Michael Thompson. "Mike" was always around to inform both theoretical and practical considerations during experiments. I am particularly in debt for his patience in teaching me the peculiarities of dilution fridges. I'd also like to acknowledge all the candid conversations and whiteboard sessions with Sergey Kafanov, who's dedication to excellence in physics is inspirational.

For the company during many long hours in the lab I thank Searbhán Peatáin. The many (many..) early morning, flat white and chocolate crossiants at Pizzeta were part of the reason I stayed sane during the most difficult days of the PhD. To Deepanjan Das, Seth Bennett, Sam Dicker, Patrick Steger and all the other students I annoyed with my daily lab rounds I thank for their patience in dealing with my chit chat.

Outside the lab I have both Bowland FC and the Lancaster University Futsal Society to thank for allowing to me to feel the sense of camaraderie that only comes with playing sport. Once more this regular exercise and the opportunity to leave the word of physics briefly helped me keep an even keel through my PhD. I also thank Joseph Earl for his friendship and the many trips (meticulously planned) into the deepest reaches of the lake district which I will always hold close in my

heart. I also thank my partner, Ioanna Pelidis for her unwavering support of my endeavor, despite my many stresses and extra hours in the lab.

Finally I'd like to thank my family. To my parents whom without their consistent, unyielding encouragement in my academic pursuits non of this would have been possible. To my brother whom I've enjoyed many holidays and great nights out with to help puncture the stresses of full time research. To my grandparents whom have always struck the correct balance between setting me straight and encouraging me. I thank you and love you all.

Contributions

This thesis contains work done in collaboration with many other parties. It is the basis for one published applications note (Low Threshold FETs for Low Power Cryogenic Electronics) and one draft paper (Voltage Noise Thermometry in Integrated Circuits at Millikelvin Temperatures) awaiting the application to publication, both drafted by myself. Results contained within here are also in the process of being used by other authors (L. Schreckenberg and N. Deshpande) for a separate publication (Thermal Interface Study for Electronic Packaging at mK Temperature). The work contained within this thesis can be separated into work done in reducing power consumption in cryogenic electronics and thermal management.

For the work regarding the measurement and testing of FETs at cryogenic temperatures I firstly thank L.Wilson and A.Wilson whom manufactured PCB boards that allowed me to build the initial test boards. I performed the initial testing of the FETs and also all the amplifiers in this thesis. I also performed the analysis, but this was informed by J.Prance and M.Thompson. J.Prance designed the first amplifier mentioned in this thesis. For more detailed FET measurements we took several FETs to Oxford Instruments. I planned the measurements while A.Graham and B.Yager carried them out. I performed all of the analysis. I'd like to thank A.Graham, B.Yager, A.Mathews of Oxford Instruments and J.Prance and M.Thompson for proof reading the applications note which followed these measurements.

For the thermal management part of this thesis, I designed the experimental setup and the PCB. The copper bracket was built by R.Grimshaw in the mechanical workshop at Lancaster. The IC used in the experiment was build by P.Vliex and A. Cabrera-Galicia from Forschungszentrum Jülich. Experiments were performed by myself, with a data acquisition software from J.Prance. L. Schreckenberg (also

from Forschungszentrum Jülich) helped to organise the collaboration along with myself. The NbN thermometers used in this experiment were created by O. Bourgeois and V.Doebele at Institut NEEL.

'You cannot step twice into the same river, for other waters and yet others go ever flowing on.' - Heraclitus - Fragments

Contents

Acronyms

ABS Acrylonitrile Butadiene Styrene plastic. 78

ADC Analog to Digital Converter. 23, 107, 124

AMM Acoustic Mismatch Model. 31

ASD Amplitude Spectra Density. 113–115

CBT Coulomb Blockade Thermometer. 5, 10–13, 75, 80–82

CCS Constant Current Source. 54, 55

CMOS Complementary Metal–Oxide–Semiconductor. 1, 21, 30, 76, 94, 128

CSNT Current Sensing Noise Thermometer. 14

DAQ Data Acquisition. 18

DIP Dual Inline Package. 35

DMM Diffuse Mismatch Model. 31

DUT Device Under Test. 133

ENT Equivalent Noise Temperature. 109–111

ESR Extrapolation in the Saturation Region. 39

FD-SOI Fully Depleted Silicon On Insulator. 63, 74, 131

FET Field Effect Transistor. 1–3, 20, 23, 26–28, 34–36, 39, 40, 44, 46, 49, 53, 56, 62–70, 73, 74, 130, 131

FFT Fast Fourier Transform. 105, 109

FOM Figure Of Merit. 33, 43, 62, 64, 66–73, 131

FPGA Field Programmable Gate Array. 18, 23

FR4 Fire Retardant 4. 76, 89

FWHM Full Width Half Maximum. 11

GBWP Gain Bandwidth Product. 64, 72

GE General Electric varnish. 76

IC Integrated Circuit. 2, 5, 14, 16, 75, 76, 78, 79, 84, 87, 89, 91, 93–95, 106, 107, 127–129, 131–133

IRN Input Referred Noise. 51, 52, 56

LNA Low Noise Amplifier. 63, 64, 121

LPF Low Pass Filters. 107

MFFT Magnetic Field Fluctuation Thermometer. 14

MFLI Medium Frequency Lock In amplifier. 13, 46, 49, 51, 107

MOSFET Metal Oxide Semiconductor Field Effect Transistor. 20–22, 34, 35, 37, 38

MXC Mixing Chamber. xii, 75, 76, 79–84, 86–90, 110, 111, 113–116, 127

PCB Printed Circuit Board. 2, 7, 76–79, 86, 87, 89, 91, 132, 134

QIP Quantum Information Processing. 2, 3

SMU Source Measurement Unit. 35

SNR Signal to Noise Ratio. 7, 8, 11, 12, 14, 18, 20, 22, 23, 42, 43, 80, 83

SOIC Small Outline Integrated Circuit. 34

SQUID Superconducting Quantum Inteferance Device. 14

TBR Thermal Boundary Resistance. 27, 30, 31

TSV Through Silicon Via. 91, 93, 133

VLSI Very Large Scale Integration. 20

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Chapter 1

Introduction

Advances in cryogenic technologies allow today's condensed matter physicists to have unprecedented access to low-noise, low-temperature platforms. In particular,"push button" dilution refrigerators that offer base temperatures of 10 mK and hundreds of micro-Watts of cooling power at 100 mK. In turn, this has led to a step change in measurements of quantum behaviour that is not accessible at room temperature. Areas that have benefited from this include fundamental helium-3 and helium-4 dynamics [1], novel electronic device physics [2, 3], and the use of quantum dots [4, 5]. The latter of these research areas is of particular interest today due to the promise of quantum computing, through the exploitation of quantum dots into qubits [6, 7, 8, 9]. In this example, the use of Complementary Metal Oxide Semiconductor (CMOS) technology on the cold plate to integrate quantum and classical aspects is considered crucial to scaling the number of qubits [10]. As such an understanding of classical electronic devices such as Field Effect Transistors (FET) [11, 12, 13] at low temperature is needed. Scaling will require the use of cryogenic read-out and management systems to overcome the large amount of wiring currently associated per qubit [14]. Therefore, it is of general interest to reduce both power consumption in these circuits and manage the dissipated power appropriately.

The movement of the electronics inside the cryostat eliminates associated thermal leakages and form factor problems caused by an excess amount of wiring, but the Joule heating of cryogenic electronics must be minimised [15]. Failing to keep the qubits cold results in reduced coherence times [16], which can render them unusable. Research into keeping qubits (as well as other low temperature experiments) cold can be split into two parts: reduction in power consumption of the read out and management electronics, and thermal management of the power dissipated.

In this thesis the reduction of power dissipation in cryo-electronics is discussed in three key ways. The first is the low temperature characterisation of FET devices, which are needed to aid the design of circuits by observing key FET characteristics as a function of temperature. The second is the *in-situ* optimisation of resistor components in two different DC coupled differential voltage amplifiers at low temperature. Finally, the mitigation of the increase in threshold voltage in transistors at low temperature is demonstrated by 'cryogenic threshold engineering'. This is the selection of FETs with a suitably negative room temperature threshold voltage so that at low temperatures it is minimised. This means that lower supply voltages can be used in subsequently constructed electronics, lowering power consumption.

This thesis describes the thermal management of electronics in three ways. Firstly, a typical Quantum Information Processing (QIP) setup was constructed and had the temperature of its constituent parts, Printed Circuit Board (PCB), interposer, copper mount, cold finger and Integrated Circuit (IC) monitored as a function of power dissipation in the IC. This was done to understand the thermal paths in the setup as well as to inform a COMSOL simulation. Secondly, in the same setup the influence of superconducting bond wires was investigated to determine the extent to which their poor thermal (phononic, not electronic) conductivity

effectively inhibits heat flow. Finally, voltage noise thermometry was used in conjunction with the cross-correlation signal processing technique to provide in-IC thermometry, opening the door to non-dissipative thermal monitoring on chip. A signal processing technique was demonstrated that can speed up the cross-correlation technique, potentially allowing for orders of magnitude faster thermometry.

The background of this thesis is located in Chapter 2. This chapter covers thermometry used in this thesis as well as providing a short introduction to cryo-electronics, its positives, negatives and a discussion of the most recent advances in this area. Key cryogenic behaviour of FETs is also outlined. This chapter concludes by discussing the origin of the thermal conductivity in insulators, metals and superconductors. Chapter 3 covers the optimisation of the two cryogenic amplifier designs as well as the characterisation of low threshold transistors at low temperatures. Chapter 4 demonstrates the concept of cryogenic threshold engineering in a commercially available FET with both simulation in LTSPICE and with measurements at temperatures down to 1.5 K. Chapter 5 describes the temperature of different parts of a QIP setup as a function of dissipated power and magnetic field. The calibration of novel niobium nitride (NbN) thermometers, used to measure the material temperatures, is also described. Finally, this chapter also demonstrates the effect of superconducting bond wires on thermal paths within this setup. Chapter 6 demonstrates the operation of the voltage noise thermometer, along with a statistical treatment of the cross-correlation procedure. This chapter also contains a method called frequency averaging, which it is possible to speed up the averaging of the cross-correlation method. Finally, Chapter 7 gives a summary and potential further work based on this thesis.

Chapter 2

Background

This chapter outlines the thermometry techniques utilised in this thesis along discussions on both cryo-electronics and the performance of transistors at low temperatures. Section 2.1 first elaborates on the theoretical background, the typical measurement setup, and an example measurement for various thermometers. Section 2.2 presents a concise background on the history and recent advancements in cryo-electronics, and also describes the behavior of key transistor parameters at low temperatures. Finally, Section 2.3 describes the theory behind thermal transport in key materials, such as insulators, metals, and superconductors at low temperatures.

2.1 Thermometry Methods

In this thesis, several different types of thermometry were used as different use cases require different thermometer characteristics. For example, resistance-based thermometers are ideal for use in large temperature ranges and are simple to operate. However, they are typically not primary thermometers and require prior calibration. On the other hand, thermometers such as Coulomb Blockade Thermometers (CBTs) are still relatively simple to operate, can be operated in a primary manner, so do not require calibration, but are limited to only low tem-

peratures (typically less than 4 K). Finally, thermometers based on the Johnson-Nyquist noise are also primary and dissipationless to use, which is extremely beneficial at low temperature but require advanced signal processing and readout techniques. Together, these techniques enable the monitoring of temperature in and around a setup which mimics a quantum computer based upon commercially available silicon technology. The main resistance-based thermometer used in this thesis was a thin film thermometer based on niobium nitride, which are detailed in Section 2.1.1. To calibrate niobium nitride at the lowest temperatures, a Coulomb Blockade Thermometer (CBT) was used, detailed in Section 2.1.2. Finally, in determining the temperature inside ICs at low temperature, typical surface-mounted devices cannot be used because they will not thermalise to the inside of the IC. Therefore, a method of thermometery was used that uses standard resistors inside the IC, voltage noise thermometry, detailed in Section 2.1.3.

2.1.1 Niobium Nitride Thin Film Resistors

2.1.1.1 Background

Resistance based thermometers are widely used in the ultra low temperature regime due to their easy readout and compact size. Today's modern dilution cryostats have many such devices in order to readout the temperature of different stages to better control cooldown. Some of the most popular devices are ruthenium oxide [17], zirconium oxynitride (Cernox) [18], thin carbon film [19], and germanium semiconductor [20]. All of these devices have their use cases, but several have intrinsic limitations. For example, semiconductor devices cannot be used as thin films because of their excessive resistances at low temperature. Ruthenium oxide is suitable for operation down to 20 mK but is only typically useful until 40 K. Cernox suffers from the opposite problem, as they work well all the way to 420 K, but can only be used down to 100 mK.

Therefore, low temperature research has turned to novel materials that can cover a temperature range from room temperature down to 20 mK. One such candidate are Metal-Insulator-Transition materials. An instance of this phenomenon is found in Mott insulators [21], which change from metallic to insulating behavior when the electrons' energy ($\approx \mathrm{k_B T}$) at a particular atomic (or multi-atomic) site is insufficient for the electrons to escape due to the Coulomb interaction. The number of electrons able to leave their sites and become available for conduction is therefore highly temperature-dependent. It then follows that the resistance of the insulator around its transistion temperature is highly temperature dependent. The temperature at which this transition takes place is highly dependent on variables such as pressure and stoichiometry. Although this is a highly simplified description, a full description is beyond the scope of this work.

One such material that displays metal-insulator-like behaviour is niobium nitride, NbN. Its metal-insulator transition temperature is mediated primarily by the ratio of nitrogen to niobium, Γ. For $\Gamma < 0.6$ it behaves as a robust superconductor with a $\mathrm{T_C}$ of 15 K [22]. NbN with this stoichiometry is used in various other applications such as bolometry, single-photon detection [23] and superconductor microwave coplanar resonators. For $\Gamma > 1.1$ it starts to behave as a Mott insulator, and the larger Γ the higher the metal-insulator transition temperature. In the case of $\Gamma \approx 1.6$ the insulator is well suited for thermometry [22, 24]. Typically made as thin films (on the order of 100 nm), these devices can be cooled in liquid nitrogen in order to predict resistances at mK temperatures. The higher the resistance ratio ($RRR_{77K-300K}$) of liquid nitrogen to room temperature, the higher the resistance at ultra-low temperatures. This process is used to help optimise the nitrogen content, so the device is sensitive over a large temperature range.

2.1.1.2 Measurement Setup and Example Measurement

As resistive devices, NbN thermometers are measured using the four-terminal AC measurement method. This is similar to the classic four-terminal resistance method with a current drive and voltage readout. However, the AC technique uses a low frequency sinusoidal current (δI_{In}), as opposed to DC, and the voltage response is demodulated by a lock-in amplifier (δV_{Out}). The ratio of the demodulated voltage response and the AC input current gives the small signal resistance of the device (R)

$$R = \frac{\delta V_{Out}}{\delta I_{In}}. \tag{2.1}$$

Although strictly this equation is frequency dependent, in the limit that the frequency of oscillation is much less than the RC cut-off frequency generated by the device resistance and the parasitic wire capacitance (typically less than 100 Hz) it can be considered frequency independent. Using a lock-in amplifier allows the reduction of the input current magnitude as their excellent signal acquisition capabilities mean that a suitable SNR can be maintained. At low temperatures, the use of low input currents is critical to avoid overheating the device. To minimise noise, it is recommended that the lines connecting the thermometer are low pass filtered in the cryostat at least once. Low pass filtering helps to eliminate the effect of high frequency noise on the NbN. Filtering at the cold plate as opposed to room temperature helps to reduce the Johnson-Nyquist noise from the resistor in the low pass filter. It is also recommended that the device is encased in a metal container to act as a Faraday cage to further reduce the impact of electromagnetic noise. Figure 2.1 gives a typical measurement setup. Figure 2.2 demonstrates a typical resistance curve for the NbN-based thermometer over a wide temperature range. The device was a thin film of NbN that had a $RRR_{77K-300K} = 2.7$, prepared on a silicon wafer. This was attached to a PCB board with GE varnish and bonded with aluminium bond wires. The device was warmed from 1.5 K to 295 K in an Oxford Instruments IO dry fridge (operation detailed in [26]). The V-to-I converter used in this experiment was

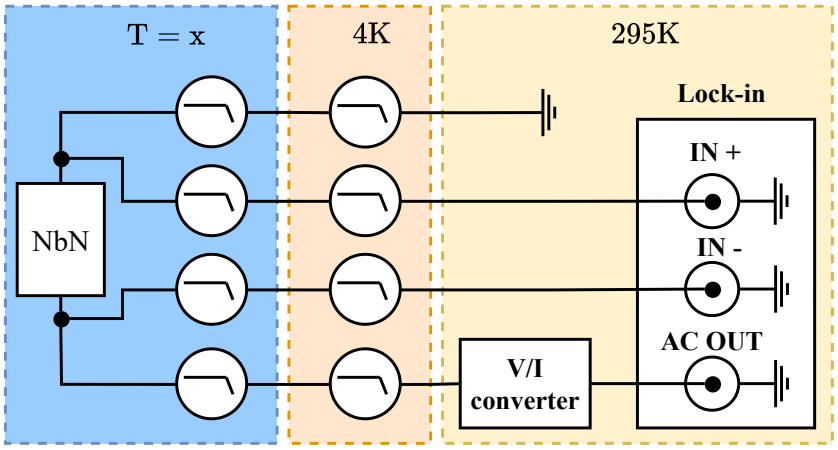

Figure 2.1: Typical measurement setup for NbN thermometer. This is the setup used to readout all NbN thermometers contained within this thesis. Other readout methods such as Wheatstone bridges, are also used [25].

made by Lancaster University and converts to $1\frac{\text{nA}}{\text{V}}$ AC. The frequency used in this case is 71 Hz. An AC excitation of 10 nA was used, keeping the power dissipated in the thermometer to less than 0.12 pW. The voltage was demodulated with a Signal Recovery 7265. In most cases an excitation of 10 nA is excessive (especially at mK temperatures) and will lead to overheating, however, due to the large resistance range this excitation was chosen to keep an acceptable SNR over the whole measurement. To avoid overheating the thermometer, the excitation that should be used to measure the thermometer should be determined by the following. At base temperature, the AC excitation should be swept from low to high slowly and the resistance recorded. This will give a constant resistance that gradually decreases as the thermometer overheats. The thermometer should be operated at an AC excitation just before the resistance decreases for maximum SNR whilst not overheating the device, a typical value of this is 0.2 nA.

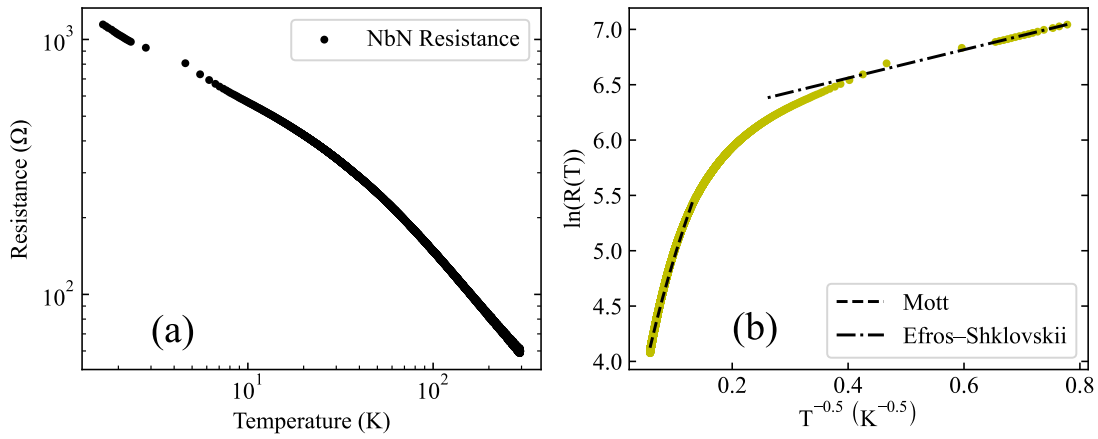

Figure 2.2: a) NbN resistance as a function of temperature. The sparse nature of the points from 3 K to 6 K is due to the rapid boil off of helium-4. b) Temperature dependence of NbN: The generic form of the resistance in Mott-insulator like materials is given by the Variable-range hopping framework [27] and is of the form $R \propto \exp\left(\frac{T_0}{T}\right)^{1/\beta}$ where T is the temperature, T_0 is a material dependent parameter and β depends on the dimension of the material. For materials with n dimensions, $\beta = 1 + n$ so β is typically 4, sometimes given as the Mott dependence. In the low temperature limit β is given as 2, which is know as the Efros–Shklovskii dependence, [28]. This dependence arises from two sources, firstly, the reduction of thermal energy available for electron hopping and limits their hopping range. Secondly a gap in the density of states near the Fermi level, created by electron-electron repulsion, also reduces the possibility for electron hopping. The Efros-Shklovskii dependence can be seen on the linear fitted dashed and dotted line for this plot. This line is a linear $(\mathrm{y} = \mathrm{mx} + \mathrm{c})$ fitting in the low temperature area. However, for higher temperatures, the relationship changes to the Mott $\beta = 4$ [29], this was seen previously in NbN at higher temperatures [24]. This is indicated by the dashed line, which is a square root fit $(\mathrm{y} = \mathrm{m}\sqrt{(\mathrm{x})} + \mathrm{c})$. Crossover between Mott and Efros–Shklovskii has been seen in other metal-insulator materials [30, 31].

2.1.2 Coulomb Blockade Thermometry

2.1.2.1 Background

Another type of thermometer used in this work is the Coulomb Blockade Thermometer (CBT) [32, 33, 34]. The most fundamental version of this device is a single metal island, separated by insulation on either side but connected to metal after the insulation on both sides. As such, if the insulation is thin enough, any electrons on the island are able to tunnel through the insulation on either side. In order for electrons to flow, we must be able to charge the central island with at least one electron. This central island has a capacitance $\mathrm{C_{tot}}$, which is the sum of the contributions to the ground and the capacitance to the near-by metal. From the equation for charging a capacitor, the energy required to charge the central island, or charging energy, $\mathrm{E_C}$, is given by

$$E_C = \frac{e^2}{2C_{tot}}. \tag{2.2}$$

If electrons in the environment have energy $\mathrm{E_C} = \mathrm{k_B T}$ then there are three possible scenarios for the conductance of the CBT.

1. $\mathrm{k_B T} \gg \frac{\mathrm{e}^2}{2\mathrm{C_{tot}}}$: In this case electrons have enough energy from the environment and will flow with some tunnel resistance, $\mathrm{R_T}$. This value will depend on the geometry and material parameters of the CBT.

2. $\mathrm{k_B T} \approx \frac{\mathrm{e}^2}{2\mathrm{C_{tot}}}$: Here, the tunneling of electrons and hence the resistance (or conductance) of the device will be heavily influenced by a temperature change. Measurements of the device's resistance can therefore help determine the temperature.

3. $\mathrm{k_B T} \ll \frac{\mathrm{e}^2}{2\mathrm{C_{tot}}}$: In this scenario, the CBT acts as a Coulomb blockade and requires an external bias to start conduction.

Modern CBTs use junction arrays to reduce resistance to simplify measurement. Single junction arrays can also be prone to errors [35]. The CBT geometry

and materials are engineered so that Scenario 2 is true at low temperatures, more specifically the island capacitance values. For lower temperature operation, higher capacitance values are typically used [36]. The CBT is primarily operated by varying the external bias across the device while monitoring the conductance of the device. At zero bias, there will be a dip in conductance as a result of the partial coulomb blockade created by scenario two. The width of this dip is determined by the temperature of the tunneling electrons in the devices. An example of this is given in Figure 2.4. More specifically, the full width half maximum voltage (FWHM), $V_{\frac{1}{2}}$ of this dip is given by,

$$V_{\frac{1}{2}} = 2 \times 5.427 \frac{k_B T}{e}, \tag{2.3}$$

the derivation of which is beyond the scope of this work but is dealt with in more detail in [36]. As this contains no empirical constants, this method is considered a primary form of thermometry.

CBTs are typically used to accurately determine electron temperatures at extremely low temperatures, either low milli-kelvin or even micro-kelvin environments. The electron-phonon coupling is extremely weak in these environments, often meaning the electron temperature greatly exceeds the phonon temperature. CBTs are advantageous as they are primary electron thermometers, capable of accurately determining the extent to which the electron temperature is separated from the phonon or nuclei temperatures. Examples of the use of CBTs for exploring extremely low temperature are in adiabatic demagnetisation cooling [37] and immersion cooling [38].

2.1.2.2 Measurement Setup

To use the CBT we use the four-terminal method described in the previous section. A low frequency, low current (typically 1 nA or less depending on SNR) AC current is applied in addition to a DC bias current. Both AC and DC voltages are

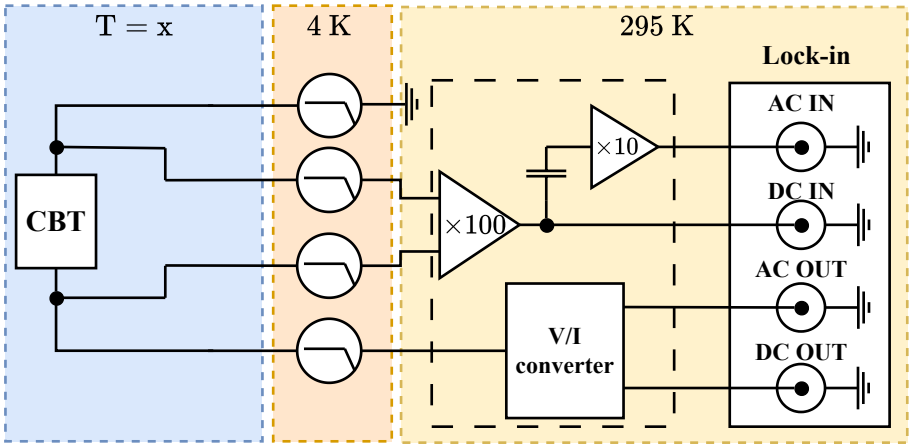

Figure 2.3: Example CBT measurement set up. The DC voltage offset is determined by demodulating at 0 Hz using the lock-in. The electronics in the dashed line box is provided by Aivon Oy. The DC voltage output is converted by the V/I converter to provide a DC bias across the CBT. The other amplifiers are necessary to boost the SNR of the both AC and DC signals.

then read out by a lock-in amplifier to give the conductance and bias voltage across the device, respectively. The DC current is stepped so to capture the conductance dip as well as the plateau's in conductance either side. Figure 2.3 gives an example setup. Although this method is primary, the need to sweep DC bias means that it has poor temporal resolution. To perform faster measurements with the CBT can be used in a self calibrated, secondary manner. To do this, the value of the conductance at zero DC bias across the device is monitored. As this is a single value this increases the temporal resolution. However, this mode requires the capacitance of the islands and the tunneling resistance to be well known. This is achieved by measuring the CBT at several different known temperatures in order to extract these values by fitting the data to a tunneling model. Then a lookup table can be generated that gives the resistance (or conductance) at zero bias as a function of temperature. Figure 2.4 gives an example of several temperatures fitted to extract these parameters. During this measurement both amplifiers and the I-V converters are encased within singular packaging, provided by Aivon Oy.

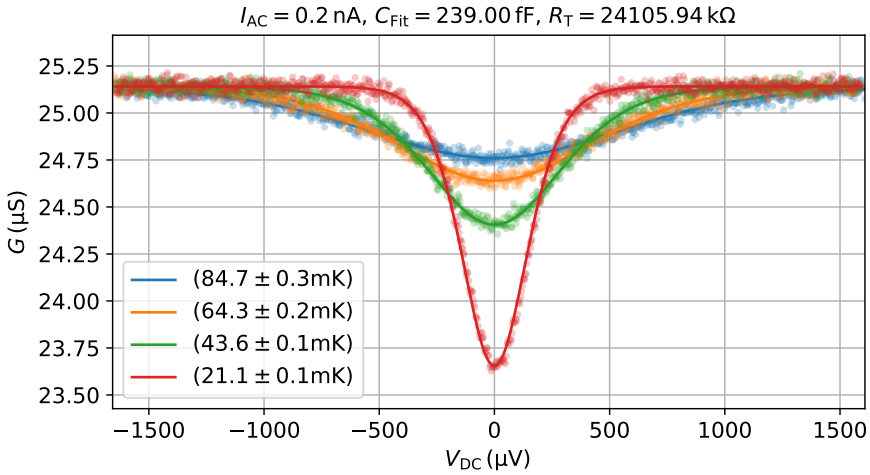

Figure 2.4: CBT example measurement. This plot and the fits on the plot were generated by J.R Prance and the data was gathered by the author. Above the plot the tunnel resistance and CBT capacitance extracted from the fits of the data from a full tunneling model.

The AC excitation used to measure in this example was 0.2 nA at 81 Hz. Given a characteristic resistance of $40\ \text{k}\Omega$ and a 0.2 nA current the power dissipated in the device by this measurement is ≈ 0.3 fW. The AC current converts to $1\frac{\text{nA}}{\text{V}}$ and the DC current converts at $100\frac{\text{nA}}{\text{V}}$. The lock-in amplifier used was a Zurich Instruments MFLI.

2.1.3 Voltage Noise Thermometry

2.1.3.1 Background

The measurement of the current or voltage response of the thermal agitation of charge carriers forms the basis for many thermometers, over an extremely broad temperature range [39]. This type of thermometry is particularly attractive for ultra low temperatures as it is fundamentally non dissipative and primary. Limiting power dissipation into the cryostat is critical for experiments in the mK regime (or lower) in order to maintain the fragile quantum states being explored. Its primary nature is also important at low temperatures in order for discoveries in fundamental physics to be repeatable. Recently, techniques such as Current Sensing Noise Thermometry (CSNT) [40, 41] and Magnetic Field Fluctuation Thermometry (MFFT)[42] have pushed the boundaries of noise thermometry in terms of both minimum temperature and precision. This is primarily due to the use of SQUIDs as very low noise pre-amplifiers, maximising the SNR to improve sensitivity. While these thermometers are fantastic examples of the cutting edge of noise thermometry, they are difficult to implement in more general settings because of the use of SQUIDs, which require specialist knowledge to operate, and are static sensitive. In the context of In-IC thermometry, these techniques are not as suitable due to this bottleneck.

An iteration of this technique that has broader applicability is voltage noise thermometry without the use of SQUIDs. This significantly decreases the barriers to entry of this technique, as any suitable resistor can now be a thermometer, including devices inside an IC. The most general form for the voltage noise across a resistor, which includes the zero point motion of the photon field, is [43]

$$\bar{V_T^2}(F) = 4hfRe(Z)\left(\frac{1}{2} + \frac{1}{\exp\left(\frac{hf}{k_BT}\right) - 1}\right)\Delta f \tag{2.4}$$

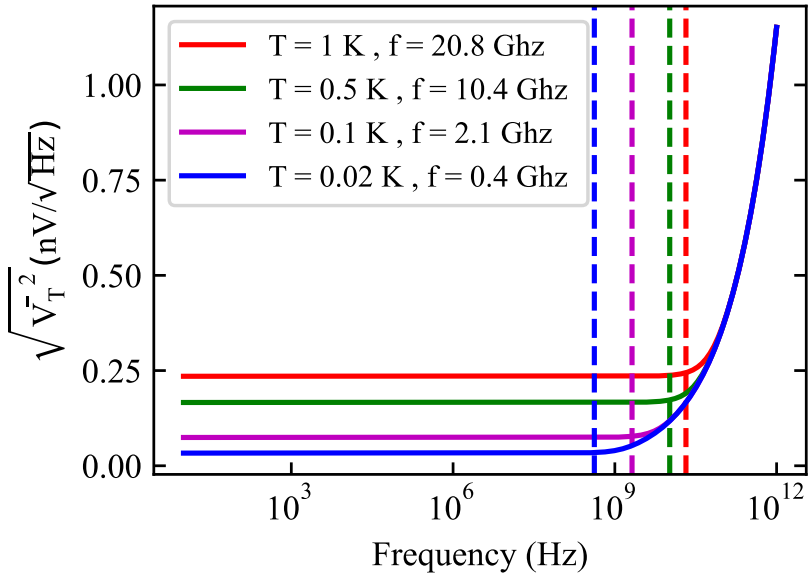

Figure 2.5: Spectral density in a 1 Hz bandwidth of a $1\ k\Omega$ resistor plotted as a function of frequency for different temperatures. The frequency in the legend denotes the frequency at which the photon energy is equal to the thermal energy, i.e. $f = \frac{k_B T}{h}$, below this frequency the spectral density is no longer frequency dependent.

where k_B is the Boltzmann constant, f is the frequency, h is Planck's constant, $Re(Z)$ is the resistance of the resistor and T is the temperature that the resistor is thermalised at. In the case that the thermal energy dominates over the photon energy, $T_e k_B >> hf$, this can be simplified to the Johnson-Nyquist theorem [44, 45],

$$\bar{V_T^2} = 4k_B T R \Delta f. \tag{2.5}$$

It should be noted that in the case of simultaneously high frequency and low temperatures, Eq. 2.5 starts to be invalid and the full description in Eq. 2.4 should be used. For example, at 1 K, the frequency spectrum of the Johnson-Nyquist noise stops being constant at 20 GHz [46] this frequency value decreases with temperature, as shown in Fig. 2.5. In the case of measuring the power spectral density across the resistor, S_D^2, within a 1Hz bandwidth, the Johnson Nyquist

formula can be further re-written,

$$S_D^2 = 4k_B TR. \tag{2.6}$$

By accurately knowing the resistance, the resistor can act as a primary thermometer as there are no empirical values within the formula. The temperature of the resistor is then given by,

$$T = \frac{S_D^2}{4k_B R}. \tag{2.7}$$

The Johnson-Nyquist theorem doesn't state that electrons have to be the charge carriers in the resistor which the noise is being measured in. This is particularly advantageous in the case of In-IC thermometry as many resistors are p-type doped (the resistance of which is approximately constant at low temperatures due to dopant freezeout).

2.1.4 Cross-Correlation

To be able to measure noise below the intrinsic noise of the amplifier measuring the voltage noise, cross-correlation must be used. This requires the simultaneous recording of voltage as a function of time using two amplifier channels. The basis of cross-correlation is that the voltage across amplifiers 1 and 2, $V_1(t)$ and $V_2(t)$, share a common signal, $V_\Omega(t)$, in addition to a noise component that is unique to the input of the different amplifiers, $V_{1:n}(t)$ and $V_{2:n}(t)$. In the context of noise thermometry, $V_\Omega(t)$ represents the voltage contribution of the thermal noise of the resistor. This is represented by,

$$V_1(t) = V_\Omega(t) + V_{1:n}(t), \tag{2.8}$$

and

$$V_2(t) = V_\Omega(t) + V_{2:n}(t). \tag{2.9}$$

The cross-correlation spectrum, S_{cc}^2, is calculated by the following,

$$S_{cc}^2(f) = \tilde{V}_1(t)^* \cdot \tilde{V}_2(t). \tag{2.10}$$

Where the tilde represents the Fourier transform. To attenuate uncorrelated noise, this is averaged n times, giving $\langle S^2_{cc}(f)\rangle_n$. With sufficient averaging, this computation approaches the Fourier transform of the shared signal,

$$\langle S^2_{cc}(f)\rangle_n = \tilde{V^2}_{\Omega}(f). \tag{2.11}$$

The magnitude of this spectra is computed (so it is no longer complex) and linearly scaled due to the use of the Hanning window during the use of the Fourier transform. The use of windowing is important to avoid spectral leakage. To calculate a final temperature from the spectra an average in a frequency range $f_1 - f_2$ encompassing m points is calculated, which is given mathematically by,

$$S^2_D = \frac{1}{m}\sum_{i=f1}^{f_2} \mathrm{Corr}[\langle S^2_{cc}(f_i)\rangle_n], \tag{2.12}$$

where the correlation operator, $\mathrm{Corr}[]$, takes the magnitude of the spectra and takes into account the Hann window scaling factor. This is subsequently converted into a temperature using the Johnson-Nqyuist formula.

2.1.4.1 Measurement Setup

Figure 2.6 gives a typical measurement set up for a cross-correlation voltage noise measurement. When performing this measurement one parameter of note is the cut off frequency (the half power frequency), $\mathrm{f_c}$, which is created between the resistor and the wire capacitance. This will limit the range in which the noise can be considered white, and hence limits the range of frequencies it is possible to average from. The $\mathrm{f_c}$ is given by,

$$f_c = \frac{1}{2\pi R C_{wiring}}. \tag{2.13}$$

Here R is the resistor resistance and C_{wiring} is the wiring capacitance. To maintain as high a possible $\mathrm{f_c}$, it is important to reduce the capacitance of the cable. The primary method to do this is to reduce the length of cabling to the sample (this would also simultaneously reduce the amount of pickup noise). As for the

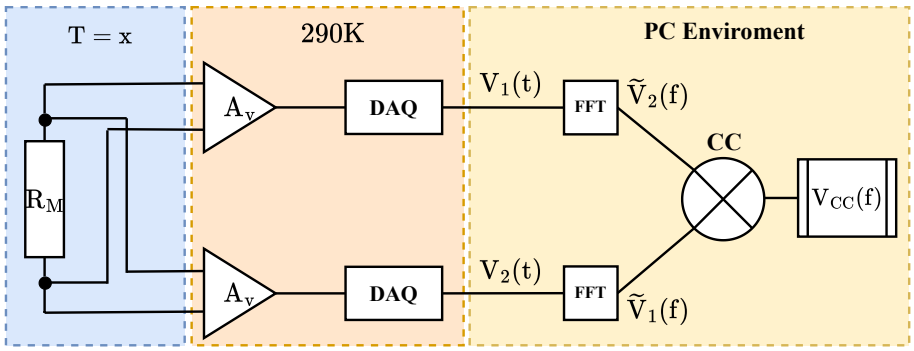

Figure 2.6: Cross-correlation voltage noise setup. Here the DAQ devices could be monolithic DAQs, digiter cards in a PC or a FPGA based lock-in amplifier. The amplifiers should be as low noise as possible so to reduce the number of cross correlation averages. The CC denotes the process of cross-correlation.

resistance, a balance must be struck between increasing f_c and maintaining a high SNR. Too large a resistance and f_c will be prohibitively low, too small a resistance, and the thermal noise may not be measurable. An advantage of a high f_c is the ability to use a fast sampling rate. This would allow for either more points in a spectra or more spectra to be taken within the same time period. The advantage of taking more spectra is that the SNR can be improved by cross-correlation. Figure 2.7 shows an example of measurement in which six resistors were measured at room temperature, some of which have a power spectral density above the intrinsic noise of the amplifiers used and some below. We used resistors with noise below the noise of the amplifier to verify our cross-correlation calculation. The resistors used in this experiment are the Vishay MBB0207 Series Axial Thin Film Fixed Resistors $(10\,\mathrm{k\Omega}, 3.3\,\mathrm{k\Omega}, 1\,\mathrm{k\Omega}$ and $270\,\mathrm{k\Omega})$ which are standard laboratory resistors. The amplifiers used in this experiment were two SRS560 amplifiers set on 5000 gain, in low noise mode, and with a 1 kHz filter. The DAQ used was an NI USB-6215, we used a sampling rate of $2^{16}\mathrm{S/s}$ and collected 2^{16} samples, giving us a one second acquisition time per spectra.

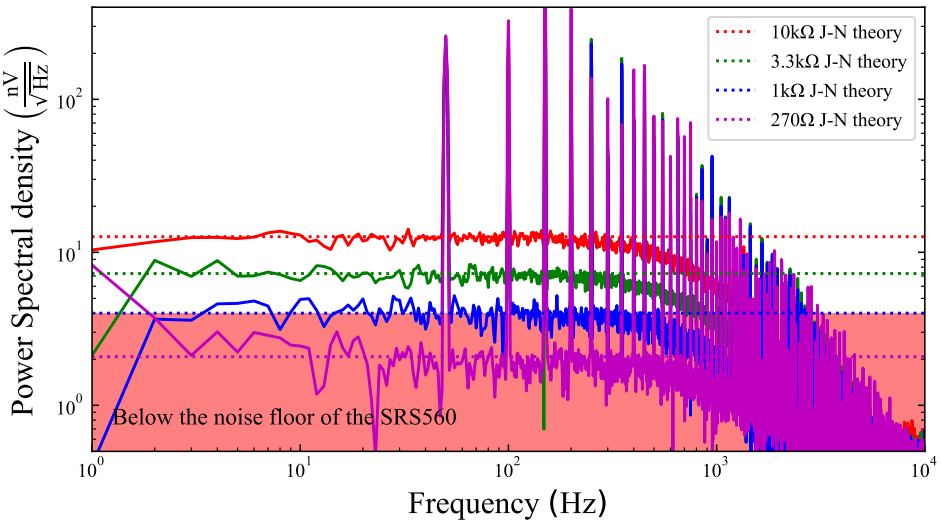

Figure 2.7: Cross-correlation spectra for four different resistance values at room temperature. Each of these spectra is the results of 100 averaged cross-correlations. Strong agreement is shown between the Johnson-Nyquist theory value and the value power spectral density of the cross-correlation. The red shaded area demonstrates the area below $4\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$, which is the amplifiers input noise. This plot shows that by performing cross-correlation we can resolve noise levels at and below this level, as shown in the case of both the $1\ \mathrm{k}\Omega$ and the $270\ \Omega$ resistors.

2.2 Silicon based Cryo-electronics

This thesis discusses a range of use cases for cryo-electronics, as such it is important to take a broad look at the background of the subject. In this Section, Subsection 2.2.1 takes a brief look at the history of cryo-electronics and the positives and negatives of cooling electronic devices in general. It also discusses the current bleeding edge of the subject. Subsection 2.2.2 details the change in common transistor characteristics at low temperature, which gives important contexts for the rest of the thesis.

2.2.1 Cryo-electronic Background

During the 1960s, the work performed by Atalla [47] enabled the large-scale manufacturing of MOSFETs. In the decades following this, innovations in manufacturing and MOSFET design reduced size and leakage currents allowing for its Very Large Scale Integration (VLSI) in many products. The continuous shrinkage of devices which led to both Moore's Law [48] and Dennard scaling [49] transformed semiconductors into a trillion dollar industry [50]. Research into cryo-electronics has proceeded along side research into fundamental electronics devices like the MOSFET. During the early days of MOSFET research, researchers began to cool a range of semiconductor devices to further primary research on these relatively new materials [51, 52, 53, 54, 55]. It was not until the 1970s and 1980s that full electronic devices started to be cooled down. Firstly motivated by both academic research, particularly for cold amplifiers [56, 57, 58, 59, 60, 61, 62, 63] in order to increase the SNR of very small signals used at cryogenic temperatures. Secondly, more research began to take place for applications in cryogenic circuits for space applications [64, 65]. Fundamental research also increased in semiconductor devices as access to cryogenic environments increased in universities throughout the world. This included measurements into noise and key characteristics of semiconductor devices such as FETs, i.e. threshold voltage

and subthreshold swing [66, 67, 68, 69, 70]. As research accelerated on all fronts, driven by the burgeoning computational potential of the CMOS process, more complex devices were eventually cooled. The first example of large scale cryogenic electronic operation is the ETA nitrogen cooled supercomputer [71].

The physics of the positive effects on material properties which have driven further research into cryogenic electronics for a large variety of applications can be summarised as:

- *Increase in drift velocity* As the temperature reduces, electron-phonon scattering also reduces, increasing the carrier mobility inside semiconductor devices. This also contributes to a higher saturation velocity and in transistors a higher saturation current [72]. This also increases the transconductance (the transistor parameter which determines the ability of a transistor to control the output drain current with respect to changes in its gate voltage) at low temperature, leading to an increase in gain in some amplifiers at low temperature.

- *Increased metal conductivity* Reduced phonon scattering at lower temperatures increases the conductivity of metals at low temperature. The main positive effect this has is the reduction in the delay caused by interconnect RC delays [71], especially in large-scale computing.

- *Reduced subthreshold slope* The subthreshold slope is the transistor parameter which determines the how quickly the transistor turns from its on state to its off state. As this reduces with temperature, it enables faster switching between the transistor on and off states which saves power in switching electronics.

- *Reduction in leakage currents* Off-state currents in MOSFETs are reduced due to subthreshold slope sharpening. Other leakage routes such as drain-gate leakage, drain-drain processes such as punch through and drain-bulk

leakage are also reduced due to reduced thermal energy [73].

- *Reduction in thermal noise* Thermal noise is reduced due to the Johnson-Nyquist formula having an explicit temperature dependence [44]. This is particularly beneficial for amplifiers to increase the SNR of sensitive experiments.

However, there are negatives to operation at low temperatures; these can be roughly summarized as follows.

- *Temperature related transport effects* Effects such as the kink effect are prevalent in larger [14] MOSFET devices at cryogenic temperatures driven by freezing out of carriers. Effects such as these necessitate the development of bespoke low temperature models [74], of which there are even today relatively few [11, 75, 76].

- *Increased threshold voltage* Widely reported, the threshold of MOSFET devices increases due to scaling of the Fermi potential within the bulk [77]. This drives the operating voltage cryo-electronics up.

- *Increased transistor mismatch* Current research suggests that mismatch in subthreshold behavior [78, 79] and threshold voltage [80] can increase at low temperatures. However, this mismatch is also related to the bias point in cooling [81] and also geometric considerations related to mechanical stress [82].

- *Decreased reliability at deep cryogenic temperatures* Transistor degradation can increase at low temperatures. Firstly, through hot electron effects, high energy electrons that are injected into the gate oxide and cause can cause damage. Secondly, mechanical stress induced by thermal mismatch between the different materials present in transistors can cause them to malfunction. Both of these issues can lead to a decrease in long-term reliability at low temperatures [83, 84].

Despite the benefits of cooling cryogenic electronics, in most cases, its cost and complexity outweigh the increases in performance for large scale computing after $\approx 100\ \mathrm{K}$ [85]. As such, cryogenic electronics at liquid helium temperatures, instead of being used for general computing, are seen as more of a supporting role for other cryogenic technologies.

The most active research area is quantum computing. The need to scale quantum computers, and the subsequent increases in wiring into the cryostat are non-commensurate due to the increase in heat leak into the cryogenic environment. Lack of cooling power could mean higher base temperatures and compromise qubit performance. As such, classical electronics are now commonly collocated near or next to the electronics in order to eliminate the number of wires into the cryostat and allow quantum computers to scale. Several comprehensive reviews are available on the subject of cryo-electronics for the integration and management of quantum computing systems [14, 86, 87]. To control and measure the qubits at mK temperatures, a host of electronics is needed. This includes, but is not limited to, RF electronics to facilitate input signals and improve the SNR ratio of the output signal[88, 89], DACs to appropriately bias the qubits [90, 91], ADCs to digitise the output [92, 93] and digital controllers such as FPGAs [94, 95]. Some of the most advanced chips combine these capabilities, in single chips at base temperature [96], chiplet approach [97], or multistage readout [98].

2.2.2 Behaviour of Silicon Transistors at Low Temperatures

2.2.2.1 Increase in Threshold Voltage

The increase in threshold voltage in low-temperature FETs is well documented, with typical increases of several hundred millivolts in recent technologies[99, 100], although this does depend on the method of threshold extraction used [77, 101]. This has implications for the design and operation of devices in

cryogenic environments. For example, higher thresholds may require higher supply voltages, which could cause higher power consumption. To understand the cause of the threshold voltage increase, we will start from its definition and identify the temperature dependencies. Beckers et al [77] and Tsividis [102] were used to form the backbone of the following work, with further comments added by the author. The threshold voltage in the low source drain bias and zero source body bias is given by,

$$V_{Th} = 2\Phi_F + \phi_{ms} + \Gamma_b\sqrt{2\Phi_F}. \tag{2.14}$$

Where Φ_F is the Fermi potential in the bulk, ϕ_{ms} is the metal-semiconductor work function and Γ_{b} is the body factor which introduces the contribution of the depletion charges. The Fermi potential of the bulk is the most important term in this formula as Γ_{b} has no explicit temperature dependence, the influence of ϕ_{ms} is assumed to be small [77] and the Fermi potential has both a linear and square root term. This is given by,

$$\Phi_F = \phi_T \ln\left(\frac{N_A}{n_i}\right) \tag{2.15}$$

where ϕ_{T} is the thermal voltage, $\phi_{\mathrm{T}} = \frac{k_B T}{q}$ (where k_B is the Boltzmann constant, T is temperature and q is the electron charge), $\mathrm{N_A}$ is the acceptor concentration and $\mathrm{n_i}$ is the intrinsic carrier concentration. The acceptor concentration is considered by to be constant at low temperatures, as even when this factor is taken into account it was found to have negligible difference on the magnitude of threshold increase [77]. This is partly because despite the fact the acceptors get frozen out, they are also ionised again by large gate or drain voltages [103]. The intrinsic carrier concentration is given by,

$$n_i = \sqrt{N_C N_V}\exp\left(\frac{-E_g(T)}{2\phi_T}\right). \tag{2.16}$$

As this equation tends to infinity at low temperatures, it is much more convenient to expand the natural logarithm. This is expanded into

$$\Phi_F = \phi_T\left[A + \frac{3}{2}\ln(\phi_T)\right] + E_g(T)/2, \tag{2.17}$$

where $\mathrm{A} = \ln(\mathrm{N_A}) - \ln\left(\sqrt{\alpha\beta}\right)$. Where $\mathrm{E_g(T)}$ is the electron bandgap for silicon, this can be ignored as the change is small [104]. The constants α and β derive from the expressions for the effective density of states in the conduction and valance bands, which also contain temperature dependencies. As such,

$$N_C = 2\left(\frac{2k_B T m_e^* \pi}{h^2}\right)^{3/2} \tag{2.18}$$

which can be re written as,

$$N_C = 2\left(\frac{q2m_e^* \pi}{h^2}\right)^{3/2}\left(\frac{k_B T}{q}\right)^{3/2} = \alpha\phi_T^{3/2}. \tag{2.19}$$

Finally this means that

$$\alpha = 2\left(\frac{q2m_e^* \pi}{h^2}\right)^{3/2}. \tag{2.20}$$

This is reproduced for N_V in order to generate β,

$$\beta = 2\left(\frac{q2m_h^* \pi}{h^2}\right)^{3/2}. \tag{2.21}$$

For the purpose of the modelling here, we assume that the effective mass of electrons and holes, $\mathrm{m_e^*}$ is constant throughout the temperature range explored. This is approximately true for electrons but not for holes [105]. Unpacking Equation 2.17 with the expressions for the density of states in the conduction band and valance band, leaves us with a simplified expression leaves the Fermi potential, where $\Delta = \sqrt{\alpha\beta}$

$$\Phi_F = \phi_T\left[\ln(N_A) - \ln(\Delta) + \frac{3}{2}\ln(\phi_T)\right], \tag{2.22}$$

which means that,

$$\Phi_F \propto \phi_T - \phi_T \ln(\phi_T). \tag{2.23}$$

This demonstrates that at the Fermi potential will increase and eventually tend to a constant at low temperatures.

2.2.2.2 Subthreshold Swing

The subthreshold regime of FET operation is the regime in which the source-drain current is exponentially dependent on the gate voltage across the FET. This regime lies between the on and off states and starts just prior to the threshold voltage, and as such its characteristics are important for logic systems. Ultra low power electronics also rely on this regime to be part of analog devices such as amplifiers because of the low current output in this state. The most common unit used to describe this state is the subthreshold swing, measured in mV/dec, the ratio of the gate volage required to change a decade of current. For logic devices, it is beneficial if this value is small, so that the devices can be easily turned on or off. Therefore, much research has been devoted to reducing the subthreshold swing in devices. The temperature dependence of the subthreshold swing (SS) is given by,

$$SS = \epsilon_{SS}\frac{\ln(10)k_BT}{q} \tag{2.24}$$

where ϵ_{SS} is a factor that depends on the various capacitive contributions of the gate oxide, depletion region and interface states [12]. Equation 2.24 gives a theoretically minimised predicted value of SS of $60\mathrm{mV/dec}$ at 300K and $0.8\mathrm{mV/dec}$ at 4.2K at $\epsilon = 1$. At room temperature, this theoretical value is not reached due to a non-unity ϵ. At lower temperatures, the SS saturates and has been attributed to interface traps close to band edges [106].

2.2.2.3 The Kink effect

One key effect that can occur in FET devices at low temperature is the 'kink effect' [107]. This described by the a step change in the drain-source characteristics at low temperatures. Commonly found in older devices typically larger than 160 nm [14], this can contribute to the failure of electronics at low temperature. The cause of this effect is a combination of carrier freeze out at low temperatures and impact ionisation. Carrier freezeout is the inability of electrons (or holes in the p-type case) to enter the conduction band due to a lack of thermal energy. This causes a

large increase in the substrate resistance in the FET. Impact ionisation occurs when a high energy charge carrier collides with a electron that is located in a bound state. This electron is knocked from the state causing an electron-hole pair to be formed. Most of the electrons will flow to the drain but a small fraction will flow through the substrate to ground. In the case of the transistor being at low temperature, the increased substrate resistance means that a large voltage is dropped across the substrate. This consequently decreases the threshold voltage and creates the 'kink', or the step change in the drain-source characteristics [108]. Smaller, more recently developed technologies are not affected by this phenomenon because of the increased vertical electric fields, resulting from the reduced oxide layers in these technologies. Higher vertical electric field, causes mobility degradation which in turn, suppress impact ionization [87]. Demonstration of the kink effect can be seen in Figure 2.8.

2.3 Thermal Transport at Low Temperatures

To effectively discuss thermal management in cryogenic electronics, the thermal conductivity of the key materials present in these devices should be discussed. This is because at low temperatures, the thermal conductivity becomes highly non-linear, resulting in the formation of non-intuitive thermal paths. The key materials used, insulators, metals and superconductors have unique temperature dependencies and origins of their thermal conductivity's. The thermal boundary resistance (TBR) also has increasing importance at low temperature in comparison to higher temperature operation.

In its most general form, the thermal conductivity $\kappa(T)$ of a material is given in Fourier's heat equation [109],

$$\dot{q} = \kappa(T)\nabla T \tag{2.25}$$

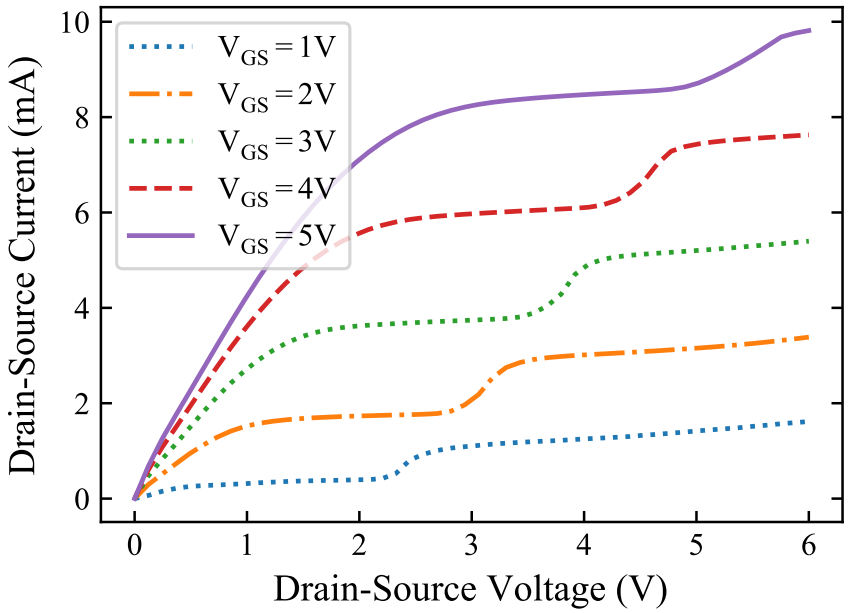

Figure 2.8: Example of the kink effect at 1.5 K. Here a ALD110800 zero threshold n-type FET was cooled and had its drain-source characteristics to taken as a function of its gate-source characteristics. The kink moves towards higher drain-source voltages for higher gate-source voltages as the higher gate source voltages suppress the scattering which causes the impact ionisation [12].

where $\dot{q}$ is the heat current density and ∇T is the thermal gradient the heat current moves through. In the case of a rod with cross section A and length L this can be simplified to,

$$\dot{Q} = \frac{A}{L}\kappa(T)\partial T, \tag{2.26}$$

where $\dot{Q}$ is the total power passing through the cross section. Functionally, $\kappa(T)$ is usually given in the form,

$$\kappa = \Lambda T^n, \tag{2.27}$$

where both Λ and n are material dependent. If we now integrate Eq. 2.26 we arrive at with,

$$\dot{Q} = \frac{A}{L}\Lambda\left[\frac{T_H^{n+1} - T_C^{n+1}}{n+1}\right]. \tag{2.28}$$

Different materials have different values of both n and Λ, in particular n gives us insight into the dominating thermal conduction process in a material.

In the case of pure metals, $n = 1$ in the low temperature limit. This is because in most metals after approximately 4 K, the electron contribution to the thermal conductivity becomes stronger than the phonon [109]. The electron contribution is proportional to temperature due to the behaviour of Fermi gases in the low temperature limit, which is outlined further in Appendix B. Impurities in metals can change n at low temperatures, one example of this is the Kondo effect [110], in which the conduction electrons are scattered by the magnetic moments of the impurities. This leads to a change in the resistivity of the metal and therefore its thermal conductivity.

Insulators on the other hand have phonons as their dominant thermal conductivity mechanism. This is because the electrons are locked out of transport by strong valance bonds, and as such contribute much less to the total thermal conductivity. In the low temperature regime, the temperature dependence of the phonon population gives $n = 3$ in an ideal insulator modelled as a phonon gas, as derived in Appendix A . However, this idealised model doesn't give the whole

picture. In materials such as plastics, can be strongly disordered and have many phonon scattering sites, which can introduce a temperature dependence to the mean free path of a the phonons. As such n can range from 1 to 3.

Another important thermal conductivity to consider is that of pure metal superconductors. These are abundant at low temperatures in aluminium wire bonds, readout electronics and even in the gate structures of advanced CMOS modes used at low temperature. The defining feature of superconductivity, is that some of the electrons in the superconductor exist in Cooper pairs, which all sit at the same energy level in a Bose-Einstein condensate. While electrons are bound in this state they cannot take part in heat transfer as they carry no entropy. However, there is an energy band gap of ΔE between the energy state of the Cooper pairs and the unpaired electrons, which can facilitate the flow of heat. The number of unpaired electrons decreases exponentially with temperature [111], as such the conductivity of a superconductor, κ_s, can be given by,

$$k_s \propto T \exp\left(\frac{-\Delta E}{k_B T}\right), \tag{2.29}$$

while there are electrons available for thermal transport. However, in the very low temperature case ($T < T_C/10$), where T_C is the critical temperature of the superconductor, the number of electrons available for thermal transport becomes negligible. This leads to the temperature dependence turning to purely phononic, or $n = 3$.

The TBR, between materials has significant impact on thermal transport at low temperature. This was first bought to the attention of the wider low temperature community in 1941 when Kapitza [112] measured a large thermal resistance between helium-4 and copper. TBR is typically described by a slightly adjusted version of Fourier's heat equation,

$$R_K \dot{Q} = \Delta T, \tag{2.30}$$

where ΔT is the temperature difference between two surfaces, $\dot{Q}$ is the heat across it and R_K is either the Kapitza resistance or the TBR (the term Kapitza resistance should be reserved for the copper to helium-4 boundary and TBR more generally the thermal resistance between two boundaries, however literature sometimes confuses these terms). This was later understood by modelling thermal transport on the exchange of phonons from phonon gases present in two different materials [113]. In the case of copper to helium-4, this logic can be used alongside Snell's law to show $R_K \propto AT^3$. Modern models such as the Acoustic Mismatch Model AMM and Diffuse Mismatch Model DMM [114] offer more reasonable agreement with theory but TBR remains largely difficult to reproduce in different material combinations. This is due to many factors, including that the area in which the thermal transport takes place is typically poorly defined. One reason is microscopic surface asperities, which in the case of metal-metal contact can mean the actual contact area which phonon transport takes place is 10^{-6} [111] the size of the assumed contact area. There is no one solution to this issue, but increased force between the surfaces as well as adding vacuum grease reduces this thermal resistance. Vacuum grease helps to decrease thermal boundary resistance by increasing the effective contact area by filling in the microscopic asperities mentioned previously.

Chapter 3

Development of Low Voltage, Low Power Cryogenic amplifiers

This chapter describes the attempted development of low supply voltage, low power consumption cryogenic amplifiers using commercially available FETs. Typically cryogenic amplifiers have high power consumption (on the order of hundreds of μW or single digit mW). This requires the amplifiers to be placed at the 4 K stage on a refrigerator to access the increased cooling power provided by a pulse tube. In the example of a typical dilution refrigerator, this can mean the sample is sat up to half a meter away from the amplifier. This can bring difficulties to readout. In the case of high frequency amplifiers, this means that complex matching networks are necessary to compensate for the impedance of the added cabling. In the case of low frequency amplifiers the parasitic capacitance limits the bandwidth due to a RC cut off filter formed between the paracitic capacitance and the sample resistance. The extra wiring can also couple to external noise sources capacitively and inductively. By designing low power amplifiers we can reduce these effects by placing them at lower stages where the total available cooling power is reduced. The low power nature of these FETs derives from their low threshold voltages, meaning any amplifiers developed can be operated at lower supply voltages, in comparison to HEMTs for example.

This chapter outlines the design, and subsequent optimisation of two different DC-coupled voltage amplifier topologies that were designed with zero threshold transistors. Both amplifiers were optimised by changing the resistance of passive load resistors *in situ*.

Section 3.1 details the characterisation of the transistors used in the experiment, performed with Oxford Instruments, which resulted in an application note [115]. It also details measurements of the resistors used in the final amplifier design. Section 3.2 discusses the first amplifier design, its simulation in LTSPICE [116] and characterisation at low temperatures. A Figure Of Merit (FOM) is also discussed so both amplifier designs could be compared. Section 3.3 discusses how the second amplifier was designed to minimise power consumption, and demonstrates its testing at cryogenic temperatures. Section 3.4 compares the two amplifiers and gives a summary of the work. Section 3.5 concludes the work and provides commentary on potential further work.

3.1 Device Characterisation

This section details the cryogenic measurements of the devices used in Chapters 3 and 4, both transistors and resistors. The measurements of transistor transport properties are detailed in Subsection 3.1.1. Subsection 3.1.2 gives an analysis of the threshold voltage as a function of temperature and finally Subsection 3.1.3 demonstrates low temperature characterisation of the resistors used in the amplifier. Furthermore, effects that are seen only at cryogenic temperatures are analysed and discussed

3.1.1 Transistor Transport Measurements

In this experiment, three commercially available low threshold MOSFETs were measured, the ALD10800, $V_{Th} = 0$ V n type, ALD310700, $V_{Th} = 0$ V p type, and ALD114904, $V_{Th} = -0.4$ V n type depletion MOSFET. All of these devices are manufactured by Advanced Linear Devices and are available commercially. Both the ALD310700 and ALD10800 came in 16 pin SOIC packages, while the ALD114904 came in an 8 pin SOIC package. All of these devices are packaged in matched pairs, and individual devices are checked for the matching of key FET parameters such as transconductance and output conductance. Matching is particularly important in minimising the reduction performance in circuits such as differential amplifiers. These MOSFETs were specifically chosen to study low-threshold enhancement n and p-type MOSFETs, as well as highly doped n-type depletion MOSFETs. This would allow us to identify differences between n-type and p-type behaviour as well as enhancement and depletion type MOSFETs.

The DC characteristics of MOSFETs are both highly temperature-dependent and geometry-dependent, however as the MOSFETs we are using were commercially available, the geometry is unknown. Hence, we needed detailed knowledge about the temperature dependence to make informed decisions about the creation of any circuitry designed to work at cryogenic temperatures. Due to both the typical size of modern transistors, $< 1\mu\mathrm{m}$, and silicon's poor thermal conductance at low temperatures, self-heating can become an issue, meaning the temperature of the MOSFETs can be much higher than the fridge temperature. Hence, care has to be taken with thermalising the FETs. During this experiment, the FETs were cooled in a TeslatronPT, in which static helium gas is used in the sample space as a thermal exchange mechanism, which increases thermalisation relative to using a dry fridge, in which the sample is sat in vacuum. This is because the whole surface area can now be used for thermal exchange, as opposed to in a dry fridge where the only surfaces available for thermal exchange are the ones directly in contact

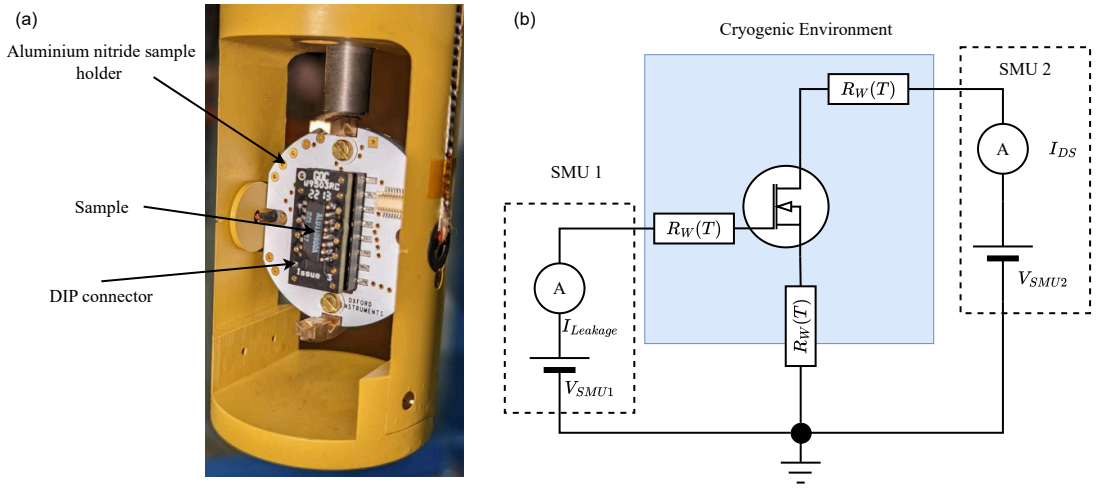

Figure 3.1: (a) IC mounted on a TeslatronPT dip stick: Here the IC is first soldered on to a DIP connector which is then inserted into the mount. The white PCB holder is high thermal conductivity ceramic aluminium-nitride [117] which also helps to improve thermalisation. (b) Electrical set-up for measuring the MOSFETs from 300K-1.5K: Here the wire resistances associated with the Drain and Gate connections of the FET are shown as $R_W(T)$ and are compensated for.

with the PCB. The cooling power was provided by a 1 K helium pot as well as a pulse tube to provide cooling to 4 K. Figure 3.1 illustrates the experimental setup used. The voltages across the FET under test were be calibrated by the resistance of the wiring. This was done because when the resistance of the FET approaches the resistance of the wiring, a non-negligible amount of voltage is dropped across the wiring, especially when the channel resistance is lowest, i.e at high gate voltages. The voltage applied by the SMU unit, V_{SMU}, is equal to the sum of the voltages across the FET V_{DS} and the voltages dropped across the wires, V_W. This can be summarised as,

$$V_{SMU} = V_{DS} + V_W \tag{3.1}$$

and when noting that there will be some current across the FET, I_{DS}, we can say,

$$V_{SMU} = V_{DS} + 2I_{DS}R_W(T), \tag{3.2}$$

	V_{Th} = 0V n-Type		V_{Th} = 0V p-Type		V_{Th} = -0.4V n-Type	
	295K	4.2K	295K	4.2K	295K	4.2K
V_{Th} (mV)	-1	440	5	810	-470	-21
g_m (μS)	32	103	13	27	34	107
SS (mV/dec)	107	20	86	17	99	29
I_{Sat} (mA)	0.47	0.92	0.19	0.33	0.55	1.08

Table 3.1: A comparison of DC characteristics at room temperature and cryogenic temperatures. The transconduance value is taken in the linear ($\mathrm{V_{DS}} = 50\ \mathrm{mV}$) region. All characteristics were taken in the same setup.

where $R_W(T)$ is the resistance associated with the source and drain connections. By measuring the resistance of the wiring at each temperature point the transistor was measured at, Eq. 3.2 was used to determine the actual voltage dropped across the transistor.

The transistors were measured at 30 temperature steps from 1.3 K to 290 K, where the temperature values were on a logarithmic scale. The transistors had both $I_{DS}-V_{GS}$ at a constant V_{DS} and also $I_{DS}-V_{DS}$ at constant V_{GS} at each temperature. In the case of the $I_{DS} - V_{GS}$ plots, two V_{DS} values were used, $50\ mV$ and $1.5\ V$, which were used to place the transistors in both the linear and saturation regions respectively (for the p type the opposite polarity was used). During this operation the V_{GS} was swept from $V_{Th} - 0.5V$ to $V_{Th} + 1.5V$ to capture the full range of gate behaviour. For the $I_{DS} - V_{DS}$ plots, six different V_{GS} values were used, starting from V_{Th} and increasing in 0.3 V intervals. Figure 3.2 shows both the room temperature and 4.2K $I_{DS} - V_{GS}$ characteristics of the -0.4V V_{Th} FET. Figure 3.3 shows a comparison between room temperature and 4.2K for the characteristics $I_{DS} - V_{DS}$. For the most part, the changes seen in the FETs measured here agree well with the literature, even with relatively advanced CMOS nodes [12, 118]. A summary of these characteristics is found in Table 3.1.

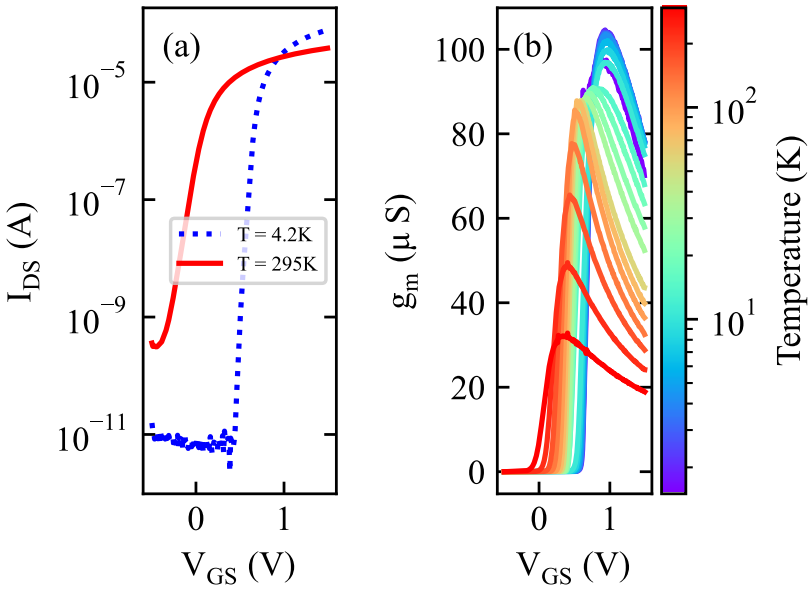

Figure 3.2: $I_{DS} - V_{GS}$ Characteristics of $V_{Th} = 0$V n-type MOSFET. Panel (a) shows the subthreshold region compared for both 4.2K and 295K at $V_{DS} = 1.5V$. This demonstrates a reduction in both the subthreshold swing, as predicted in Eq. 4.12 and the increase in the threshold voltage, shown by the shift of the subthreshold area to a higher V_{GS} at 4.2 K. It also shows the reduction in the off state current, or leakage current. For 295 K the leakage current is 0.5 nA while at 4.2 K this is reduced to 10 pA. Panel (b) demonstrates the increase in transconductance at low temperature, under linear ($V_{DS} = 50$ mV) conditions. Transconductance increases due to the reduction of phonon scattering at lower temperatures.

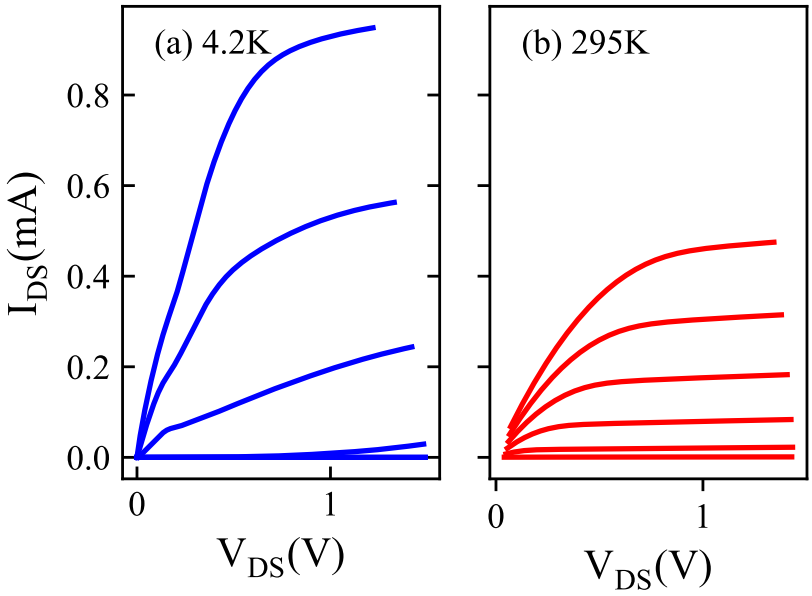

Figure 3.3: $I_{DS} - V_{DS}$ Characteristics of V_{Th} = 0V n-type MOSFET. Here plot (a) is at 4.2 K while plot (b) is at 290 K. The V_{GS} values used are 0 V, 0.3 V, 0.6 V, 0.9 V, 1.2 Vs and 1.5 V. The clearest difference in these plots is the increased drain current, which is another effect which stems from a reduction in phonon scattering. Small kinks are also seen in the low V_{DS} region in (a). These could possibly be coulomb blockade like effects as they only appear at low temperature within these transistors.

3.1.2 Threshold Voltage

Figure 3.4 presents the V_{Th} values of all measured FETs as a function of temperature. The threshold voltages were extracted in both the linear and saturation regimes. In the linear regime ($|V_{DS}| = 50\mathrm{mV}$), the maximum transconductance method [101] was used to determine the threshold. In the saturation region ($|V_{DS}$— = 1.5V), the Extrapolation in the Saturation (ESR) method was applied. For n-type FETs, the V_{Th} initially increases and then stabilises at low temperatures in the linear regime. While factors like impurity freeze-out (other materials present in the silicon that are present due to the manufacturing process) and the expansion of silicon's bandgap also influence V_{Th}, the primary influence is the scaling of the bulk Fermi potential with temperature [77]. As temperatures approach deep cryogenic levels (T <30 K), the threshold voltage measurements begin to diverge, particularly marked by a step change in the saturation region. There are multiple potential explanations for this divergence in V_{Th} at low V_{DS}. Firstly, the increase in channel resistance caused by freeze-out [119] has been observed to elevate the threshold voltage. Furthermore, the freeze-out of dopants modifies the criteria for determining threshold voltage [77]. Consequently, at elevated V_{DS}, where freeze-out is mitigated by substantial electric fields across the channel, the definitions of threshold voltage will vary from those at lower V_{DS}. Hence, beyond freeze-out conditions, different V_{DS} values will yield varying threshold voltages. The lack of saturation for the p-type voltage threshold, as depicted in Figure 3.4 (b), has been documented in prior studies. Nonetheless, the exact physical cause of this phenomenon remains uncertain and has been linked to the temperature-dependent properties of the gate oxide capacitance [77], as well as the pronounced donor freeze-out within the channel [11]. It should also be noted that the threshold voltages for V_{Th} = 0V n-type and p-type FETs significantly rise at low temperatures, making them far less ideal for low-voltage circuits compared to room-temperature conditions. In contrast, the V_{Th} = -0.4V n-type device has a near-zero threshold at low temperatures, making it highly

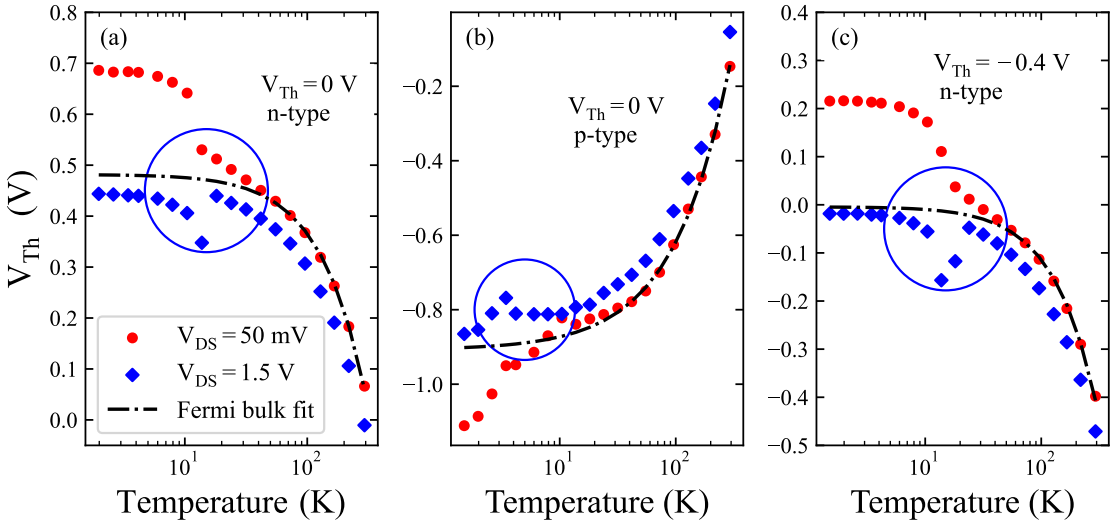

Figure 3.4: Threshold voltage variation with temperature in the saturation (red squares) and linear regions (blue diamonds). In all of these figures the blue circles denote the onset of freezeout in the devices. The Fermi bulk fit is a fitting based upon Eq. 2.22, in the form $y = \phi_T \left(\ln N_A - \ln \Delta - \frac{3}{2} \ln \phi\right) + V_{Th}(T = 0)$ where both N_A and $V_{Th}(T = 0)$ are fit on the V_{DS} = 50 mV data in the range 295 K to 50 K, or prior to freezeout. (a) V_{Th} = 0V n-type FET. (b) V_{Th} = 0V p-type FET. (c) V_{th} = -0.4V n-type FET. The fitting here indicated an acceptor concentration, N_A, of $2.1 \times 10^{21} \pm 5 \times 10^{20}$ m^{-3} and a zero temperature threshold, $V_{Th}(T = 0)$ of -4.8 mV $\pm$ 4.9 mV. The almost zero threshold in this device at low temperatures makes it a good candidate for low supply voltage circuitry at low temperatures.

suitable for low-voltage applications.

3.1.3 Resistors

The resistors used in the amplifiers built in ths chapter were from the TE Connectivity Thin Film SMD Resistor series (these resistors made from various materials dependent on the resistance values, materials such as nickel-chromium and tantalum nitride are used). These were measured to ensure the resistors didn't significantly diverge from their room temperature values. The temperature

was stabilised at every 0.5 K from 2 K to 30 K. Each resistor was measured with a Keithley 2400 multimeter in two terminal resistance measurement mode, which used a current bias and automatic current ranging which to optimise the resistance measurement accuracy. Four terminal connection was not needed as the wiring resistance is on the order of 10Ω and is much smaller than the resistance of the devices. These devices were measured in a custom Oxford Instruments 1 K cryostat. Figure 3.5 demonstrates the low temperature behaviour of these resistors.

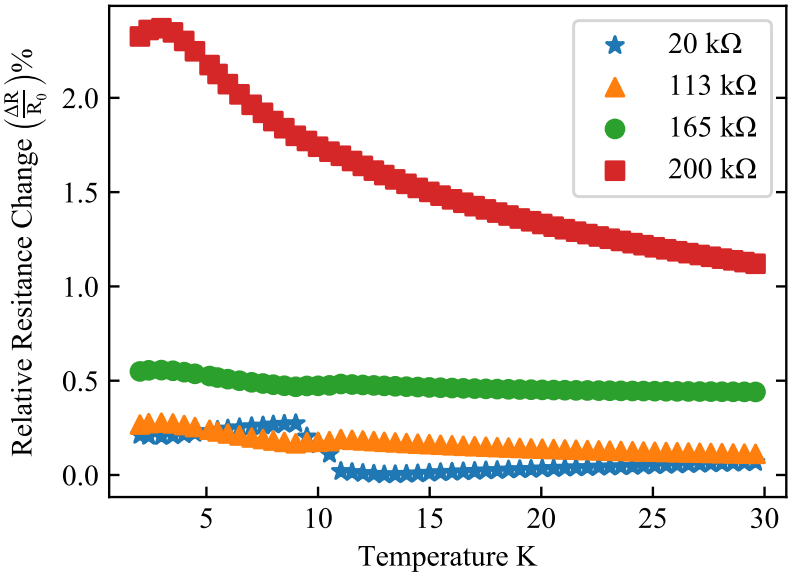

Figure 3.5: Relative resistance change from the 300 K value as a function of temperature: Resistance values do not change significantly from their room temperature values, especially the lower resistance resistors, which differ less than 0.5%. Thin film resistors have low resistance change for several reasons. Firstly materials such as nickel-chromium can be constructed to have a low temperature coefficient of resistance [120]. Secondly the thin nature of the films helps to limit the mean free path of electrons, meaning the mean free path is less temperature dependent.

3.2 Multistage Resistively Loaded Differential Amplifier

This Section describes the first amplifier design and its subsequent measurement and optimisation. Subsection 3.2.1 outlines the motivation for building it and the key characteristics it needs to be useful. Subsection 3.2.2 gives detail of the simulation of the load resistors in the device and its initial optimisation at low temperature. Subsection 3.2.3 demonstrates key amplifier characteristics such as noise, gain and bandwidth as a function of temperature.

3.2.1 Design Considerations

Cryogenic amplifiers are necessary in many readout setups to increase the SNR of measurements at low temperature, so that signals can be measured with precision at high temperatures. The largest market today is for rf amplifiers that take advantage of the efficacy of measurement techniques such as rf reflectometry [121] for reading qubits [122] and other high-frequency physical phenomena [123]. However, less attention is paid to the low frequency regime, DC-10 kHz. One of the uses of amplifiers in this range would be to increase the SNR of transport measurements as a function of temperature. Sensitive transport measurements typically use the four-terminal lock-in measurement technique, which uses a low-frequency current to probe DUT transport properties. If the voltage response could be effectively amplified at low temperature, then this would increase the SNR when readout by the lock-in at room temperature.

The utility of such a cryogenic voltage amplifier is primarily given by four factors:

- Power consumption: The power consumption of the amplifier will determine the location in which it can be placed. Typically, amplifiers sit on the pulse tube plate at approximately 4 K where the cooling power is on the

order of mWs. Therefore it is desirable for the amplifier to have a power consumption of less than 1 mW.

- Gain: The gain of a cryogenic amplifier is crucial for maximising the SNR of an amplified signal at room temperature. This needs to be large enough to boost the signal from low temperature, so its larger than the noise of the room temperature amplifier. A typical minimum gain would be 10 V/V or 20 dB.

- Bandwidth: This will determine the possible frequency operating range for the amplifier, which will change depending on the use case. Our amplifier should be able to amplify signals from DC to 10 kHz.

- Noise: The input noise of the amplifier will determine the size of the signal its possible to measure at low temperature. This should be smaller than the noise of room temperature amplifier $(4\,\mathrm{nV}/\sqrt{\mathrm{Hz}})$ for the amplifier to effectively boost the SNR at room temperature.

We can define some approximate minimum specifications for our amplifier at 4 K in order to assess its utility. These are given in table 3.2. As several amplifier

Power consumption (mW)	Gain (V/V)	Bandwidth (kHz)	Noise $(\mathrm{nV}/\sqrt{\mathrm{Hz}})$
< 1	> 10	$\mathrm{DC} - 10\,\mathrm{kHz}$	< 4

Table 3.2: Minimum specifications for the cryogenic amplifier.

designs will be assessed we can define a Figure Of Merit (FOM), Π, to more effectively compare these designs. This is given as

$$\Pi = \frac{A_v BW}{P} \tag{3.3}$$

where A_v is the DC gain, BW is the bandwidth and P is the power consumption. This will give us an idea of the utility of the amplifier, the product of the DC gain and the bandwidth that is weighted by the power consumption.

As with all cryo-electronics, power consumption is a key parameter of concern, excess power consumption can lead to the heating up of the environment and therefore disrupting the temperature stability of the measurement. The static power consumption $\mathrm{P_{static}}$ of an amplifier is given by,

$$P_{static} = V_{Supply} I_{Supply} \tag{3.4}$$

where V_{Supply} and I_{Supply} are the supply voltages and current respectively. One such way to reduce the power consumption is to use low threshold FETs so to keep the supply voltages of the electronics low. Some examples of the uses of low threshold FETs include bioelectronics [124] and energy harvesting circuits [125]. The reduction in the supply voltage can provide efficiency increases, providing circuit performance is maintained. Hence why low threshold FETs were used and characterised at low temperature prior to the construction of these amplifiers.

3.2.2 Multistage Resistively Loaded Differential Amplifier Design

The initial amplifier topology designed by J.R.Prance was that of a two gain stage, one buffer stage differential amplifier, shown in Figure 3.6. The two gain stages were chosen to boost the gain of the amplifier, while a buffer stage was used to reduce the output impedance and increase the amplifier bandwidth. The amplifier being differential was also important, as a single ended amplifier wouldn't have been useful in amplifying signals from the four terminal measurement technique. The theory behind each of the subcircuits is given in Appendix C.1.

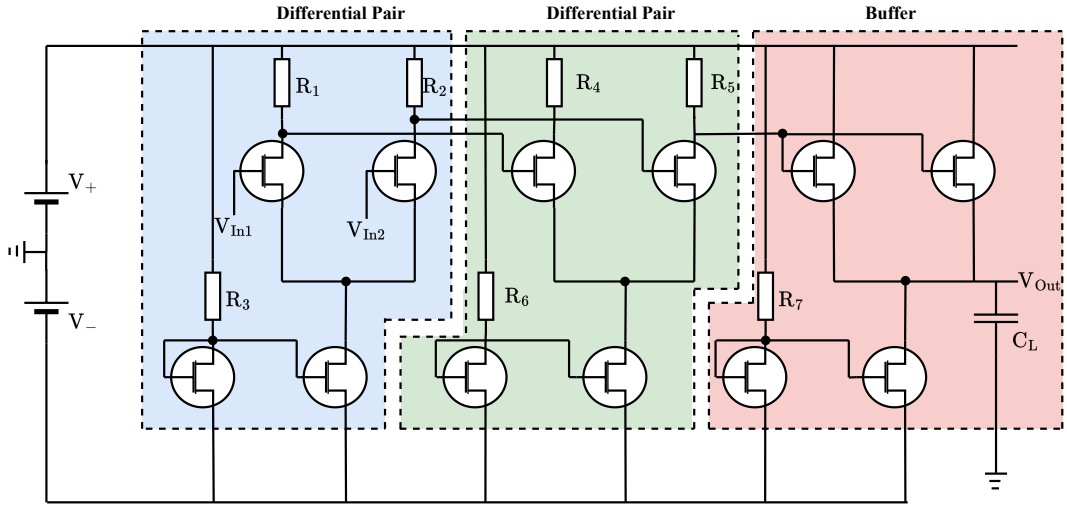

Figure 3.6: Three stage differential voltage amplifier: The gain stages are composed of differential pairs which are loaded by constant current sources. The output buffer is composed of two common drain amplifiers, also with a constant current source. C_L is the load capacitance of the wiring. All the transistors used in this design were the ALD110800 zero threshold n type. This amplifier was built at Lancaster on a PCB from JCL PCB.

3.2.3 Simulation and Testing

To better understand the amplifier, a simulation of the resistor parameter space was undertaken. The simulation was performed in LT SPICE with a Python wrapper developed by J.R.Prance and modified by myself in order to extract data and change the resistance values in the simulation. Of key importance were two parameters, low frequency gain and DC offset. The DC offset is important to retain as large as possible dynamic range. A single differential pair stage, with a constant current source as described previously, was simulated. The whole amplifier was not as this would have made the parameter space too large. We were able to further reduce the parameter space in the simulation by noting the differential pair had to be well balanced, so that $R_1 = R_2$. Figures 3.7 and 3.8 demonstrate the results. These simulations informed us that all three resistors needed to be roughly equal in order to maintain low DC offset values and

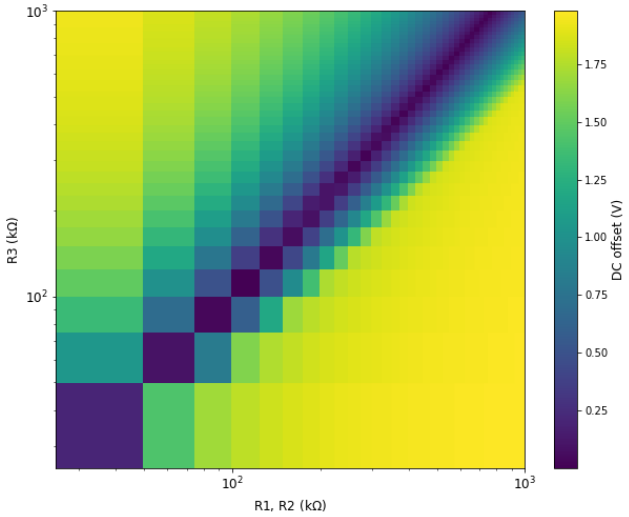

Figure 3.7: LT SPICE simulation of the DC Offset of a single stage differential voltage amplifier: Lower offset values are achieved when all three resistor values are equal to each other.

fair gain values. However, increasing R_3 would increase gain. This knowledge gave us a starting point to testing the devices at cryogenic temperatures. To optimise the resistor values, we could not rely on simulations alone, this is because the level two SPICE models for the FETs and the LT SPICE simulator doesn't adequately represent the physics of cooling to deep cryogenic temperatures [126]. As such, we cooled down an amplifier and instead of placing resistor values we expected, we connected the resistor connections to variable resistors at room temperature. This allowed to vary the resistors and monitor parameters such as gain, DC offset and power consumption. This sped up development time, as we did not have to cycle the cooling of the cryostat (minimum 30 hr turn around time) in order to test different resistor combinations. Figure 3.9 shows the set up for this. Gain characteristics were captured by a Zurich Instruments MFLI. The power supplies in this example two Keithley 2400s and were kept to ± 2 V. Additional capacitance from the resistor cabling made measurements of

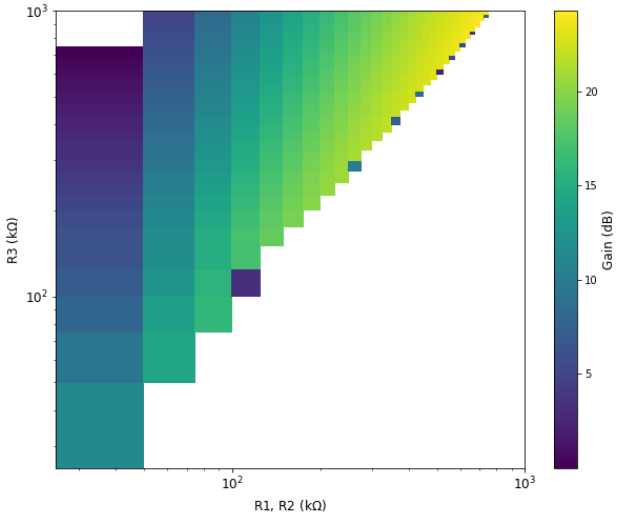

Figure 3.8: LT SPICE simulation of the low frequency gain of a single stage differential voltage amplifier: Here the gain is extracted at 10 Hz. Values less than 0dB are discarded as it fails to amplify.

the amplifiers frequency response inaccurate, as such only the power dissipation, DC gain and DC offset were measured in this analysis. Several iterations of this process were performed, in order to choose resistors for each stage. The final amplifier has resistances $R_3 = 120\ k\Omega$, $R_{1,2,4,5} = 120\ k\Omega$ and $R_7 = 50\ k\Omega$. This gave an amplifier with 30 (V/V) gain, DC offset of approximately zero and power consumption of 2 mW at 1.2 K.

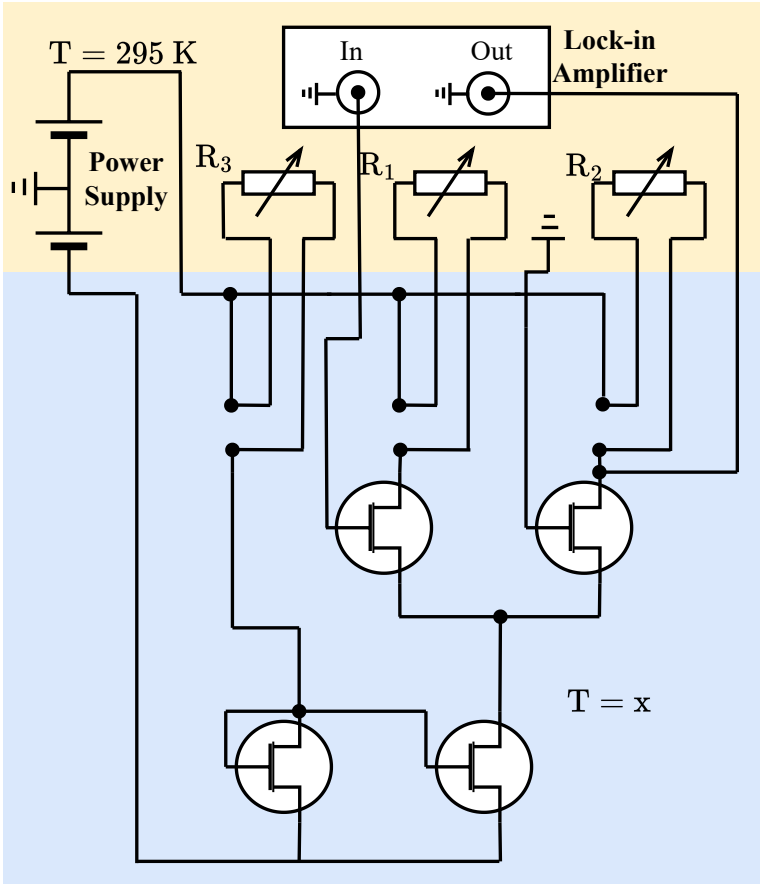

Figure 3.9: Setup for measuring the properties of cryogenic amplifier as a function of resistors different resistor values. T = x denotes the ability to change the temperature of the amplifiers environment.

3.2.4 Temperature Dependence of Multistage Resistively Loaded Differential Amplifier

3.2.4.1 Gain and Bandwidth

After optimising the resistor values for gain and DC offset at low temperature, the amplifier was built (with surface mount resistors from the same series measured previously) and cooled to test its operation as a function of temperature. This was in the range 1.5 K to 30 K where the IO had the best temperature stability. The amplifier had its frequency response taken in this range with a supply voltage of ± 2 V. All the frequency characteristics were captured with a Zurich Instruments MFLI and the power supplied by two Keithley 2400 in four terminal mode. The results of this are shown in Figure 3.10. At 30 K the amplifier performs well, it has a low frequency gain of approximately 70 V/V at a power consumption of 1 mW. The increase in the amplifiers performance can likely be related to the increase in transconductance. However one such notable feature is the kink in the frequency response after approximately 10 kHz at 30 K. This suggests there is a reactive component in the circuit interfering with the output. The ideal output of the amplifier is a low pass filter cut off defined by the output impedance of the amplifier and the load capacitance. We can also see that the performance degrades as the temperature is dropped further, both in terms of gain and frequency response. The degradation in the response could potentially be due to the freezeout effects discussed in Section 3.1.2. This effects key characteristics such as the threshold voltage, this could in turn effect the amplifier operation. It is also possible the material properties of the FETs such as the gate oxide could change as a function of temperature [77], which could explain the reactive effects.

Figures 3.10 (b) to (d) demonstrate the frequency characteristics of the amplifier as a function of the power supply for three key temperatures. The first noteworthy point is that in Figure 3.10 b, the amplifier retains its frequency response charac-

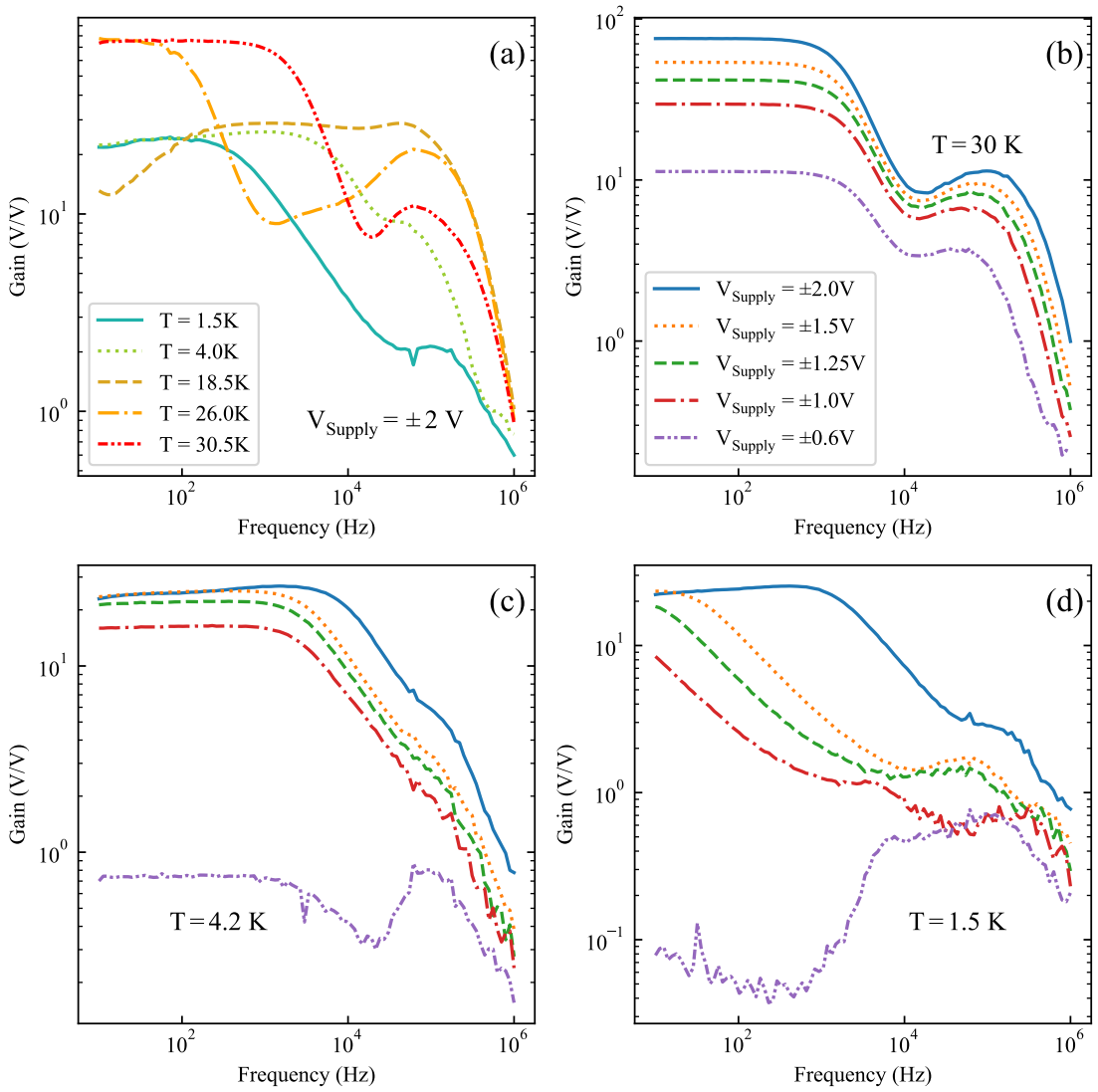

Figure 3.10: (a) Measured differential amplifier performance as a function of temperature for $\pm 2\ V$ supply voltage. (b)-(d) Differential amplifier performance as a function of supply voltage for three temperatures, 1.5 K, 4.2 K and 30 K. Both 1.5 K and 4.2 K are important temperatures as these are the potential temperatures at which the amplifier could be located if it was used to amplify the signal from a sample. At 1.5 K this would be the amplifier sat at the base plate of the IO and at 4.2 K the pulse tube plate. It was also measured at 30 K as this was the optimal temperature of operation in the IO's temperature control range.

teristics, despite the decrease in gain as the amplifier supply voltage is turned down. This is not the case for Figures 3.10 c and d. One explanation could be that the threshold increase shown at the very lowest temperatures means that the transistors exit the saturation regime, and hence the amplifier starts to fail.

3.2.4.2 Input Referred Noise

The noise characteristics of this amplifier were also measured as a function of temperature and supply voltage. The noise was determined by the amplifiers Input Referred Noise (IRN), which is the spectral density of the output in some frequency range of the amplifier, divided by the gain in that frequency range with short inputs. The frequency range the IRN was taken over was 10 Hz to 20 Hz. The noise was taken by a Zurich Instruments MFLI at a sample rate of $f_{clock}/2^{13} = 7.3\ kHz$ (where $\mathrm{f_{clock}} = 60\ \mathrm{MHz}$ is the clock frequency) capturing 2^{13} points and as such had a 0.89 s acquisition time per spectra. A low sampling frequency was chosen to have good frequency resolution at lower frequencies. Figure 3.11 demonstrates the IRN at 1.5 K, 4.2 K and 30 K for a range of different power supply voltages. Firstly, the IRN is high, on the order of $1\ \mu\mathrm{V}/\sqrt{\mathrm{Hz}}$. Typical room temperature voltage amplifiers have noise on the order of nano volts per square root hertz. Figure 3.11 a may however provide some context for poor noise performance. At lower temperatures, the gain in the amplifier is suppressed, which may mean the amplifiers noise is gain limited in this instance. The fact that at 30 K the noise is lower, and decreases for increasing power consumption (which increases gain) also suggests this. As such higher gain topologies may reduce this noise. However, the presence of strong 1/f noise could well be a limiting factor.

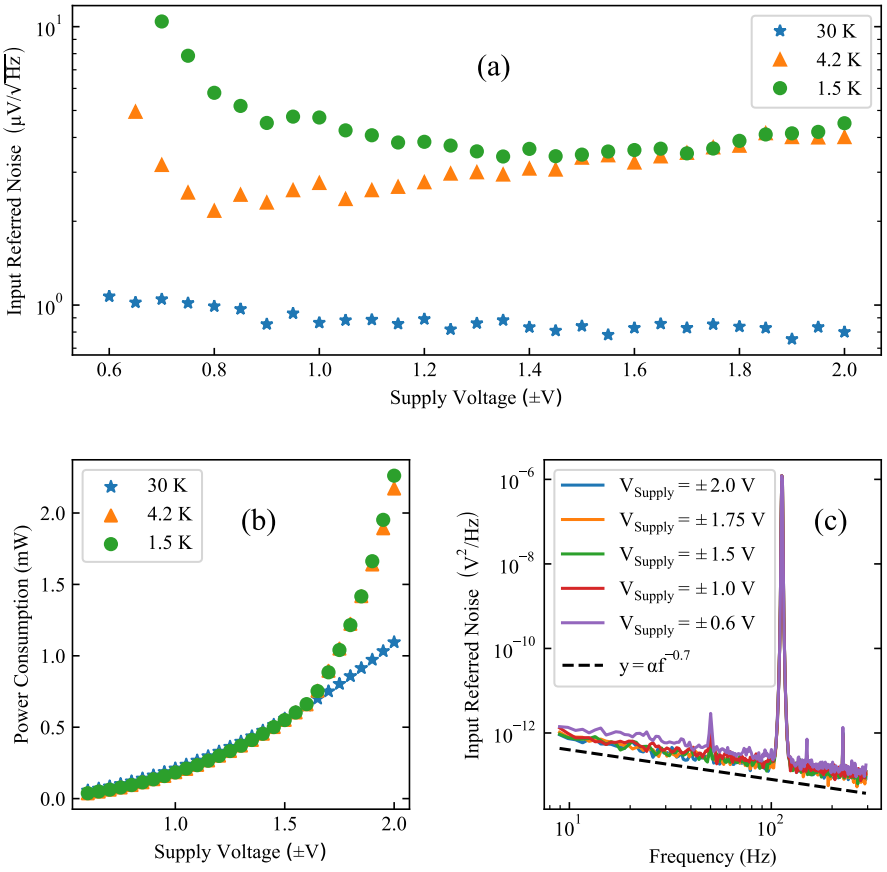

Figure 3.11: (a) IRN as a function of temperature and power supply. Lower IRN at higher temperatures suggests that at lower temperatures it is gain limited, as at higher temperatures, higher gain is achieved for the same operating supplies. (b) Power consumption as a function of supply voltage and temperature. The changing of the power consumption dependence of both 1.5 K and 4.2 K just after 1.5 V suggests the amplifier is working in a fundamentally different manner. One explanation is the local heating in the environment is causing the threshold voltage to shift, which changes the DC operating conditions of the amplifier. This change may not happen at 30 K as the device is likely better thermalised due to improved thermal conductance of of silicon at this temperature. (c) $1/f^x$ noise ($x = 0.7$) in the amplifier, can also be found in the literature in MOSFETs at low temperature [127].

3.3 Single Stage Actively Loaded Differential Amplifier

This Section illustrates the design and testing of the second amplifier design. In Subsection 3.3.1 the motivation behind the second amplifier design is outlined. Subsection 3.3.2 gives key amplifier details as a function of temperature.

3.3.1 Design Considerations

When measuring the previous design it was also noticed that relatively large voltage supplies were still having to be used to keep high gain. This is to the drain-resistor problem [128] and further made worse by the increase in threshold voltage at low temperatures. From Appendix C.1.0.1 the small signal gain, A_V of the differential pair is given by,

$$A_V = g_m R_D \tag{3.5}$$

where g_m is the transconductance of the transistor and R_D is the resistance value of the resistor at its drain. Increasing this resistor value therefore increases the gain of the amplifier. The trade of however is that by increasing this drain resistance, you also drop a large fraction of the supply voltage across this resistor. This means that the voltage at the drain of the FET reduces. If this reduces too much it can violate the saturation condition which is critical for amplifier operation,

$$V_{DS} > V_{GS} - V_{Th}. \tag{3.6}$$

One such way to counter this is to increase the supply voltages, but this will increase power consumption. The updated design is based upon the an active current mirror design, which was inspired by Advanced Linear Devices whitepaper [129]. This is a p-type current source replacing the load resistors in the differential pair and is shown in Figure 3.12. The active load helps to solve the drain resistor problem as the current source has a high small signal resistance, and so high gain,

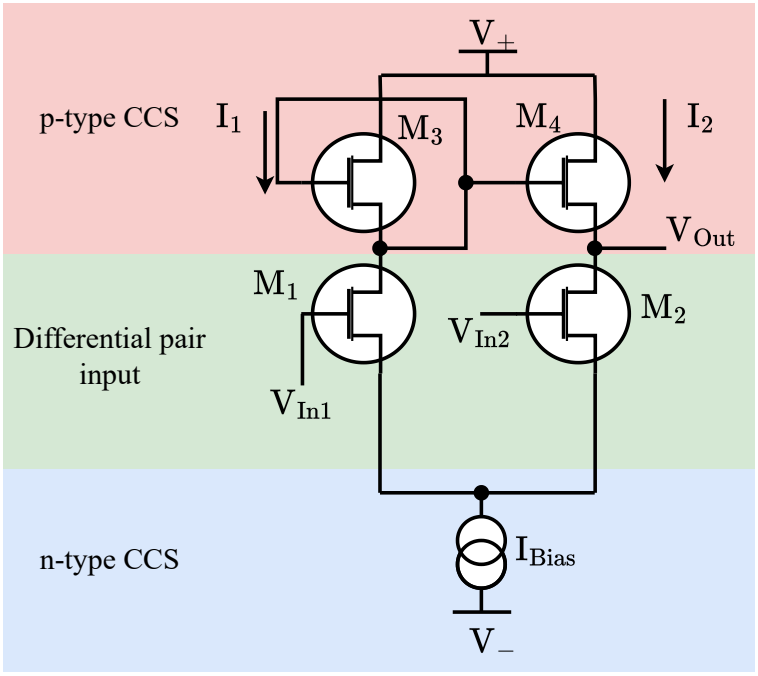

Figure 3.12: Single stage actively loaded differential amplifier: Here CCS is the constant current source described in Appendix C.1.0.2, the current it provides will be set by a resistor R_1 not seen in this plot. This amplifier has a single ended output and doesn't need to be read out in a differential manner. The p type transistors used in the p type constant current source (M_3 and M_4) are the ALDALD310700 zero threshold devices while the rest of the transistors are n type are the same ALD110800 zero threshold devices used in the previous design. The different colours denote the distinct stages of the amplifier.

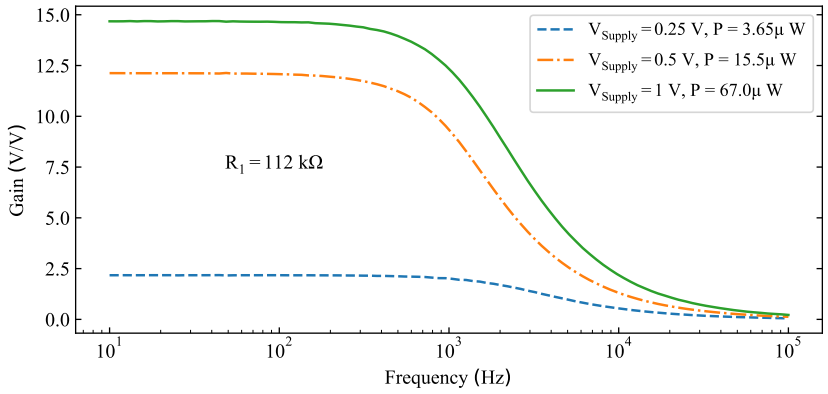

Figure 3.13: Room temperature operation of the actively loaded differential pair: The resistor value R_1 denotes the value of the bias resistor of the n-type CCS. The amplifier provides high gain still at $\pm 0.5\ V$ supplies and still has gain at $\pm 0.25\ V$.

but the biasing of the drain of M_4 is not set by a resistor. Instead its set by the V_{GS} of transistor M_3, which is in turn set by I_{Bias}. This bias current should be large enough to keep M_3 in saturation. An appropriately sized bias current can be supplied even with low supply voltages as we can change the bias resistor (Appendix C.1.0.2 gives more detail on this). As such, we can retain high gain, at lower supply voltages. Another advantage of this design is its single ended conversion, which helps preserve the gain. In Figure 3.6 we see that in the second differential pair, the gain is only read out of one of the transistor drains, and isn't read out differentially. This effectively halves the gain of the amplifier. This is in contrast to the updated circuit which automatically converts the gain into a single ended output at the drain of M_4. An example of its room temperature operation is given in Figure 3.13.

3.3.2 Temperature Dependence of Amplifier characteristics

Further *in situ* testing of the resistor was performed in a similar manner to Fig. 3.9, except there was now only one resistor to vary, which was the bias resistor in the constant current source. It was found that the best balance between DC gain and power consumption was at $R_1 = 100\ k\Omega$, with DC gain of 3 and power consumption of 4μW at a $\pm 1V$ supply. This amplifier was then built and cooled from room temperature to 4 K at a constant supply voltage of $\pm 1\ V$. The results are shown in Figure 3.14. The amplifier performance increases as temperature decreases until around 70 K. The DC gain increases, power decreases, and bandwidth is largely constant. The DC gain increase is due to the transconductance increase in the FETs. The decrease in power can be attributed to the throttling of the bias current as the threshold voltage shifts upward (as $I_{DS} \propto (V_{GS} - V_{Th})^2$ in the saturation region and the constant current) as a constant voltage is supplied. Despite the reduction in bias current, the FETs are still likely to be in saturation mode, so the amplifier continues to operate. After 70 K performance drops off slightly with the DC gain decreasing. Around 30 K the performance collapses. This is very similar to the previous amplifier, the frequency characteristics start to deviate from the expected low-pass like shape and the DC gain decreases rapidly. As such the decrease in performance can be attributed to the same factors, freezeout related phenomena such as the kink effect and threshold voltage increase. The IRN was also measured for this amplifier in the same manner as the previous, shown in Fig. 3.15. It also had a similar noise level to the previous amplifier which was on the order of $1\mu V/\sqrt{(}Hz)$.

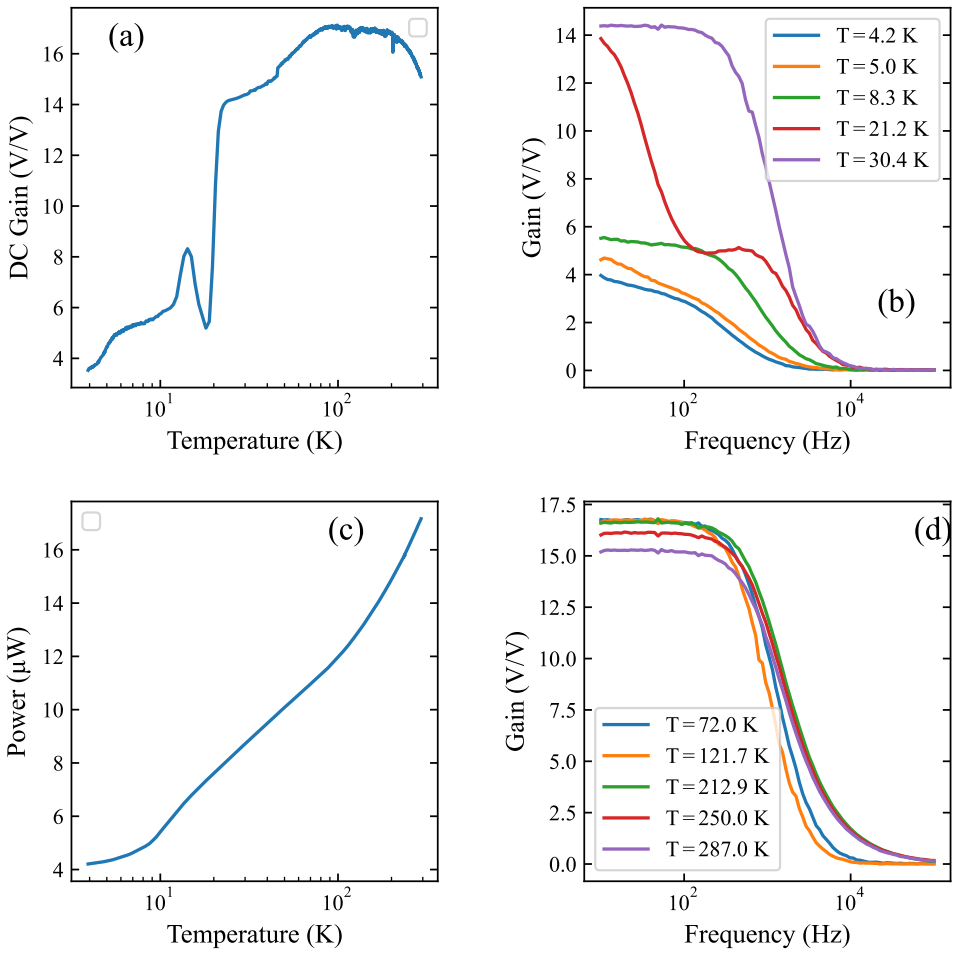

Figure 3.14: (a) DC gain as a function of temperature. (b) Frequency response at temperatures lower than 30 K. After 30 K the amplifiers performance drastically decreases as similar to the previous amplifier. Also of note that performance decreases sharply again after 5 K. This wasn't expected as after the dopant freezeout it was thought that the amplifier would be in a steady state. (c) Power consumption as a function of temperature. Power consumption consistently decreases likely due to the shifting of the threshold voltage of the FETs. (d) Frequency response at temperatures higher than 72 K. This illustrates the initial increase in performance as the amplifier is cooled.

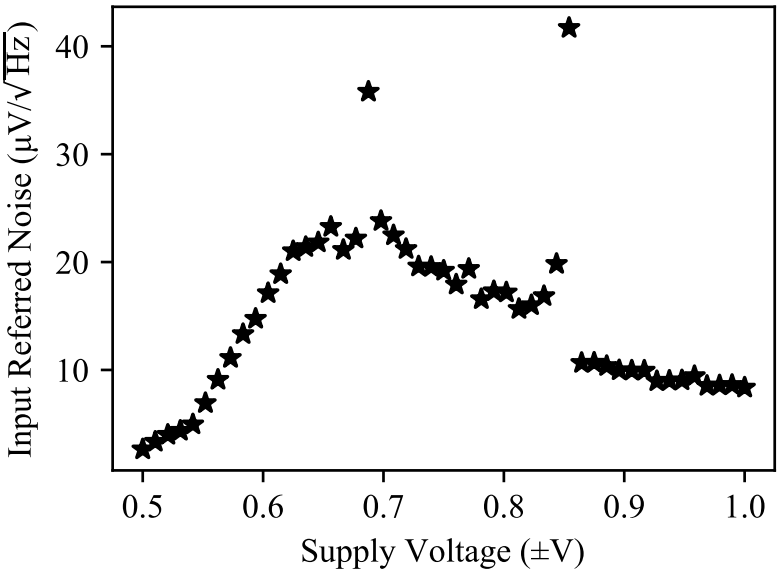

Figure 3.15: Input referred noise of the current mirror amplifier at 4.2 K in the 10 Hz-15 Hz region as a function of supply voltage. While the reduction of input referred noise is expected at higher supply voltages due to the increasing gain of the amplifier, the reduction at low supplies in this plot is unexplained. The spikes in the IRN are likely measurement artifacts.

3.4 Summary of Amplifier Study

In the preceding sections, two different amplifier topologies were tested at cryogenic temperatures. The first, a three stage amplifier, with two passively loaded differential pairs and a buffer output, and the second a single stage actively loaded differential pair. Their specifications at 4.2 K are assessed against the specifications in Table 3.2, in Table 3.4 and Table 3.3. Neither amplifier meets

Specification	Value	Meets Spec?	Comments
Power (mW)	2	No	Excessive for 4 K plate.
DC gain (V/V)	23	Yes	-
Bandwidth (kHz)	15.2	Yes	Buffer lowers output Z.
Noise (μV/$\sqrt{\text{Hz}}$) (10-20Hz)	1	No	$1/\text{f}^{\text{x}}$ noise dominates at low f.
$\Pi(4\ K)$ ($\frac{\text{kHz}}{\mu\text{W}}$)	0.16	NA	NA
$\Pi(30\ K)$ ($\frac{\text{kHz}}{\mu\text{W}}$)	0.1	NA	NA

Table 3.3: Specification results for the first amplifier design at 4 K.

Specification	Value	Meets Spec?	Comments
Power (mW)	4×10^{-3}	Yes	Very low power
DC gain (V/V)	3.7	No	Acceptable at 30 K, not 4.2 K
Bandwidth (kHz)	0.112	No	Needs additional buffer.
Noise (μV/$\sqrt{\text{Hz}}$) (10-20Hz)	8.4	No	$1/\text{f}^{\text{x}}$ noise
$\Pi(4\ K)$ ($\frac{\text{kHz}}{\mu\text{W}}$)	0.7	NA	NA
$\Pi(30\ K)$ ($\frac{\text{kHz}}{\mu\text{W}}$)	2.6	NA	NA

Table 3.4: Specification results for the second amplifier design at 4 K.

the minimum specifications set out in Table 3.2. Performance severely decreases in both amplifiers after 30 K likely due a combination of threshold increase and freezeout related effects. Both amplifiers also show elevated noise characteristics

with 1/f noise being the likely reason for high low frequency noise. The single stage active loaded amplifier has a better Π at both 4.2 K and 30 K, due to its reduced power consumption. This suggests that this topology is preferable to the passively loaded differential amplifier combination.

3.5 Conclusion

In conclusion, we characterised three low threshold transistors for cryogenic temperatures and extracted key parameters as a function of temperature. All of these transistors showed evidence of freezeout below 30 K. These transistors were used to create two DC-coupled differential voltage amplifiers, optimized by *in-situ* testing of load resistors. The amplifiers were tested at low temperature for noise, bandwidth, gain, and power. Both amplifiers showed improved performance down to 30 K, after which freezeout in the transistors likely caused disruptions. They both also demonstrated 1/f noise at low frequencies. The second amplifier, with an active current mirror, performed slightly better, as it allowed for lower supply voltages and therefore power consumption. The single ended conversion of this design also helped maintain high gain. Neither amplifier met the initial specifications for operation at cryogenic temperatures. This study suggests a transistor-first approach for cryogenic electronics, involving the mass testing of different types of transistor. Specifically, transistors that are from more modern nodes, 160 nm or smaller, would significantly reduce the risk of freezeout behaviour being present. One such technolgy is the TSMC 28 nm HPL (High Performance Low power), which has been shown to work reliably down to 4 K in complex electronics, such as FPGAs [130]. However, it is likely that it will take some time for cutting edge nodes such as this to become more widely commercially available. This would enable the identification of commercially available transistors which are more resistant to freezeout effects, and as such the resulting electronics would both perform better at low temperatures and have

more predictable behaviour. The most promising commercially available technology SiGe transistors, which have been proven to work at cryogenic temperatures [131], especially for the readout of SQUID based detectors [132]. These are preferable to HEMTs in the medium-frequency (as targeted in this study) regime as they have reduced 1/f noise. For more ready made solutions it should also be noted that devices such as the Texas Instruments LMH6629 is a SiGe based ultra low noise operational amplifier that would be worth testing at cryogenic temperatures.

Chapter 4

Cryogenic Threshold Engineering

This Chapter builds on the previous work characterizing three types of FETs by exploring the concept of cryogenic threshold engineering. In earlier studies, it was observed that the depletion mode FET, which has a room temperature threshold voltage of approximately -0.45 V, exhibited a threshold voltage near zero at low temperatures (below 30 K). This observation led to the idea of cryogenic threshold engineering—minimizing the threshold voltage of bulk FETs at low temperatures by initially having negative thresholds at room temperature. Such optimization could enhance the efficiency of devices utilizing these bulk FETs under cryogenic conditions.

Section 4.1 introduces the concept of cryogenic threshold engineering and an analytical framework is presented to explain how an amplifier's performance might improve as the threshold voltage approaches zero. This is supported by an analytical expression for the Figure of Merit FOM discussed in Chapter 3. Section 4.2 validates the analytical model through simulations conducted in LT SPICE. In Section 4.3, experimental measurements of the amplifier are presented to demonstrate the practical impact of this technique. Finally, Section 4.4 concludes the Chapter with a discussion on the broader implications and potential applications of cryogenic threshold engineering.

4.1 Introducing Cryogenic Threshold Engineering

As covered in Chapter 3 bulk FETs suffer from an increase in threshold voltage at cryogenic temperatures, which increases the supply voltage at which any circuitry made of these FETs can be operated. As we saw in the previous Chapter, threshold voltages can increase on the order of 100s of millivolts (Figure 3.4), this is also seen in modern native (room temperature threshold approximately zero) transistors [118]. The knock-on effect is that this threshold increase has to be compensated by increasing the supply voltage, increasing the power dissipation in the electronics. In cryogenic environments, this can have many detrimental effects, such as overheating the local environment and disruption of the temperature stability of the cryostat. One of the most promising technologies for low voltage circuitry is the Fully Depleted Silicon-On-Insulator (FD-SOI) technology, which can be back-gated at low temperature to adjust the threshold in order to compensate for threshold increases [13, 80, 133]. Theoretical work has shown that threshold engineering reduces the power consumption of simulated FD-SOI low-noise amplifiers (LNA) for quantum computing applications [134]. Recent practical work has also shown threshold engineering that improves efficiency metrics in ring oscillators [135]. However, the drawbacks of this approach include induced telegraphic noise [136] and that it can require large back-gate voltages, outside circuit operating voltages, to adequately shift the threshold [137]. An alternate approach to back biasing is using depletion mode FETs with an appropriate room temperature threshold voltage less than zero. This leverges the decrease in temperature to "cryogenically engineer" the threshold towards zero, hence cryogenic threshold engineering. This has been demonstrated at 77 K to reduce the supply voltage and increase the frequency of ring oscillators (which are common electrical circuits used for generating a voltage at specific frequency, usually used to create the clock frequency for an IC) [138]. In this work, we further demonstrate the utility of this technique by demonstrating its effect on a typical cryogenic use case, an amplifier.

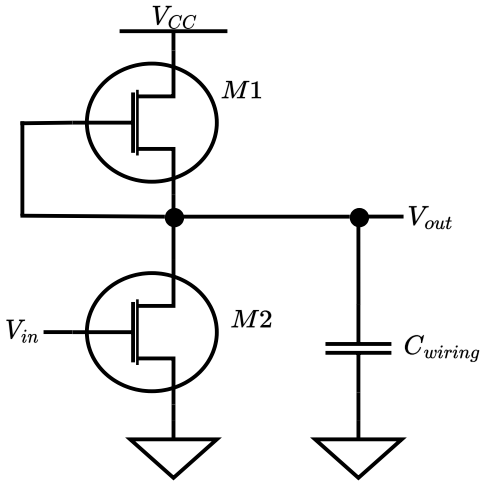

Figure 4.1: Common source amplifier: M1 and M2 are low threshold n-type FETs. V_{CC} is the power supply voltage to the amplifier. C_{wiring} is the capacitance from the cryostat wiring, which dominates over the internal capacitances of the FETs.

A common source amplifier, Fig. (4.1), was used to quantitatively determine the effect of threshold engineering on a common cryo application, namely amplification. The simplicity of the common source amplifier allows for analytical attribution to any increases in utility/efficiency to the threshold of the FETs that make up the amplifier. In the case of a differential amplifier such as an LNA (low-noise amplifier), the parameter space would be much larger, and it would be much more difficult to identify the dependence of the efficiency on the threshold voltage. To quantify the improvements, we first need to define a Figure of Merit FOM, Π, the same as Chapter 3. This is given as the ratio of the gain-bandwidth product (GBWP) to the power consumption of the amplifier. First, we consider the Hybrid-Pi model [139] for the DC gain of the amplifier. This is given by

$$|A_v| = \frac{v_{out}}{v_{in}} = \frac{g_m R_D}{1 + g_m R_S} \tag{4.1}$$

where $|\mathrm{A_v}|$ is the small signal gain, $\mathrm{g_m}$ is the transconductance of the FET, $\mathrm{R_D}$ is the drain resistance of M2 (the resistance of M1) and $\mathrm{R_S}$ is the source resistance (or output resistance at M2). As the source resistance in our case is the wiring

resistance of the refrigerator, which is approximately $10\ \Omega$, is small compared to the load resistance (the resistance of the channel at $V_{GS} = 0$ is approximately $5\ \mathrm{k}\Omega$ as per the datasheet [129]), we can simplify this expression to

$$|A_v| = \frac{v_{out}}{v_{in}} = g_m R_D. \tag{4.2}$$

Next, we have to consider that the amplifier sits at the bottom of a cryostat with 1-2m of wiring. In the case of our fridge, the wiring we use has a capacitance of approximately 70pF/m to ground (Brass twisted pairs with a copper nickle shielding) giving a total capacitance of 140pF at the output of the amplifier. If we compare this value to the internal capacitances of the FET in the datasheet, the wiring capacitance dominates. As such, we can say that the wiring capacitance, ($\mathrm{C_{wiring}}$), forms an RC low pass filter with the output resistance of FET M1 ($\mathrm{R_1}$). Putting all this together, we can give an expression for Π,

$$\Pi = (g_m R_1) \left(\frac{1}{2\pi R_1 C_{wiring}} \right) \left(\frac{1}{V_{CC} I_{CC}} \right), \tag{4.3}$$

where $\mathrm{V_{CC}I_{CC}}$ represents the product of the amplifier supply voltage and current, and is the power consumption of the amplifier. Simplifying this gives

$$\Pi = \left(\frac{g_m}{2\pi C_{wiring}} \right) \left(\frac{1}{V_{CC} I_{CC}} \right) \tag{4.4}$$

where $\mathrm{g_m}$ is the transconductance of transistor M2. Unpacking further, to see the dependence of Π on $\mathrm{V_{Th}}$, $\mathrm{g_m}$ can be replaced by one of the universal FET equations for a subthreshold or saturation mode of operation. The conditions for a FET in saturation mode are

$$\mathrm{V_{GS}} > \mathrm{V_{Th}} \tag{4.5}$$

and

$$\mathrm{V_{DS}} \geq \mathrm{V_{GS}} - \mathrm{V_{Th}}. \tag{4.6}$$

These conditions will always be met in the circuit in Fig. 4.1 as long as $\mathrm{V_{CC}}/2 \geq \mathrm{V_{GS}} - \mathrm{V_{Th}}$ and the $\mathrm{V_{Th}}$ doesn't exceed 0 V as each FET has $\mathrm{V_{GS}} = 0$. The primary reason for having FET M1 instead of a resistor is that having $\mathrm{V_{GS}} = 0$ means

that the effective resistance of each FET is equal. This means that the voltage is equally dropped across both FETs, even as the temperature drops and the threshold changes. It also means that the biasing conditions will remain the same for both FETs, as they are both nominally identical and have the same current and therefore power dissipated within them. The drain current, $\mathrm{I_{DS}}$,is given by,

$$I_{DS} = \kappa V_{\mathrm{ov}}^2 \tag{4.7}$$

where $\mathrm{V_{ov}}$ is the overdrive voltage and $\kappa = \frac{\mu \mathrm{C_{ox}}}{2} \frac{\mathrm{W}}{\mathrm{L}} (1 + \lambda V_{DS})$, where $\mathrm{C_{ox}}$ is the gate oxide capacitance, μ is the carrier mobility, $\frac{\mathrm{W}}{\mathrm{L}}$ is the ratio of the channel width to length of the channel, λ is the channel length modulation parameter and V_{DS} is the drain-source potential. Taking the derivative of $\mathrm{I_{DS}}$ with respect to $\mathrm{V_{GS}}$ we arrive at

$$\frac{\partial I_{DS}}{\partial V_{GS}} = g_m = \frac{2 I_{DS}}{V_{ov}} \tag{4.8}$$

as such, as $\mathrm{I_{DS}} = \mathrm{I_{CC}}$, we arrive at

$$\Pi = \frac{1}{\pi C_{\mathrm{wiring}} V_{CC} V_{ov}}, \tag{4.9}$$

for the FETs in saturation mode where $\mathrm{V_{CC}}$ is the supply voltage. In thisFOM the current factors, which are temperature dependent, cancel so that the only temperature dependent factor is $\mathrm{V_{ov}} = \mathrm{V_{GS}} - \mathrm{V_{Th}(T)}$ where $\mathrm{V_{GS}}$ = 0 V for both FETs in this circuit. As such, the FOM becomes

$$|\Pi| = \frac{1}{\pi C_{\mathrm{wiring}} V_{CC} V_{Th}(T)}. \tag{4.10}$$

Therefore the only temperature dependent factor is $\mathrm{V_{Th}}$. This allows us to identify any increases in efficiency due only to V_{Th}, rather than increases in transconductance due to temperature related changes in phonon scattering. This process can be repeated for the subthreshold regime of transistor operation. The condition for subthreshold operation is

$$V_{GS} \leq V_{Th}. \tag{4.11}$$

The corresponding universal FET equation is

$$I_{DS} \approx I_{D0} \exp\left(\frac{V_{\mathrm{ov}}}{nV_T}\right) \tag{4.12}$$

where V_T is the thermal voltage given by $\mathrm{k_B T/q}$ and n is a factor given by the internal FET capactiances. Taking the derivative of Eq.4.12 with respect to $\mathrm{V_{GS}}$ and dividing the result by the same expression, we arrive at the following

$$\left(\frac{\partial I_{\mathrm{DS}}}{\partial V_{\mathrm{GS}}}\right)\frac{1}{I_{\mathrm{DS}}} = \frac{g_m}{I_{\mathrm{DS}}} = \frac{1}{nV_T} \tag{4.13}$$

Subbing this expression into Eq 4.4 we arrive at the expression for the common source amplifier when the FETs are in the subthreshold regime

$$|\Pi_{Sub}| = \frac{1}{2\pi C_{\mathrm{wiring}} V_{\mathrm{CC}} n V_{\mathrm{T}}}. \tag{4.14}$$

4.2 Simulation

The expressions generated analytically can now be tested via simulation. The method chosen for the simulation of these amplifiers was LT SPICE, as Advanced Linear Devices offers models of each of its transistors for LT SPICE simulation. In order to interact with LT SPICE and run large parameter runs, as well as to collect the data from each of these runs, a Python script, created by Jonathan Prance and edited by myself, was used. The amplifier was simulated for its frequency response in the range of 10 Hz-1 MHz and $\mathrm{V_{CC}}$ stepped from from 0.1 V to 2 V in 10 mV steps. This was repeated for $\mathrm{V_{Th}}$ in the range from -0.45 V to 0 V in 10 mV steps. This whole process was repeated to capture the power consumption at each supply voltage/threshold voltage step. The FOM was then determined via the product of the low frequency gain and the bandwidth, divided by the power consumption. The low frequency gain was determined by the average gain in the 10 Hz-100 Hz range. The bandwidth was determined by the frequency at which the response is -3 dB from the DC gain value. Power consumption is a product of supply voltage and supply current. Any frequency responses with

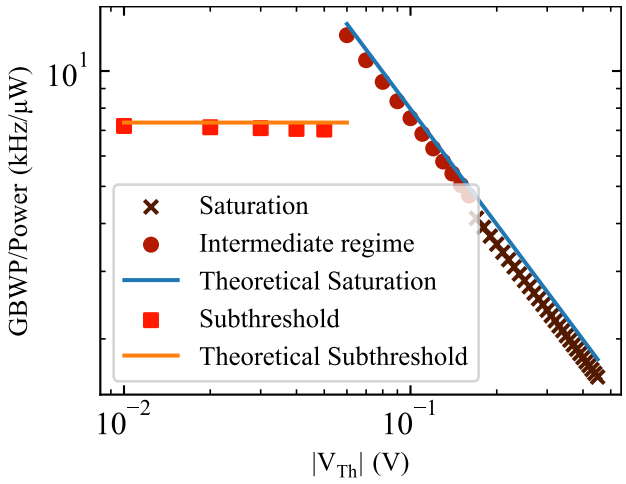

Figure 4.2: FOM plotted a function of $|V_{Th}|$ at a constant $V_{CC} = 2$ V : V_{Th} was varied from -0.45 V to 0 V. Saturation and intermediate regime data points agree well the theoretical line predicted by Eq. 4.9.

DC gain less than unity were removed as this meant that the amplifier was not functioning. As the models used by Advanced Linear Devices are level 2 PSPICE nmos models, there is an option to vary the temperature in LT SPICE. This was not used because these models did not capture all of the effects on the threshold at cryogenic temperatures.

Fig. 4.2 confirms that both Equations 4.14 and 4.10 agree with the simulation results. The simulated wiring capacitance in this case was $200\,\mathrm{pF}$. For the subthreshold regime, the oxide capacitance factor n in Eq. 4.12, was extracted from another simulation of the FET and was found to be 0.45. This was performed by performing simulations of the FETs in the saturation regime and using Eq. 4.7 as we know the width, length and mobility from the LT SPICE model. It also shows that in the subthreshold regime, the FOM does not depend on V_{Th} according to Eq. 4.14. This figure also demonstrates that while in saturation regime, decreasing the threshold will increase the FOM. The intermediate regime points do not explicitly model the 'medium inversion' regime, but rather will be a numerical model that bridges the gap in the drain current between the

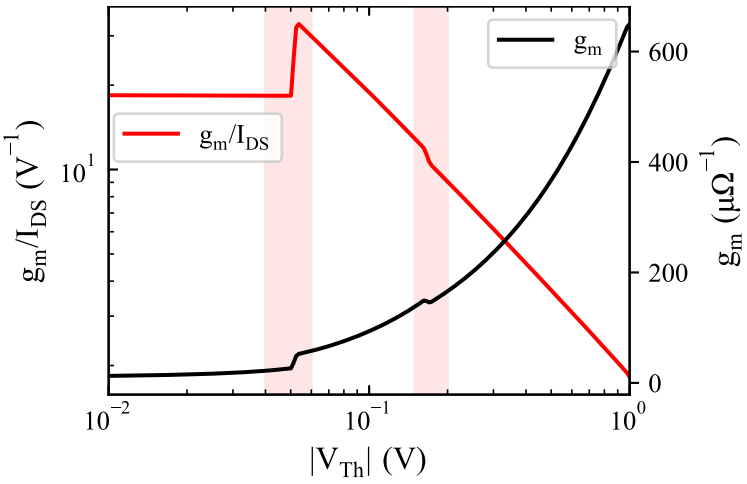

Figure 4.3: Simulation of the transconductance as a function of $|\mathrm{V_{Th}}|$ for a FET with $\mathrm{V_{GS}} = 0\mathrm{V}$: The black line demonstrates that the plot of $\mathrm{g_m}$ has kinks in at the transitions inbetween saturation, intermediate and subthreshold regimes. These voltages are the same as the kinks in Fig. 4.9. The red line, the quantity $\mathrm{g_m/I_{DS}}$ determines the functional dependence the FOM has upon $|V_{Th}|$ as per Eq. 4.4 and hence is proportional to the data in Fig. 4.9. This demonstrates clearly how the FOM would be effected by these kinks. The transparent red bars demonstrates that kinks happen at the same voltages.

saturation regime ($\mathrm{V_{GS}} > \mathrm{V_{Th}}$) and the subthreshold regime ($\mathrm{V_{GS}} \leq \mathrm{V_{Th}}$). This is demonstrated in Fig. 4.3, the intermediate regime has been named this because this is between the subthreshold and saturation regime. This is likely a mathematical patch between the two well defined models. Fig. 4.4 shows the FOM as a function of the supply voltage. This Figure also agrees with Eq. 4.9 as the FOM is inversely proportional to the supply voltage. This plot also serves to demonstrate that as $\mathrm{V_{Th}}$ is lowered, the amplifier can be used at lower supply voltages without failure. In addition to this, when the amplifier operates here, it has a much higher FOM. Even at high supply voltages, the FOM is much higher for lower $\mathrm{V_{Th}}$. The explanation for this can be found in Fig. 4.2, where in the saturation regime the lower the $\mathrm{V_{Th}}$, the higher the FOM. It should be noted here that the FOM improves by a factor of 8 for the highest supply voltage when $\mathrm{V_{Th}}$

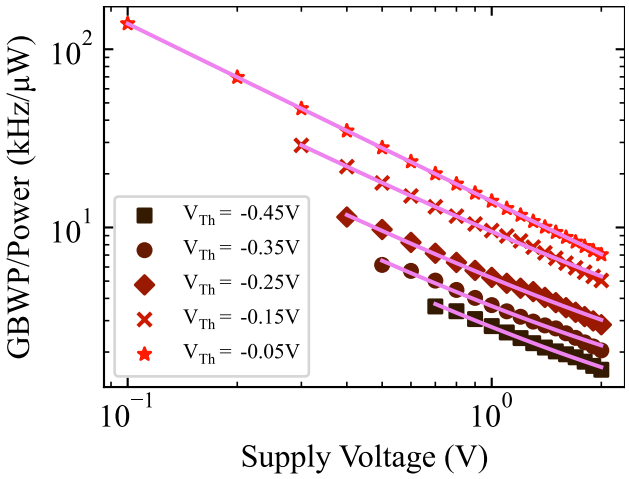

Figure 4.4: FOM as a function of supply voltages for different V_{Th}: The fitted lines are fit with an inverse supply voltage function.

goes from -0.45 V to 0V.

4.3 Measurement

Following simulation, the amplifier in Fig. 4.1 was built and cooled by myself. To show the cryogenic threshold engineering technique, both M1 and M2 are ALD114904. These FETs were chosen because in Fig.3.4 the V_{Th} moves from 0.45 V to 0 V at 1.5 K, as such it represents the simulation well and its threshold is minimised at low temperature. As such, we expect an increase in the FOM of approximately 8.

The amplifier had a 1 V supply voltage (designed to keep the FETs in saturation) supplied by a Kiethley 2450 SMU and its frequency response was taken by a Zurich Instruments MFLI lock-in amplifier. The amplifier was cooled in an Oxford instruments 'OI' cryostat from 295 K to 1.5 K and had continuously had its frequency response taken from 10 Hz to 100 kHz. The results of this cooldown are shown in Fig. 4.5.

The only temperature-dependent factor in the FOM is V_{Th} as per Eq. 4.9. Therefore, as V_{Th} goes towards 0 V upon cooling, the FOM will increase. This is demonstrated in Fig. 4.5, showing that from room temperature to cryogenic temperatures, the FOM improves by a factor of 8.5 (the ratio of the FOM at room temperature to the maximum FOM at low temperature), close to the simulated 8. It also shows agreement with Eq. 4.10 within the uncertainties until freeze-out occurs at approximately 35 K. The large dip in the FOM in Fig. 4.5 at this temperature is likely caused by the impact ionisation, which itself is both temperature and gate voltage dependent. In Fig. 4.6 the line at 34K is below the room temperature value due to the onset of impact of ionisation around this temperature in the common source amplifier. More measurements are needed to obtain a greater resolution of the impact of freeze-out here.

Another area which needs further investigation is why the FOM dips again after dipping initially at 35 K. It would be expected that after freezeout has been completed, the amplifier FOM would plateau, because the number of acceptors/donors has become fixed again. However, this isn't the case and the amplifier FOM still continues to dip.

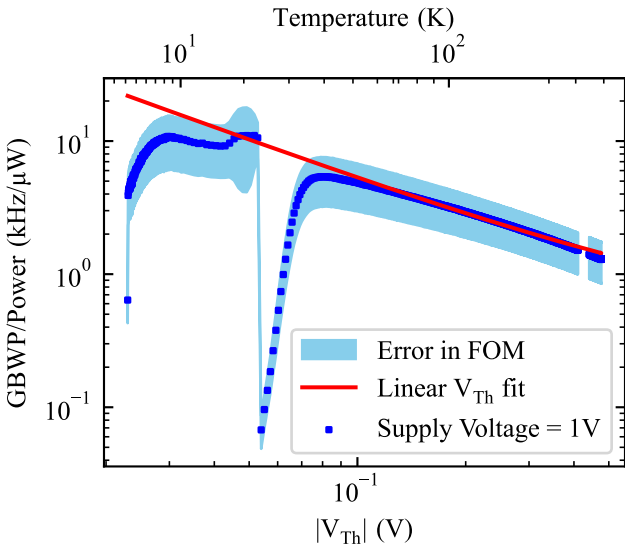

Figure 4.5: FOM of a common source amplifier as a function of $|V_{Th}|$ and temperature: Here the red line is a fit of Eq. 4.10 and the light blue is the uncertainty in the FOM measurement. The uncertainty was given by the product of the relative uncertainty of the GBWP and the FOM value, as the uncertainty in the power was considered negligible. The relative uncertainty in the GBWP was given by the addition of the relative uncertainty in the gain and the bandwidth added in quadrature. The uncertainty in the gain was given by the standard error in the values taken for the linear gain, i.e. the values taken in the 10Hz-100Hz range. The uncertainty in the bandwidth (δ_{BW}) was given by $\delta_{BW} = (f_{BW}[n+1] - f_{BW}[n-1])/2$, where $f_{BW}[n+1]$ and $f_{BW}[n-1]$ as the n+1 and n-1 values of frequency where $f_{BW}[n]$ is the bandwidth value. As such, the uncertainty is relatively large as the frequency was taken using a logarithmic scale. In this case this in turn made the uncertainty larger as at higher frequencies the spacing was much larger than at lower frequencies.

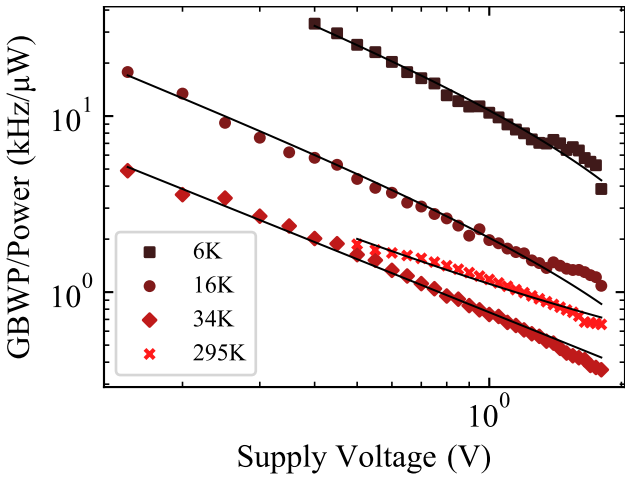

Figure 4.6: FOM vs Supply Voltage with changing temperature: Each curve is fitted by an inverse supply voltage fit. At each of these temperatures the amplifier was able to work at lower voltages than the room temperature amplifier. At 6 K the amplifier has an order of magnitude higher FOM at V_{CC} 1 V. Performance is reduced at 34 K due likely due to this temperature being close to the onset of freezeout, so the bias conditions in the amplifier could be unstable.

4.4 Conclusion

This section uses commercially available FETs to demonstrate that with careful selection of room temperature threshold voltage it is possible to demonstrate efficiency savings in a simple cryogenic electronics application, a common source amplifer. The efficiency of this amplifier was given by a FOM, the ratio of the Gain-Bandwidth-Product to the power consumption. This FOM was first calculated analytically and it was found that the FOM was inversely proportional to V_{Th} in the case where the amplifier was in saturation. The analytical expression was then validated by LT SPICE simulation. The amplifier was then built and cooled. This demonstrated an order-of-magnitude increase in the FOM from 295 K to 6 K, that was attributed to the threshold increase and not other factors like a reduction in phonon scattering.

If this technique is applied to FETs in a modern semiconductor process it could allow the creation of lower voltage supply circuitry for bulk FETs. Very recent work by SemiQon [140] demonstrated its own transistors which have extremely low (0.8 mV/dec) subthreshold swing at cryogenic temperatures. This would allow the turning on and off of the transistors within extremely small voltage range. Combining this with a low threshold, provided by a backgate, allows for the operation of dynamic circuitry at extremely low voltage supplies (less than 0.1 V). As the power consumption of dynamic circuitry is proportional to the square of the supply voltages, this would significantly push the power consumption down. This work and this thesis are comparable in the respect that they aim to use the unique properties of transistors at cryogenic temperatures to create extremely low power consumption electronics. This work demonstrates that the reduction in threshold part of this process can be achieved for bulk FETs (which lack back biasing). The most obvious usecase that would benefit from this is the supporting electronic infrastructure for quantum computing that are designed with bulk FETs rather than FD-SOI based. This would allow greater flexibility in circuit design by allowing for parts of the electronics to be powered by much lower supply voltages, which could in turn allow for power savings.

Chapter 5

External thermometry of a Cryo-CMOS platform at mK temperatures

This chapter describes the monitoring of the temperature profile of materials and devices found in a typical quantum computing set-up as a function of the power dissipation of an IC at 20 mK. Alongside this a thermal management technique unique to low temperature operation is also demonstrated, with superconducting wirebonds acting as a heat switch.

In this chapter, Section 5.1 describes the electrical set up, devices, and their mounting in the cryostat. Section 5.2 first demonstrates the calibration of the NbN thermometers against both the MXC thermometer and a CBT mounted at the MXC. After this, the temperature of each of the components of the setup is given as a function of power dissipation inside the IC and the external magnetic field. Finally, Section 5.4 concludes this work.

The IC's in this chapter were supplied by Forschungszentrum Jülich and designed by P. Vliex and A. Cabrera-Galicia. L.Shreckenberg both helped with the experi-

ments and helped to coordinate the experiment. The interposer was also supplied by Forschungszentrum Jülich and was created at the Helmholz Nano Facility. The niobium nitride thermometers were supplied by O. Bourgeois and V. Doebele at Institute NEEL, Univ. Grenoble Alpes thermometers.

5.1 Set Up

The set-up in this work was designed to mimic the materials and interfaces present in typical quantum computers at low temperatures. Thermometers were placed at key locations around this setup to understand the effect of power dissipation of an IC on the temperature of the surrounding environment. Figure 5.1 shows a photo of this setup.

The two ICs in the setup are fabricated used 65 nm CMOS technologies with various devices in both. Ultra-high purity copper was used as a mount to connect to the MXC, chosen for its low thermal resistance, mechanical robustness and machinability. The PCB, made of FR4 with additional copper layers and connections, contained low pass filters and connectors for outer DC electronics. Despite FR4's poor thermal conductivity at low temperatures, it was better thermalised to the cold copper via gold-plated holes at screw locations. A tight metal-on-metal connection between the cold copper and the PCB ground plane helped thermalise it to the MXC. The ICs were glued to a silicon interposer and the interposer to the copper mount using GE varnish, ensuring maximal thermalisation to the MXC. An interposer was used in this set up as interposers provide high density electrical connections, which in the future could be key to integrating the many different chips needed to control and readout a quantum computer [142].

A cold finger made of annealed silver, screwed directly into a copper holder, was

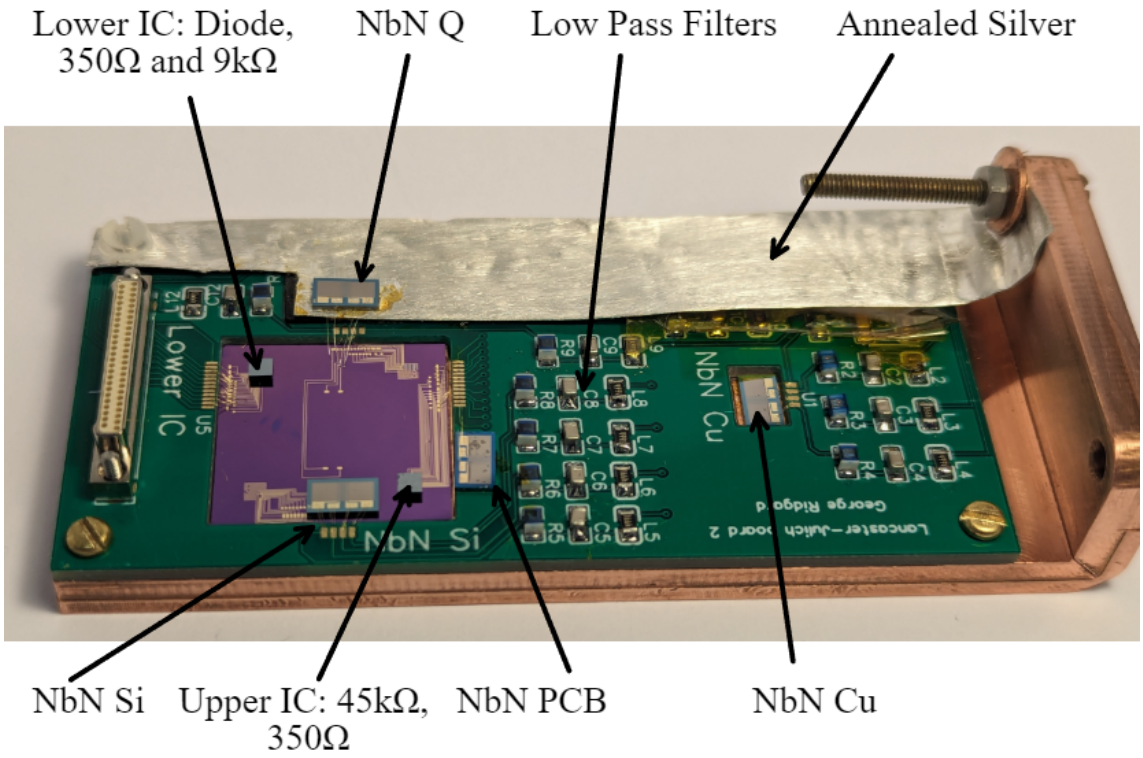

Figure 5.1: The four thermometers (the same Niobium Nitride, NbN, based as in Section 2.1.1), NbN Q, NbN Si, NbN PCB and NbN Cu are niobium nitride thermometers with $\mathrm{RRR}_{300\mathrm{K}-77\mathrm{K}}$ of 3.2, 3.1, 19, and 3.1 respectively. All these thermometers with the exception of NbN Q are gold bonded directly to the PCB. All of these thermometers are low pass filtered on PCB by a RLC filter consisting of a $5\ \mathrm{k}\Omega$ thin film resistor in series with a $560\ \mathrm{nH}$ wirewound inductor and in parallel with a $180\ \mathrm{pF}$ ceramic capacitor. This has a cut off frequency of approximately 15 MHz. The annealed silver strip is constituted of high purity silver has a $\mathrm{RRR}_{300\mathrm{K}-4\mathrm{K}}$ of 284 (measured at Lancaster by the author), which is commensurate with the literature [141]. This was measured in a helium-4 dewar. The interposer cut into the centre of the PCB is $20\ \mathrm{mm}^2$, which is cut from a single silicon crystal (orientation $\langle 100 \rangle$) wafer of thickness $550\ \mu\mathrm{m}$. The tracks on the interposer are 300 nm thick gold with 5 nm of titanium to bind the gold tracks to the silicon crystal.

added to the setup. An ABS spacer, chosen for its poor thermal conductivity, was used to prevent contact with the PCB to avoid thermal shorts. The spacer was 3D printed in a hollow frame design to further minimize the surface area of contact. The cold finger was designed to hold a thermometer that mimicked a qubit, keeping it cold while connected to the hot electronics on the interposer. The thermometer was bonded to the interposer with aluminum wires, which are superconducting at millikelvin temperatures and exhibit poor thermal conductivity due to phononic thermal conduction when superconducting as per Section 2.3. Studying the effects of breaking the superconductivity of the bond wires under a magnetic field on the thermometer helps to understand their role in shielding sensitive devices from the thermal effects of IC power dissipation. Figure 5.2 demonstrates a simplified diagram of this. The thermometers that are used to keep track of the temperature in this set up are all connected via four-terminal lock-in connections and are all measured simultaneously. Figure 5.3 demonstrates the electrical setup.

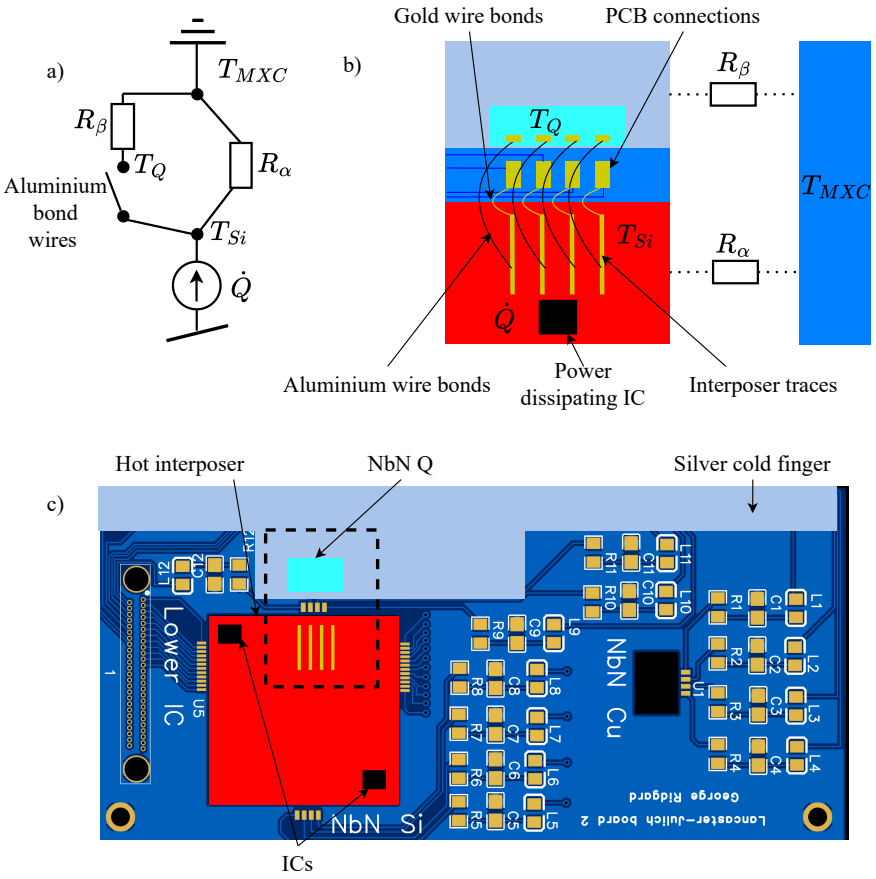

Figure 5.2: a) A simplified thermal circuit of the superconducting wire connections. Here $\dot{Q}$ is the power dissipated by the IC, T_{Si} the temperature of the interposer, T_Q the temperature of the thermometer on the cold finger, and T_{MXC} the mixing chamber temperature. The thermal resistance, R_β denotes the thermal resistance from the thermometer to the MXC, this will primarily be mediated metals (the silver cold finger and copper mount) and the TBR between metals and hence will be low. It should be noted that R_β also encompasses the electron-phonon coupling in the NbN thermometer, as well as the thermal conduction through the chip itself. R_α, represents the thermal resistance from the hot interposer to the MXC. b) Demonstrates the physical setup. NbN Q is connected to the gold interposer traces by aluminium wire bonds. As this thermometer has to be readout by four-terminal measurement, it is connected to the PCB by gold bond wires. c) The dotted box on this figure demonstrates where the setup is located on the PCB.

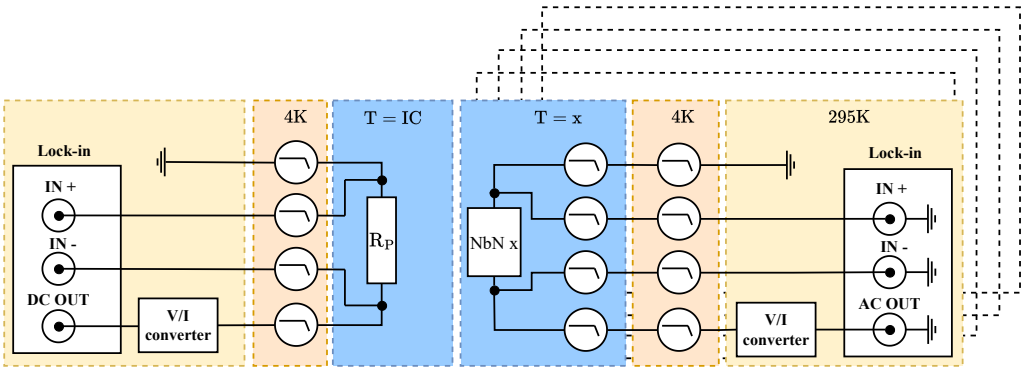

Figure 5.3: Electrical setup: On the right hand side, the thermometers (NbN x) are all double filtered and readout by lock-in amplifiers so to maximise their SNR. The dotted boxes behind the thermometer setup illustrates there are five of these thermometer connections. On the left, a four terminal setup for applying power through R_P is demonstrated.

5.2 Temperature as a Function of Power and Magnetic Field

5.2.1 Calibration

The niobium nitride thermometers were first calibrated against the cryostat ruthenium oxide thermometer at the MXC. This was a pre installed thermometer that is well thermalised to the MXC and is read out by a Lakeshore resistance bridge. Despite the fact that the ruthenium oxide was calibrated when it was first installed, it was calibrated again by CBT, located near to the MXC, to ensure the calibration had not changed significantly since installation.

5.2.1.1 Fridge RuOx Calibration

A CBT was used in the self-calibrated mode described in 2.1.2. The DC characteristics were taken at base temperatures, 30 mK, 60 mK, and 90 mK, operating in primary mode (DC current bias swept to capture the conductance dip and its asymptotes). These sweeps were fitted to a master tunneling model to generate

a lookup table that correlated the electron temperature in CBT with the height of the conductance dip at zero DC voltage. The dip minima were found by cooling the CBT to base temperature and sweeping the DC current bias to maximize the voltage response on the demodulated AC signal. This corresponds to the conductance minima (resistance maxima) at 0 V DC across the CBT. The conductance dip can shift due to factors like DC offsets in the amplifier chain, so research has focused on automating the process to ensure the DC bias aligns with the conductance minima [36].

Here the temperature was stepped from 20 mK to 100 mK. Figure 5.4 demonstrates the electron temperature against the MXC temperature. This gives good agreement with the fridge in the range 20 mK to 70 mK which is its intended use range and confirms that the fridge thermometer has no major drifting of its values. At temperatures higher than 70 mK the temperature diverges and the spread of the CBT temperatures becomes larger. This is because the conductance dip becomes much weaker at higher temperatures (when $k_B T >> E_C$), making it much more difficult to accurately determine the temperature.

5.2.1.2 NbN Thermometer Calibration

After the MXC thermometer had been calibrated against the semi-primary CBT, the NbN thermometers were calibrated against the MXC thermometer. A total of ten points were taken at each temperature step, with a settling time of 3 s per point and a 3 s sweep delay, giving a total of 33 s per point. The first step to ensure adequate thermalisation was that the MXC temperature setting program had to have two consecutive temperature readings within a defined threshold of the target temperature before it allowed the values to be taken. This process took on the order of 5 mins per step. The temperature steps were also made to be small reduce the risk of the puck not being thermalised with the MXC. In the interval 16 mK to 360 mK the temperature step was 2 mK, from 360 mK onwards this was

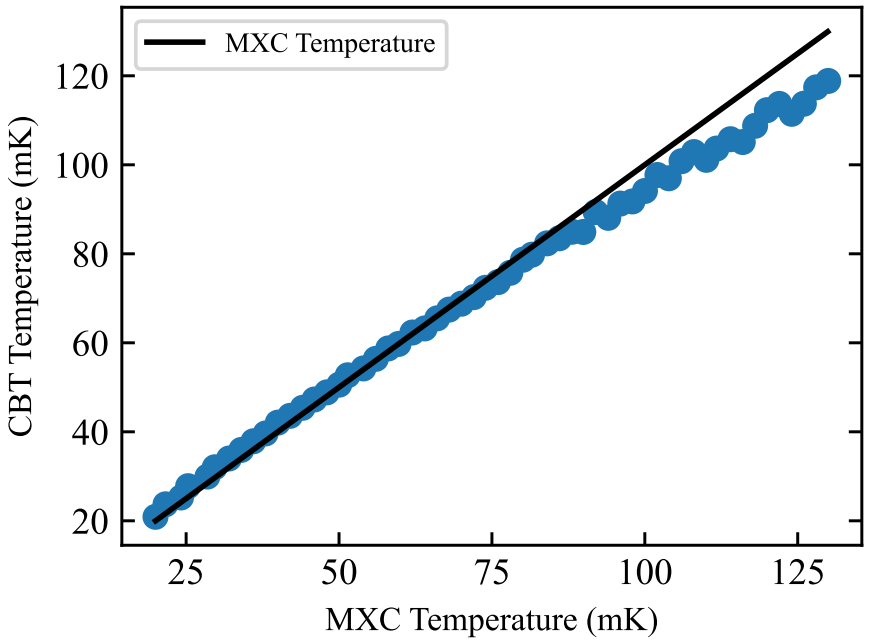

Figure 5.4: CBT electron temperature against dilution refrigerator MXC temperature, measured by the pre calibrated ruthenium oxide thermometer installed in the refridgerator: The CBT is operated in self calibrated mode.

5 mK.

Each of the NbN thermometers had different resistance values, however NbN Si had an especially high value of $360\ \mathrm{k}\Omega$ at base temperature. This is unexpectedly high value as the other NbN with the same $RRR_{300K-77K}$ (NbN Cu) had a resistance on the order of $100\ \mathrm{k}\Omega$. To ensure this thermometer didn't overheat due to the AC excitation, it was cooled to 30 mK (as at this temperature, temperature stability of the MXC was better than at 20 mK) and the AC excitation was varied and the power across the thermometer recorded. Figure 5.5 demonstrates this. It

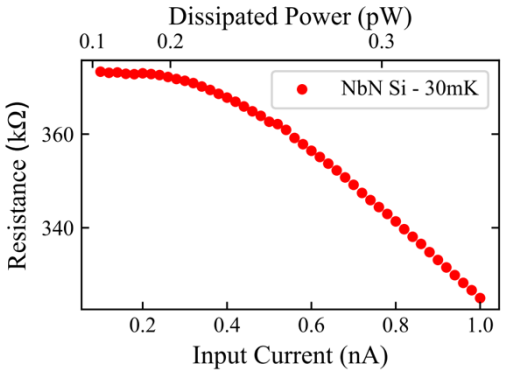

Figure 5.5: Power dissipation testing in a NbN thermometer with RRR of 3.1: Input AC excitation swept from 0.125 nA to 1 nA. The decrease in the resistance after 0.2 nA suggests the thermometer is overheating from the applied power.

was found that after 0.2 nA the resistance of the resistor starts to dip, indicating overheating. This equated to 0.2 pW of power dissipation. The rest of the thermometers had acceptable SNRs at this excitation so this was used for all thermometers.

All the thermometers were calibrated in a zero field environment and at 100 mT (z axis). As bulk aluminium has a critical field of approximately 10 mT [143], this field ensures that they would be normal instead of superconducting. The NbN thermometers have low magneto-resistance at low temperatures [22], as such the

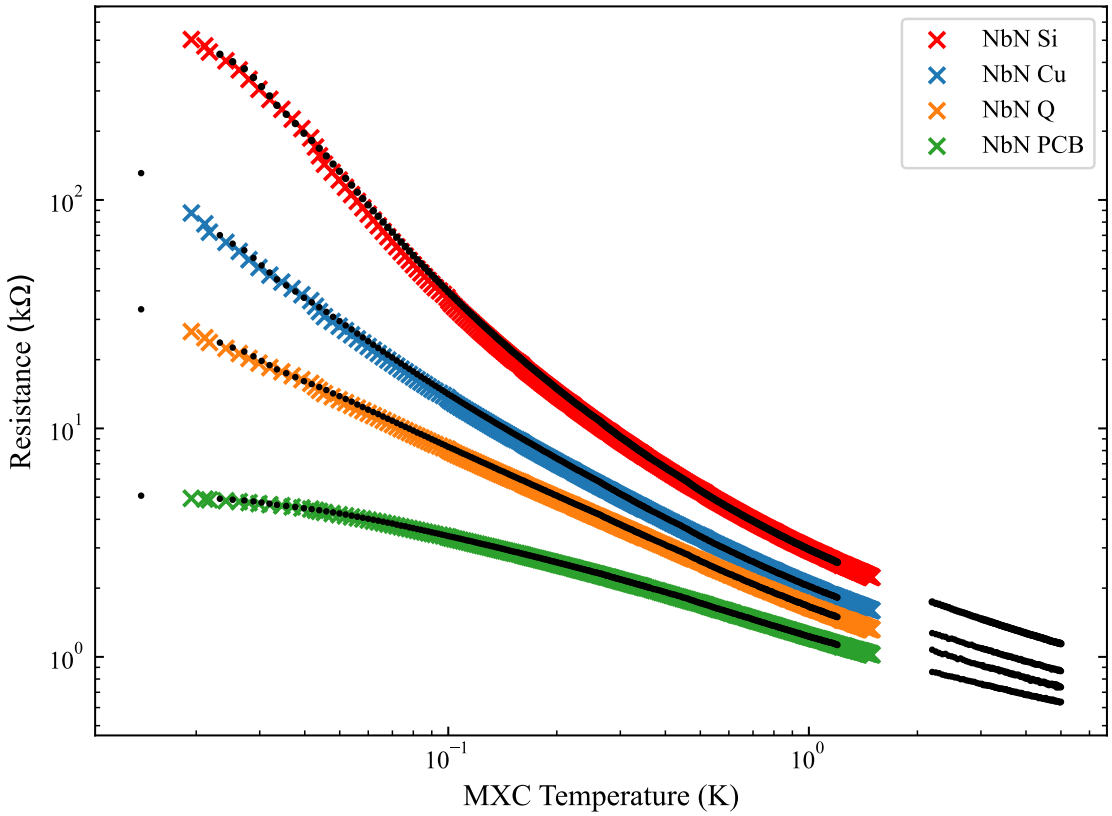

Figure 5.6: Multiple NbN thermometers calibrated against dilution refrigerator MXC temperature: Crosses denote calibration in the 100 mT field, the black dots are values with the field off.

both calibrations are extremely similar. Figure 5.6 shows the calibration.

5.2.2 Measurements

After calibrating the thermometers, the thermal behaviour of the setup was tested by applying power through the power IC with the field on and off. Data were taken in four sections, low power 1 nW to 1 μW and 1 μW to 100 μW in the high power section. These sweeps were then repeated in a 100 mT field to ensure that the superconductivity in the Al wires was broken. In the high power section the current was swept in 0.1μA steps. In the low power mode, it was swept in 10 nA steps. At each step the temperature was recorded 11 times and the average

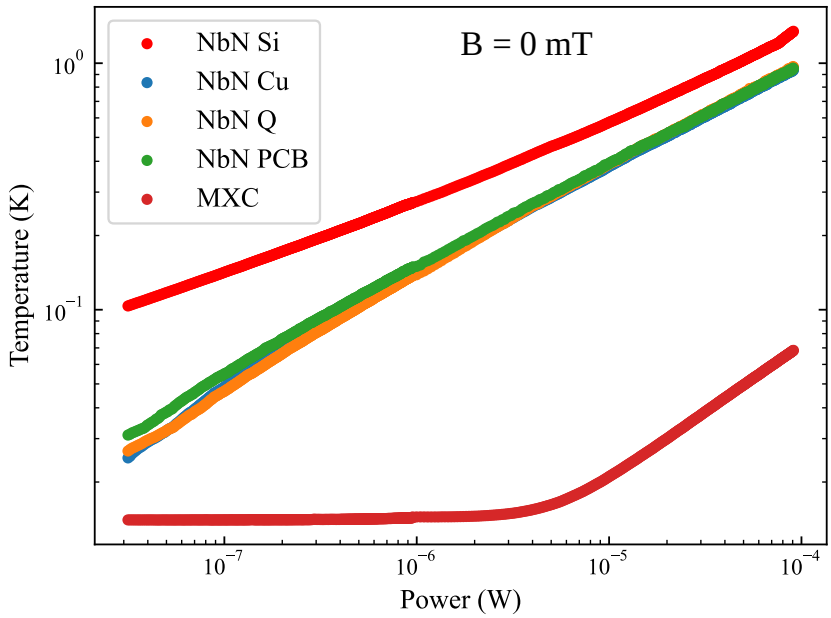

Figure 5.7: Temperature dependence of various NbN thermometers with magnetic field off.

value taken. The settling time for each value was 3 s per temperature point and the settling time for each power step was 3 s. This meant that for each power step there would be 33 s of settling time, which was considered enough time for thermalisation given the small power dissipation step size. This data was then pieced together. The results of this are shown in Figures 5.7 and 5.8.

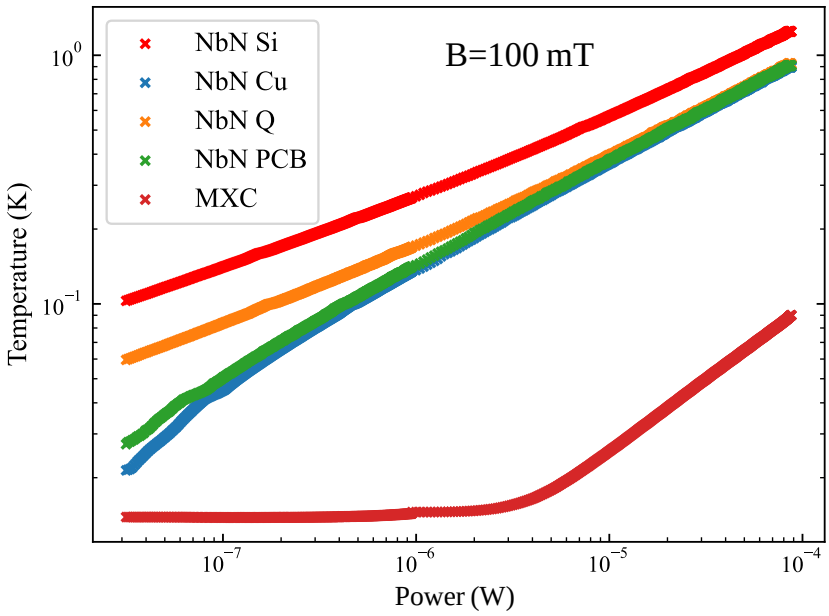

Figure 5.8: Temperature dependence of various NbN thermometers with magnetic field at 100 mT.

5.3 Analysis

5.3.1 Material Temperature Commentary

5.3.1.1 Copper Temperature

The first temperature dependence of note is the temperature of the copper holder, NbN Cu. At low powers this exhibits temperatures that are much higher than the MXC. For example, at 100 nW power dissipation, the copper holder is approximately 50 mK while the MXC is still at a base temperature of 15 mK. This was unexpected as the metal-metal interface between the MXC and the holder should be a low thermal resistance boundary, and therefore the two should be well thermalised. This data can be compared with that of a previous experiment, which was used to plan this experiment. It used exactly the same copper mount and nominally identical PCB, it also had NbN thermometers in exactly the same locations on the copper and interposer, however it did not contain the cold finger

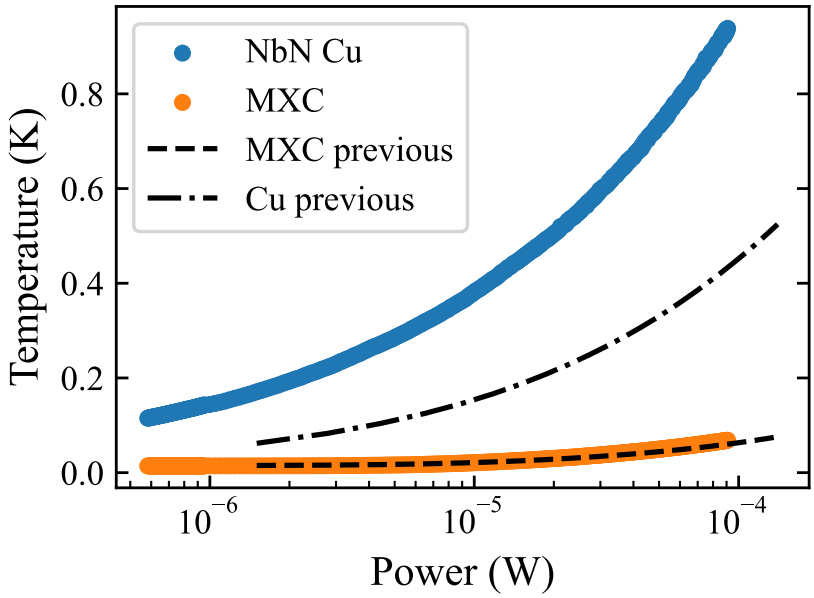

Figure 5.9: Comparison of MXC and NbN Cu temperatures in separate, but nominally identical experiments. While both MXC temperatures follow very similar power-temperature dependencies, the NbN Cu in the previous experiment is much colder at every power step. As the mount and the location of NbN Cu is exactly the same in both experiments, one explanation is a change in the boundary resistance between the mount and the cold plate on the fridge.

or the NbN PCB measurement. Data comparing the two experiments is shown in Fig. 5.9 demonstrates the NbN Cu is significantly colder at every power dissipation in the previous experiment. The thermal conductivity between the MXC and the copper holder can be given in the same form as Eq. 2.28 as we know that all the power that is dissipated in the IC must leave through the copper holder-puck boundary. In the regime where the MXC temperature is much lower than the copper temperature (at $1\ \mu$W and greater), this equation reduces to

$$Q = \frac{A}{L(n+1)}\Lambda T^{n+1}. \tag{5.1}$$

However as the copper is not an ideal rod as presupposed in this equation, we have to fold the surface area and length dimension dependencies into a constant,

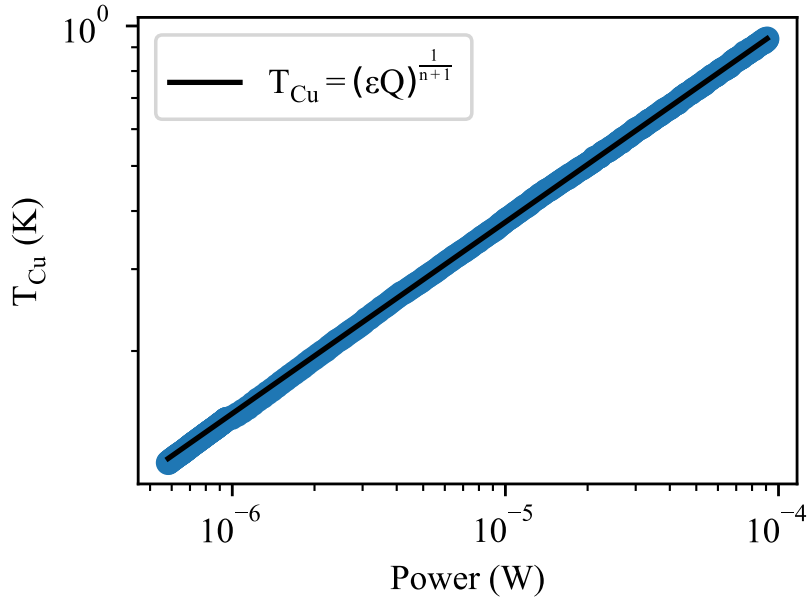

Figure 5.10: Temperature of the NbN Cu as a function of power, in the region where power is greater than $1\mu W$. The fitting of the equation in the legend gives n as 1.423 ± 0.001.

as neither of these are well defined in our system. However, the exponent still gives us information as to the dominant conduction method from the copper to the MXC. The exponent can then be found by plotting

$$T = (\epsilon Q)^{\frac{1}{(n+1)}} \tag{5.2}$$

and doing a least squares fit where both ϵ and n are fitting parameters. The results are plotted in Fig. 5.10. Given the exponent is close to one suggests electron based thermal conductivity is dominant. One potential explanation for the lack of thermalisation between the two is that there was not enough force connecting the copper mount and the cold plate of the refrigerator. This could be the result of user error when operating the refrigerator's bottom loaded sample mount. If there is a lack of force between the copper mount and the cold plate, the influence of surface asperities at the metal-metal boundary can reduce the effective contact area between both metals significantly. As this is the the primary

thermal connection to the cooling power of the MXC, it means that it will also have a significant impact on the other temperatures in the setup.

The second point of commentary is that the PCB temperature tracks the temperature of the copper holder in both field and non field conditions. This means that the PCB is well thermalised, likely due to the direct connection of its ground planes to the cold copper by the screw holes in the PCB. As the ground planes were well thermalised with the copper they provided a high contact to the FR4 board, which, despite the fact its an insulator, allowed it to thermalise well.

5.3.1.2 Interposer Temperature

Next, the interposer temperature exceeds all other temperatures in the setup at all powers and isn't dependent on magnetic field. This was expected due to silicon's poor thermal conductivity at low temperature. However, the thermal path from the silicon to the cold copper is further restricted by the presence of a silicon-GE varnish-copper interface. This interface is insulator-metal and as such the thermal boundary resistance and the impact of phonon mismatch becomes important. It is likely this thermal boundary resistance adds significantly to the total thermal resistance from the IC through the silicon interposer and to the copper. The significant heating shown by the interposer means that the integration of thermally sensitive ICs (especially ones containing qubits) will not be possible without significant thermal mitigation.

5.3.1.3 NbN Q/Cold Finger Temperature

We investigated a solution to the hot interposer by using the setup shown in Fig. 5.2. In this setup our cold electronics are simulated as the NbN Q thermometer and superconducting wirebonds were used in order to break thermal connection to the interposer while maintaining electrical connection. The cold finger was used to better heat sink the thermometer. Firstly in the no field regime, the NbN Q

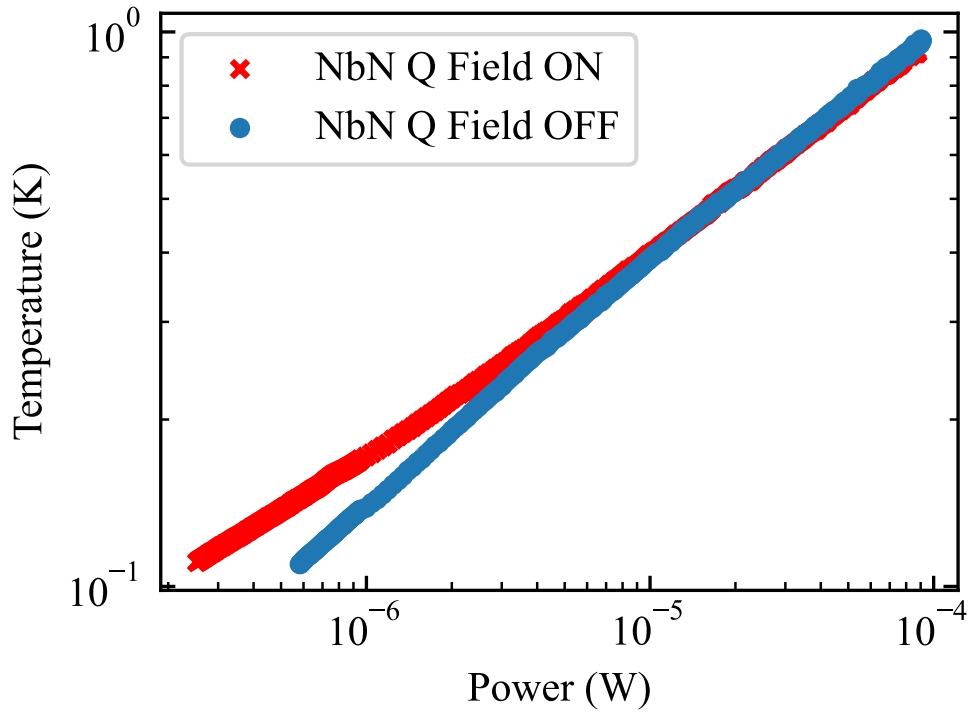

Figure 5.11: Temperature dependence of NbN Q in both field and non field conditions as a function of power. Here we see the temperature is larger for field on, meaning a decreased thermal resistance to the NbN Q thermometer. This could be explained by the increased thermal conductivity of the Al wirebonds which are normal metal in the field on state, rather than in a superconducting state in the field off configuration.

is well thermalised to the copper for the whole temperature range, which suggests that the annealed silver is well thermalised to the copper. This also suggests that NbN Q could be cooled further by better thermalising the copper to the MXC. Figure 5.11 demonstrates that the temperature of NbN Q is higher in a magnetic field environment, especially in the low power regime. This supports the idea that superconducting nature of the wirebonds restricted heat flow to NbN Q. However this behaviour is limited to the low power regime. One explanation for this is that interposer gets hot a higher powers and breaks the superconductivity in the Al wires. Figure 5.12 demonstrates the difference in NbN Q temperature as

a function of power and also interposer temperature to further investigate this. This means that the hot interposer may have broken the superconductivity in the wirebond, leading to the NbN Q increasing in temperature. Therefore this technique may be further improved by the use of niobium wirebonds, which have a much higher critical temperature of around 9 K. Niobium wirebonds have already been demonstrated [144]; however, as (pure) niobium has a critical field of 200 mT this is too small to still be superconducting at the fields required for silicon qubits (0.5T-2T) which could be a limiting factor.

While this work has demonstrated the effectiveness of using wirebonds, in the near future, 3D integration will be required to further scale up qubit count, meaning wirebonds will become less relevant. It has been shown that Through Silicon Vias (TSVs) with copper bump bonds (as opposed to superconducting Indium) help to reduce qubit temperatures by allowing the heat to be removed from the system [145]. The same logic, however, applies in the opposite direction; superconducting materials could be used to effectively block the flow of heat to the qubits. Work that could be used to implement this in higher field environments is underway, in the form of niobium TSV [146] devices. This could lead to thermal management techniques which use both superconductors and normal metals to guide the flow of heat though the quantum-classical infrastructure, carefully avoiding heating up the critical quantum areas.

5.4 Conclusion

In conclusion, we characterised the temperatures the components typically present in a quantum computing setup (copper mount, PCB and interposer) as a function of power dissipated in an IC. In the same setup we also demonstrated techniques to help keep a thermally sensitive device cold, that is to heat sink the material with a high thermal conductivity metal and use superconducting wirebonds as a

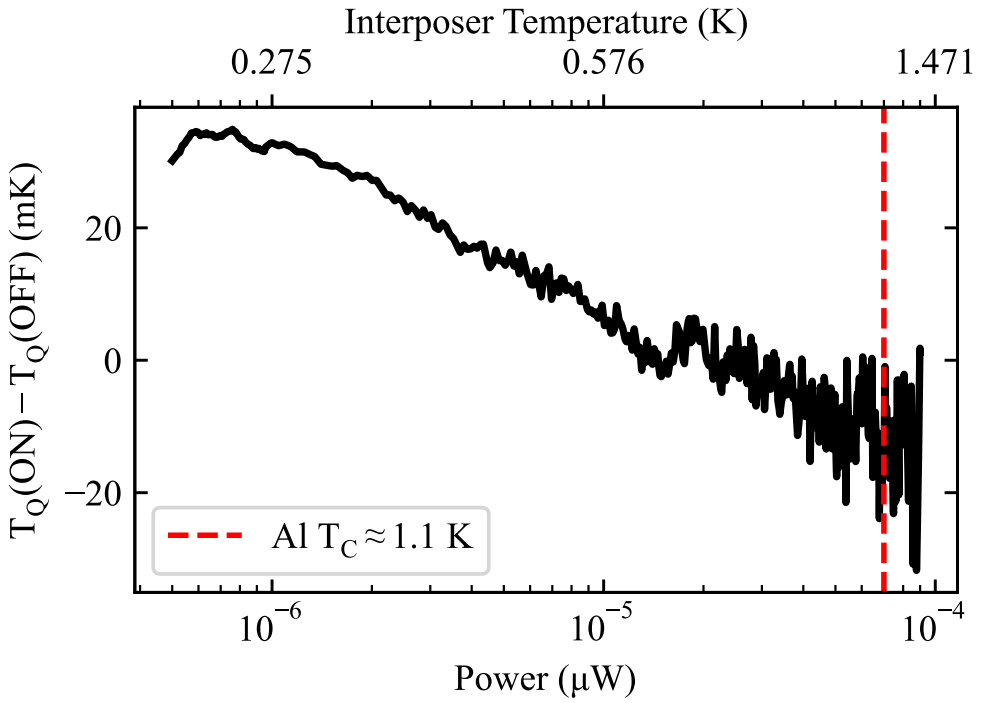

Figure 5.12: Temperature difference between NbN Q in both the field on ($T_Q(ON)$) and field off ($T_Q(OFF)$) states vs power and interposer temperature. The presence of a thermal difference between the ON and OFF states suggests that superconducting wirebonds have an effect on the thermal transport between the heat source and NbN Q. The fact that this difference starts to reduce as the power increases could be related to the critical temperature of the Al wires. As the interposer heats up the wires, it breaks the superconductivity and provides a reduced thermal connection meaning the ON and OFF states are now equivalent, meaning the difference goes close to zero. In this plot the red line is the textbook value of the T_C for aluminum to demonstrate when the temperature difference should be minimal. The fact that the temperature difference decreases gradually rather than sharply can be explained by Eq. 2.29 which shows the transition shouldn't be step function like. The temperature difference does also appear to go negative, however the spread in the data also increases at higher powers due to fewer points being taken at these levels.

thermal blocker to hot electronics. As for component temperatures; the interposer showed the most significant heating even at low power dissipation, at 1μW the interposer showed at temperature of 150 mK and was over 1 K at 100μW. This brings into question the potential for interposers to be used for the large scale integration of hot electronics and thermally sensitive qubit devices on chip. To mitigate these challenges, the use of both normal metal and superconducting TSVs was also discussed. As for the challenge of keeping a thermally sensitive device cold, it was found that at low power dissipations the superconducting nature of aluminium bonds can act as a significant thermal block. At an IC power dissipation level of 1μW the difference in temperature of the thermally sensitive test device (NbN Q, only thermally connected to the interposer by aluminum bonds) between the superconducting state (no magnetic field applied) and the non superconducting state (100 mT field applied) was 30 mK. Evidence also suggested that the reason the wires stop becoming such an effective thermal block at higher power dissipation is that the hot interposer exceeds the critical temperature of the bonds, turning them normal again. This suggests that using wire bonds with higher critical temperatures could help to extend this technique to higher power dissipation levels.

Chapter 6

Internal thermometry of a Cryo-CMOS platform at mK temperatures

This chapter describes the use of noise thermometry to determine the temperature of a resistor in an IC (the same IC mentioned in the previous chapter) developed by a commercial 65 nm CMOS process down to millikelvin temperatures. Noise thermometry makes an ideal thermometry method for low temperature, in-IC measurements, as it is both primary and dissipationless. To extend the utility of noise thermometry, a cross-correlation technique was used. In this chapter, the statistical properties of this technique are described in depth. More specifically, an expression is given which describes the relationship between the standard deviation of the cross-correlation spectrum, the number of averages taken, the noise floor of the amplifiers used and the noise of the CMOS. Furthermore, a technique that increases the speed of the cross-correlation convergence is outlined, and its application to speeding up noise thermometry is discussed. To the author's knowledge this technique has not been applied to thermometry yet.

In this chapter, Section 6.1 describes the statistics of cross-correlation and why it is

effective. This includes discussions on the different Gaussian distributions needed to fully describe the technique. It ends with a derivation of a series of useful equations which determine the efficacy of cross-correlation given the target noise floor and the read-out amplifier noise. Section 6.2 describes the setup, results and analysis of the experiment in which an IC was cooled and noise thermometry was performed. Section 6.4 describes a way to speed up the cross-correlation measurement at the expense of its primary nature. Finally, Section 6.6 concludes this section.

6.1 Cross-Correlation

The principles behind cross-correlation are introduced in Section 2.1.4, this Section details the mechanism by which the technique works. When performing cross-correlation, the noise level that is possible to measure, and therefore also the temperature that is possible to measure, is a function of the number of averages and the input noise of the amplifiers. To understand this relationship properly, we must first consider the statistics of cross-correlation. The following is structured upon E. Rubiola's work in [147], however, in this work we will include the explicit dependence on the input noise of the amplifier. Subsection 6.1.1 gives a background in the statistics needed to approach the concept, and Subsection 6.1.2 shows why cross-correlation works. It also gives expressions for the dependence of the standard deviation in the measurement as a function of the noise level you are trying to resolve, the number of averages taken, and the noise level of the amplifiers used.

6.1.1 Statistical Background and Definitions

6.1.1.1 Gaussian Distribution

In this analysis, understanding the Gaussian distribution is crucial, first because thermal noise is a Gaussian process and second because at the noise of amplifiers

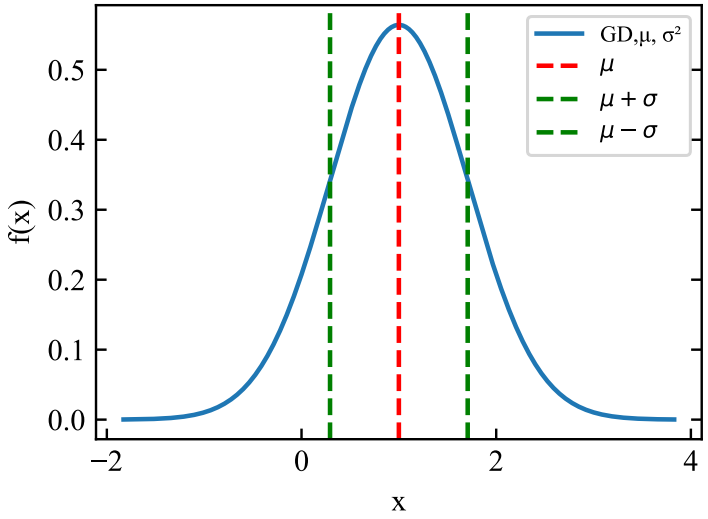

Figure 6.1: Gaussian Distribution with variance (σ^2) of 0.5 and average (μ) of 1.

the noise can be modelled as Gaussian (outside the influence of 1/f noise). The corresponding distribution for a normally distributed process x, with mean μ and variance σ^2 is

$$f(x) = \frac{1}{\sigma\sqrt{2\pi}} e^{-\frac{(x-\mu)^2}{2\sigma^2}}. \tag{6.1}$$

This gives the typical bell shaped curve shown in Figure 6.1. When discussing distributions such as this, the Expectation Operator $E[]$ is a powerful tool in predicting the behaviour of the distributions. This operator gives the ensemble average of whatever it acts upon. For example, we can find the average of the distribution,

$$E[f(x)] = \mu. \tag{6.2}$$

Other expectation values are well defined for the Gaussian distribution such as the average of the square of the distribution

$$E[f^2(x)] = \mu^2 + \sigma^2, \tag{6.3}$$

and the expected variance of the distribution, which as it will be useful later on, can be defined as $var[]$,

$$E[|f(x) - E[f(x)]|^2] = var[f(x)] = \sigma^2. \tag{6.4}$$

When averaging n distributions, the variance drops with the same factor as the number of averages, i.e.

$$var[\langle f(x)\rangle_n] = var[f(x)]/n. \tag{6.5}$$

To apply this to the thermal noise, the Johnson-Nyquist voltage noise can be described by a Gaussian distributed function of voltage as a function of time, V(t), with mean $\mu = 0$ and variance $\sigma^2 = 4k_BTR$ in a 1Hz bandwidth. For V(t), expectation value is given by,

$$E[V(t)] = \mu = 0 \tag{6.6}$$

and for $V^2(t)$ given by,

$$E[V^2(t)] = \sigma^2 + \mu^2 = \sigma^2. \tag{6.7}$$

In the case applying a Fourier transform to this time series, $\tilde{V}(f)$, results in a signal which contains both a real and imaginary part $\tilde{V}(f) = \tilde{V}_{Re}(f)+i\tilde{V}_{Im}(f)$. Both parts are statistically independent and both contribute equally to the signal variance, i.e. $var[\tilde{V}_{Re}(f)] = var[\tilde{V}_{Im}(f)] = var[\tilde{V}(f)]/2$. This applies more generally to Gaussian distributions.

6.1.1.2 Chi-square Distribution

Another important statistical distribution to understand cross-correlation is the Chi-Square distribution. This defines the sum of many normal distributed variables, x, with $\mu = 0$ and variance σ^2. As such,

$$\chi^2 = \sum_{i=1}^{r} x_i^2 \tag{6.8}$$

χ^2 is Chi-squared distributed with r degrees of freedom. The distribution is shown in Fig. 6.2. Where $f(x)$ is a Chi-squared probability distribution, the expectation operators for this distribution can be described by,

$$E[f(x)] = \sigma^2 r, \tag{6.9}$$

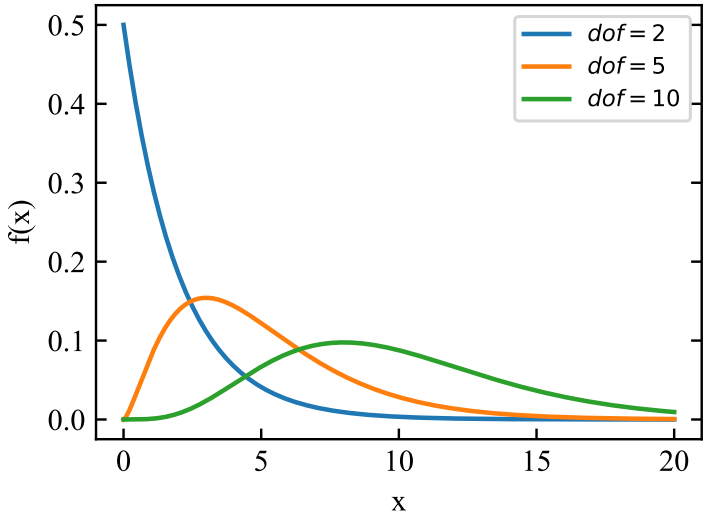

Figure 6.2: Chi-Squared distribution for different degrees of freedom (dof).

$$E[f^2(x)] = \sigma^2 r(r+2) \tag{6.10}$$

and

$$var[f(x)] = 2\sigma^4 r. \tag{6.11}$$

An example application of this distribution is the magnitude of a complex Gaussian distributed variable, $Y = Y_1 + iY_2$, where $|Y|^2 = Y_1^2 + Y_2^2$ is a Chi-Squared function with two degrees of freedom.

6.1.1.3 Bessel K_0 Distribution

The third key distribution in this analysis is the Bessel K_0 distribution, a modified Bessel function of the second kind. This distribution describes a variable x which is the product of two normally distributed variables, x_1 and x_2,

$$x = x_1 x_2. \tag{6.12}$$

This is plotted in Fig. 6.3. If x_1 and x_2 have variances σ_1^2 and σ_2^2 respectively, then x has a variance given by $\sigma^2 = \sigma_1^2\sigma_2^2$. This is plotted in Fig. 6.3. Its operator values can be given as,

$$E[f(x)] = 0 \tag{6.13}$$

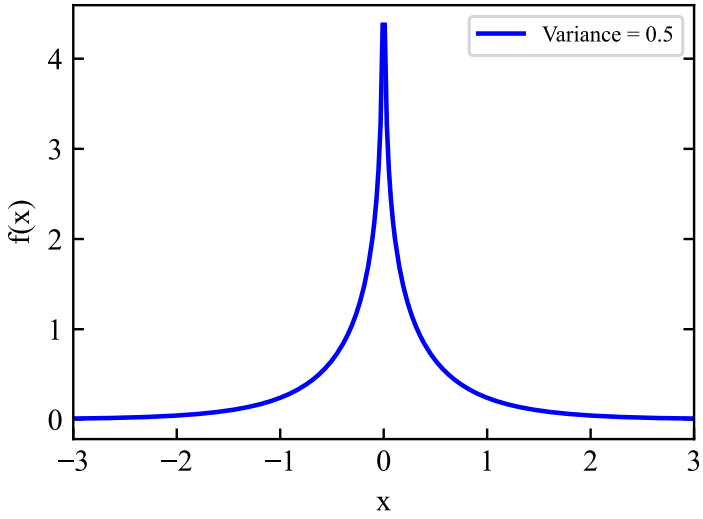

Figure 6.3: Bessel K_0 function with $\sigma^2 = 0.5$. Both sides of zero were plotted to avoid the singularity at zero.

and

$$var[f(x)] = \sigma^2. \tag{6.14}$$

6.1.2 Statistics of Cross-Correlation

For cross-correlation, we measure two channels simultaneously in order to resolve a signal below a noise floor, which is typically given by the noise floor of the amplifiers used to measure the common signal. In this case, the Johnson Nyquist noise of a resistor is the common signal (which is Gaussian) and the amplifiers can be modelled to have Gaussian noise in the frequency region not dominated by 1/f noise. In channel one, we measure the voltage V_1, which contains the sum of Gaussian noises ϕ (amplifier 1 noise) and θ (common Johnson Nyquist noise) and in channel two, V_2, we measure the noise ρ (amplifier 2 noise) and θ,

$$V_1 = \phi + \theta \quad \text{and} \quad V_2 = \rho + \theta. \tag{6.15}$$

The common noise in both channels θ has a variance (normalised in a 1Hz bandwidth) $\sigma^2 = X^2$, which in the case of our noise measurement is equal to the

Johnson-Nyquist noise. The other two noise sources have variance of $\sigma_\phi^2 = \sigma_\rho^2 = A^2$, in our experiment this is the input noise of both amplifier channels, equal in magnitude but separate, random processes. To generate the cross-spectrum $S_{V_1V_2}(f)$ we now take n averages of the following,

$$\langle S_{\tilde{V_1}\tilde{V_2}}(f)\rangle_n = \langle \tilde{V_1}(f)\tilde{V_2^*}(f)\rangle_n, \tag{6.16}$$

where the tilde denotes the Fourier transform and the star denotes the complex conjugate. We can remove the frequency dependence as the same applies to all frequencies,

$$\langle S_{\tilde{V_1}\tilde{V_2}}\rangle_n = \langle \tilde{V_1}\tilde{V_2^*}\rangle_n. \tag{6.17}$$

As we have taken the Fourier transform, all both channels now possess both real and imaginary parts with the form,

$$\tilde{V_1} = (\phi_R + i\phi_I) + (\theta_R + i\theta_I) \quad \text{and} \quad \tilde{V_2^*} = (\rho_R - i\rho_I) + (\theta_R - i\theta_I). \tag{6.18}$$

We can now calculate $\langle S_{\tilde{V_1}\tilde{V_2}}\rangle_n$, by splitting up the resulting product real and imaginary, as

$$\langle S_{\tilde{V_1}\tilde{V_2}}\rangle_n = \text{Re}\left[\langle S_{\tilde{V_1}\tilde{V_2}}\rangle_n\right] + \text{Im}\left[\langle S_{\tilde{V_1}\tilde{V_2}}\rangle_n\right]. \tag{6.19}$$

We get,

$$\text{Re}\left[\langle S_{\tilde{V_1}\tilde{V_2}}\rangle_n\right] = \langle \phi_R\rho_R + \phi_I\rho_I\rangle_n + \langle \phi_R\theta_R + \phi_I\theta_I\rangle_n \tag{6.20}$$

$$+\langle \theta_R\rho_R + \theta_I\rho_I\rangle_n + \langle \theta_R^2 + \theta_I^2\rangle_n \tag{6.21}$$

and

$$\text{Im}\left[\langle S_{\tilde{V_1}\tilde{V_2}}\rangle_n\right] = \langle \phi_I\rho_R - \phi_R\rho_I\rangle_n + \langle \phi_I\theta_R - \phi_R\theta_I\rangle_n + \tag{6.22}$$

$$\langle \theta_I\rho_R - \theta_R\rho_I\rangle_n. \tag{6.23}$$

To estimate the magnitude of the cross-correlation spectrum $S = |\langle S_{\tilde{V_1}\tilde{V_2}}\rangle_n|$, we do the following,

$$S = \sqrt{\text{Re}\left[\langle S_{\tilde{V_1}\tilde{V_2}}\rangle_n\right]^2 + \text{Im}\left[\langle S_{\tilde{V_1}\tilde{V_2}}\rangle_n\right]^2}. \tag{6.24}$$

The real part dominates, as it contains the $\langle\theta_R^2 + \theta_I^2\rangle_n$ term, we then take S to be,

$$S \approx \text{Re}[\langle S_{\tilde{V}_1\tilde{V}_2}\rangle_n]. \tag{6.25}$$

To assess the rate of non-correlated noise attenuation, we can calculate a relative error, $\frac{\delta S}{S}$, by calculating the ratio of the expected deviation to the expected value. This can be defined as

$$\frac{\delta S}{S} = \frac{\text{dev}\,[S]}{\text{E}\,[S]}, \tag{6.26}$$

where $dev[] = \sqrt{var[]}$. To do so, we calculate the total variance and expected value for Eq.6.20. The first three terms, which we denote A,

$$A = \langle\phi_R\rho_R + \phi_I\rho_I\rangle_n + \langle\phi_R\theta_R + \phi_I\theta_I\rangle_n + \langle\theta_R\rho_R + \theta_I\rho_I\rangle_n \tag{6.27}$$

contains three sums which contain Bessel K_0 distributions. Lets first consider the first of the three terms in A,

$$\langle\phi_R\rho_R + \phi_I\rho_I\rangle_n. \tag{6.28}$$

As we know that ϕ and ρ are Gaussian distributed with zero mean, we know,

$$\text{var}[\phi] = \text{var}[\rho] = \sigma_\phi^2 = \sigma_\rho^2 = A^2. \tag{6.29}$$

However in A we are working with the imaginary and real components of ϕ and ρ. In the example of ρ,

$$\rho = \rho_R + i\rho_I \tag{6.30}$$

As both real and imaginary contribute equally to the variance,

$$var[\phi_R] = var[\rho_R] = var[\phi_I] = var[\rho_I] = \frac{A^2}{2}. \tag{6.31}$$

We can then write the variance of Eq.6.28 as

$$\text{var}\,[\langle\phi_R\rho_R + \phi_I\rho_I\rangle_n] = (\text{var}\,[\phi_R\rho_R] + \text{var}\,[\phi_I\rho_I])\,/n, \tag{6.32}$$

which is just the sum of the variance of two Bessel K_0 functions. From Subsection 6.1.1.3 we know that the variance of a Bessel K_0 function is the product of the

variances of the distributions which make it up. Putting this together along with Eq. 6.31, we arrive at,

$$\text{var}\left[\langle\phi_R\rho_R + \phi_I\rho_I\rangle_n\right] = \left(\frac{A^2}{2}\frac{A^2}{2} + \frac{A^2}{2}\frac{A^2}{2}\right)\frac{1}{n} = \left(\frac{A^4}{4} + \frac{A^4}{4}\right)\frac{1}{n} = \frac{A^4}{2n}. \tag{6.33}$$

If we continue this reasoning then for the first three terms we arrive at a total variance of

$$var\left[A\right] = \frac{A^2}{2n}\left(A^2 + 2X^2\right) \tag{6.34}$$

and the expectation value,

$$\text{E}\left[A\right] = 0 \tag{6.35}$$

as expectation value for any given Bessel K_0 is zero.

Now we look at the final term in Eq.6.20, which we denote B, is Chi-Squared distributed,

$$B = \langle\theta_R^2 + \theta_I^2\rangle_n. \tag{6.36}$$

with 2 degrees of freedom. Given we know $var[\theta_R] = var[\theta_I] = \frac{X^2}{2}$, using Eq. 6.11 we arrive at,

$$\text{var}[B] = 2\left(\frac{X^2}{2n}\right)^2 2n = \frac{X^4}{n}. \tag{6.37}$$

As for the expectation value of B, using Eq. 6.9,

$$E[B] = 2\cdot\frac{X^2}{2} = X^2. \tag{6.38}$$

Finally, if we calculate the total variance of S we know,

$$S \approx A + B \tag{6.39}$$

and as such,

$$var[S] = var[A] + var[B] \tag{6.40}$$

which then equates to

$$var[S] = \frac{A^2}{2n}\left(A^2 + 2X^2\right) + \frac{X^4}{n} \tag{6.41}$$

and tidying the expression up and taking the square root to find the $dev[]$, we get,

$$dev[S] = \sqrt{\frac{(A^2 + X^2)^2 + X^4}{2n}}. \tag{6.42}$$

Equation 6.42 was verified by simulation. The two channel time series were modeled using *numpy.normal.random* to first generate a time series for the voltage response of a $9\ \mathrm{k}\Omega$ resistor at 2 K, 5 K, 10 K, 20 K and 50 K (the common thermal signal). Next, two separate random time series with the same standard deviation were generated to represent the output noise of the two amplifiers (both with noise equivalent to $4\ \frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$). The common signal was then added to both time series of the amplifiers to create a simulation of what each amplifier would measure. The resulting time series were then processed according to Section 6.1.2 and repeated one thousand times. Then a rolling count of the standard deviation of each cross-correlation spectra was calculated. The results are shown in Fig. 6.4. From Eq. 6.42 we can derive another useful quantity, the relative error in our experiment. The average is $E[B] = X^2$ so the relative error is then given by,

$$\frac{\delta S}{S} = \frac{dev[S]}{\mathrm{E}[S]} = \frac{1}{X^2}\sqrt{\frac{(A^2 + X^2)^2 + X^4}{2n}}. \tag{6.43}$$

This expression can be compared with Rice's relationship [148, 149] which is given by the following,

$$\frac{\delta S}{S} \geq \frac{1}{\sqrt{\tau \Delta f}} \tag{6.44}$$

where τ_{Int} is the integration time and Δf is the correlation bandwidth. In the case of analog cross-correlation, we note that

$$n = \tau_{Int}\Delta f. \tag{6.45}$$

It should be noted that this time is different from the time per spectral acquisition in the digital method, $\tau_{Spectra} = \frac{N}{f_{sample}}$, where N is the number of samples in a spectra and $f_{sample} = 2\Delta f$ is the sample rate. This recovers the Nyquist-Shannon theorem that when $\tau_{Int} = \tau_{Spectra} = \tau$, n=1, $N = 2\tau\Delta f$. We find that both

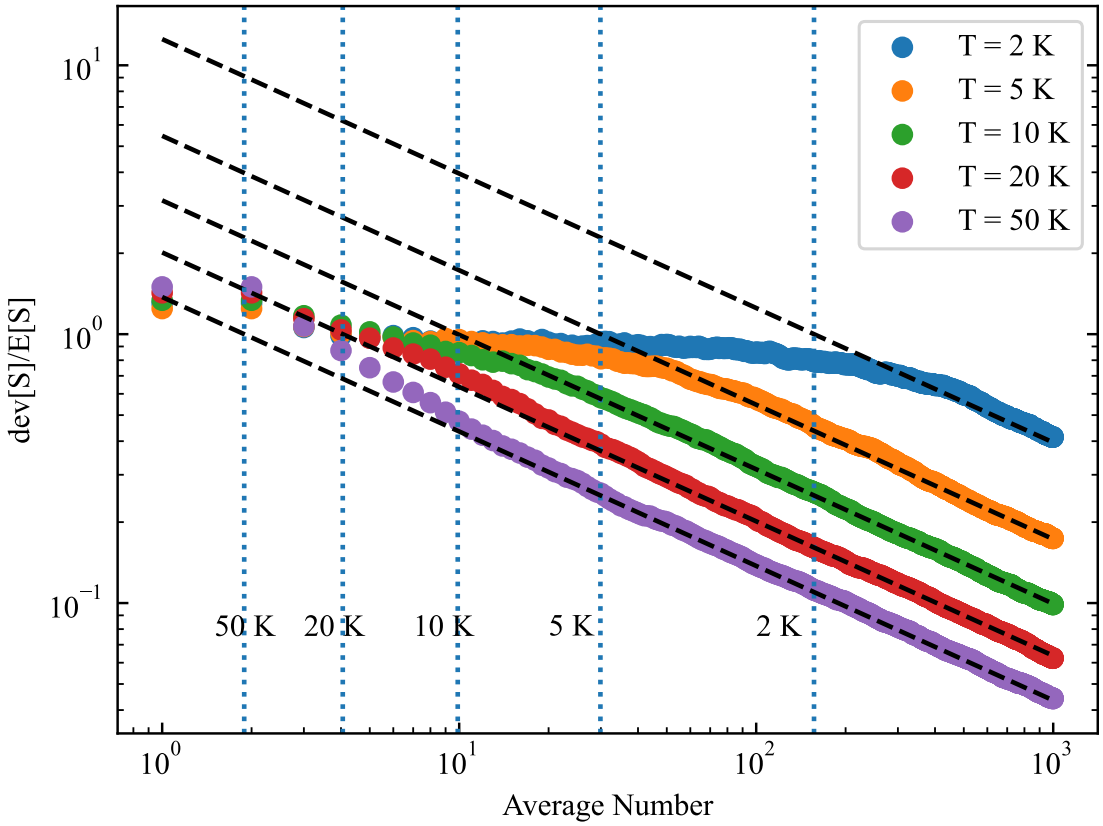

Figure 6.4: Simulation of the ratio of the standard deviation ($dev[S]$) and the expectation value ($E[S]$) of the cross-correlation for five different temperatures of a $9\text{k}\Omega$ resistor. The dashed line denotes the theoretical uncertainty given by Eq. 6.43. The dotted lines denote the number of averages it takes to converge the cross-correlation for each resistor, given by Eq. 6.46 (from left to right in increasing resistances). After the cross-correlation has converged, the standard deviation then drops with $1/\sqrt{n}$. This plot also demonstrates the standard deviation derived agrees with the theory developed. This was simulated in python with standard numpy and scipy packages.

equations agree that $\frac{\delta S}{S} \propto \frac{1}{\sqrt{\tau \Delta f}}$. We can re-arrange Eq. 6.43 to find the number of averages needed so the relative error will be less than unity,

$$n > \frac{1}{X^4}\left(\frac{\left(A^2+X^2\right)^2+X^4}{2}\right). \tag{6.46}$$

This is a useful expression as it gives an idea as whether it is possible to resolve a noise floor with this technique within a realistic number of averages. The condition that $E[C] = dev[S] = X^2_{DUT}$, (where X^2_{DUT} is the true device under test noise) is the condition for convergence of the cross-correlation. After this condition is fulfilled, the standard deviation of the resulting spectra then reduces with $1/\sqrt{n}$ as with a normal FFT averaging. With further manipulation we can use this equation to find the noise value measurable given n averages and an amplifier noise A^2,

$$X^2 = \frac{A^2}{\sqrt{2n-1}-1}. \tag{6.47}$$

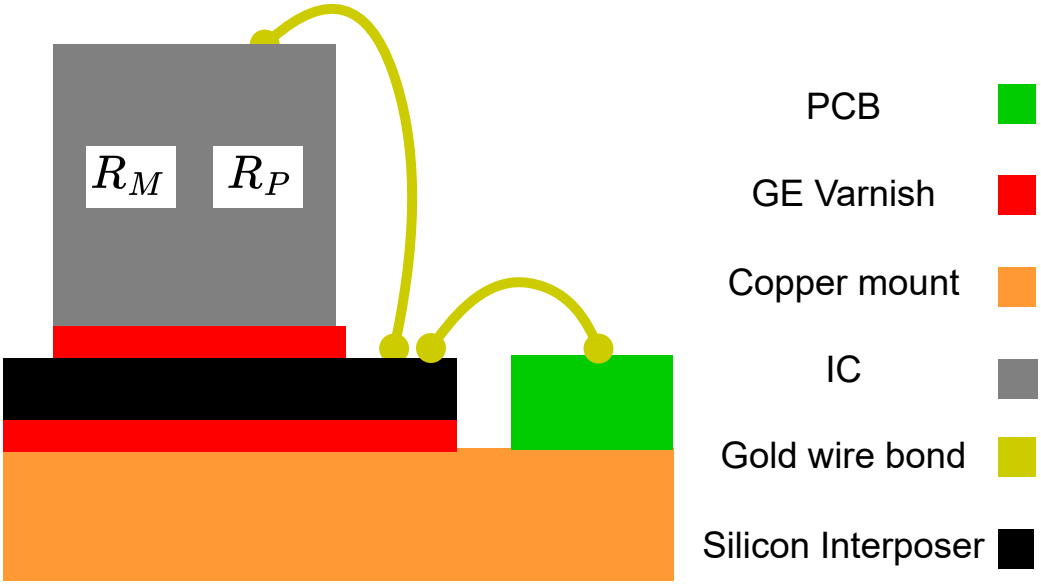

Figure 6.5: Illustration of the experimental arrangement

6.2 Experiment

This section describes the measurement of the voltage noise in a $45\ \mathrm{k}\Omega$ resistor in a dilution refrigerator. The physical setup and mounting of the device is described in Subsection 6.2.1. The electrical methods used to readout the noise and the signal processing is described in Subsection 6.2.2.

6.2.1 Physical Setup

Figure 6.5 shows the setup of the IC, which is the same 1mm x 1mm chip, used in the previous Section. It is attached to the same setup used in the previous section, which is composed of a copper mount attached to the puck, with an interposer on the copper and the IC on the interposer. The relevant devices inside the IC for this Section are a $350\ \Omega$ power resistor, R_P, and a $45\ \mathrm{k}\Omega$ measurement resistor, R_M. The setup unit is cooled in the same *Oxford Instruments Triton 400*.

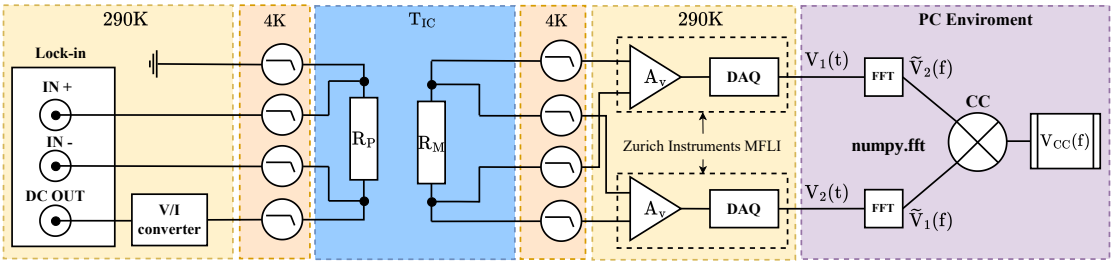

Figure 6.6: Cross-Correlation Experiment Schematic. The initial box on the left-hand side houses a *Zurich Instruments MFLI* lock-in amplifier, delivering DC voltage via the auxiliary output to a low noise voltage-current converter designed at *Lancaster University*, which operates at $1\mu\mathrm{A/V}$. This setup applies current through the power resistor R_P. The same MFLI captures the corresponding DC voltage response by demodulating at 0 Hz. All wiring is filtered at the 4 K stage using *Aivon* Low Pass Filters (LPF). The subsequent box illustrates the power resistor R_P and the measurement resistor R_M within the IC at a temperature of $\mathrm{T_{IC}}$. Finally, R_M is linked to two MFLIs that simultaneously measure the voltage across the resistor.

6.2.2 Detail of Operation and Electrical Setup

Figure 6.6 provides an illustration of the experimental electrical setup. The synchronization and triggering of the Zurich Instruments MFLI lock-ins were controlled by the Multi-Device Synchronization (MDS) package. To verify the synchronization of the traces, timestamps from each amplifier were cross-referenced, ensuring they began within 20 μs of eachother. The analog-to-digital converters (ADCs) in the amplifiers sampled data at $f_{clock}/2^9 \approx 120$ kHz, where f_{clock}, the clock frequency, is 60 MHz, and 2^{16} samples were collected. This yielded a measurement duration of 0.56 s per spectrum. After obtaining both time traces, the cross-correlation spectrum was calculated and subsequently averaged to minimize residual noise. After the spectra was generated 5 different frequency ranges were averaged to generate the temperature values. These frequency ranges were chosen so they had no external interference present (noise spikes for

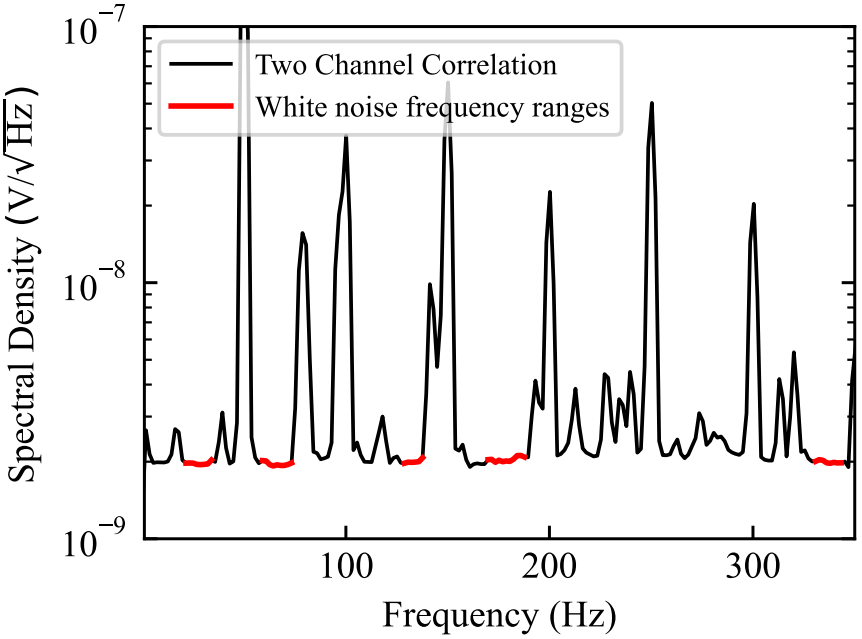

Figure 6.7: Frequency ranges used to calculate the final cross-correlation value. If the sections which include the peaks are included in the final average, the value calculated is overestimated. Working at higher frequencies would help to mitigate this issue, as common harmonics, such as mains are not present in the spectra.

example). These frequency ranges can be seen in Fig. 6.7. In our experiment, the number of averages was set to 3000 to ensure the total measurement time remained below 30 minutes. The necessary number of averages to sufficiently lower the noise floor in the measurement depends on both the noise of an individual channel amplifier and the target noise floor resolution, as indicated by Eq. 6.46. If we then want to discover the minimum possible temperature we can measure with 3000 averages and given a amplifier noise floor of $4\ \frac{nV}{\sqrt{Hz}}$ we can use Eq. 6.47. This yields a minimum measurable noise of $0.5\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$, corresponding to a minimum measurable temperature of approximately 100 mK (for $R = R_M = 45\ \mathrm{k}\Omega$). To re-enforce the importance of cross correlation, without this technique the minimum measurable noise would be that of the amplifier at low frequencies, which gives equivalent minimum temperature of ≈ 6.4 K.

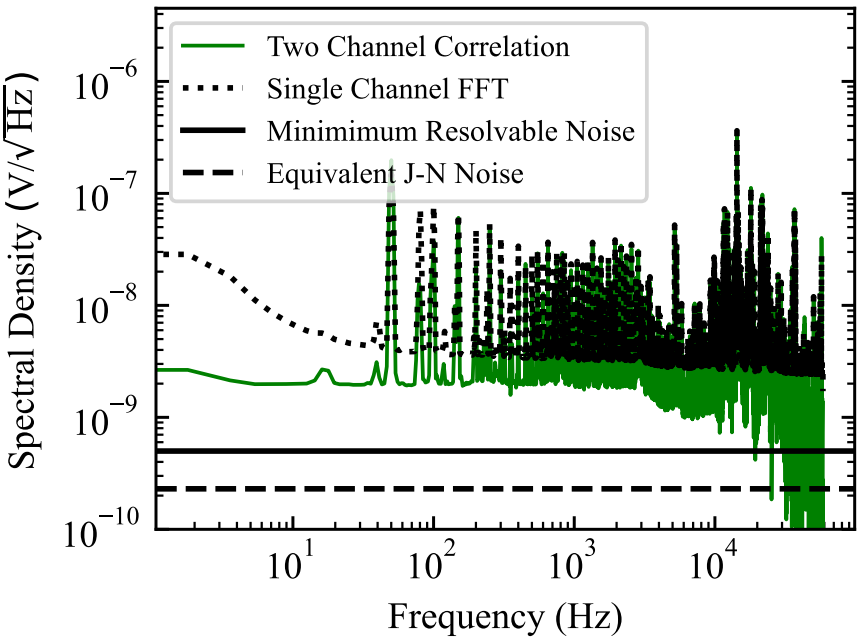

Figure 6.8: Base Temperature Measurement of R_M. After 3000 spectral averages the two channel correlation (green line) is below that of the single channel FFT. However, the two channel correlation should be much closer to the minimum resolvable noise (black line) as the thermal contribution at base (dashed line) is below the minimum resolvable noise. As such there is likely another source of noise

6.2.3 Characterisation of measurement resistor

Preliminary noise measurements at base temperature ($\mathrm{T} = 15\ \mathrm{mK}$) showed that the measurement resistor had a higher than expected noise floor as depicted in Fig. 6.8. Although this noise level is lower than that of the amplifier, it possesses an Equivalent Noise Temperature, ENT, of 1.77 K. To ensure that this observation was due to the experimental configuration, noise measurements across the resistor were also performed in an another resistor present in the setup (R = 9 kΩ) and with a dead short of the measurement resistor, the results are plotted in Fig. 6.9. As we ruled out any systematic noise offsets in our measurement chain, two options for the existence of this unexpectedly high noise level were considered.

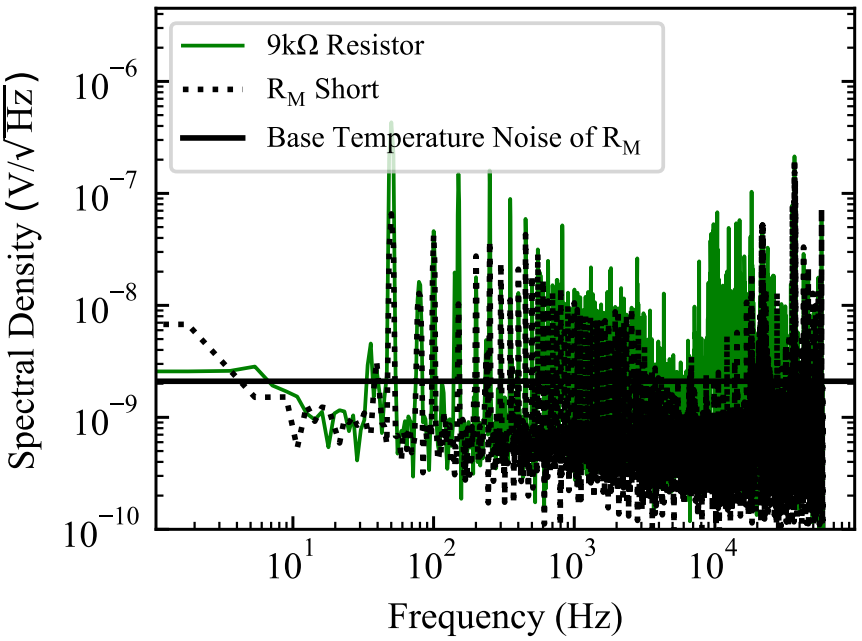

Figure 6.9: Base Temperature measurements of R_M shorted and a $9\ \mathrm{k}\Omega$ resistor. The correlation of both the shorted R_M and the $9\ \mathrm{k}\Omega$ resistor are much below the noise floor of the base temperature measurement of R_M. This would suggest the offset noise of R_M is not related to the set up.

1. R_M fails to thermalise with the MXC and instead only reaches the ENT of 1.77K at base temperature. In this case the noise would be thermal noise.

2. The noise is derived from a mix of the thermal contribution at the base temperature and a constant offset due to the resistor's properties.

To investigate if R_M had thermalised, its resistance was taken as a function of temperature, as shown in Fig. 6.10. This was determined through four-terminal lock in technique with a AC excitation of 500 pA. The absence of a resistance plateau at the ENT of 1.77 K implies the resistor did not saturate here, meaning scenario 1 was unlikely to be true. The source of the noise is difficult to pinpoint as we don't know the exact material the resistor is made of. Previous literature however, [150] has shown that non-thermal noise can be present in silicon-based

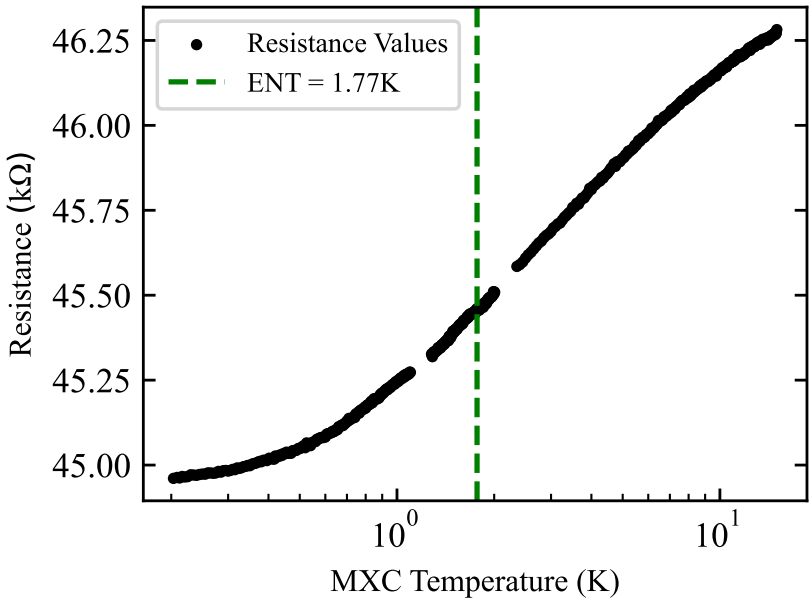

Figure 6.10: Resistance of R_M as a function of temperature. The resistance of R_M continues to change past the ENT of the base temperature noise measurement. This would suggest that R_M is still thermalised to the MXC plate and hence would rule out that the saturation in the temperature of R_M as the source of the extra noise.

resistors at low temperature. The offset noise at base temperature (denoted by $S_{Offset}(f)$) was found to be temperature independent in the region below 1.77 K, which meant we were able to treat it as a constant. To calculate this value, we took a spectral measurement of the resistor at a well defined temperature, measured the resistance and then subtracted the theoretically predicted Johnson-Nyquist value. This was conducted at a low temperature to reduce the influence of thermal noise on the noise offset value. The theoretical base temperature thermal contribution is denoted $S_{T=15mK}$. The total spectral density at base after 3000 cross correlation averages, $\langle S^2_{Base}(f)\rangle$, is given by,

$$\langle S^2_{Base}(f)\rangle = S^2_{Offset}(f) + S^2_{T=15mK}. \tag{6.48}$$

which is simply the sum of the thermal and non-thermal contributions. Following this, the non-thermal offset spectra, $S_{Offset}(f)$, can be found,

$$S^2_{Offset}(f) = \langle S^2_{Base}\rangle - S^2_{T=15mK}. \tag{6.49}$$

This offset is then removed from every averaged temperature spectral reading, $\langle \mathrm{S_{MXC=x}(f)}\rangle$, with the result $\mathrm{S_{T=x}(f)}$,

$$\langle S^2_{T=x}(f)\rangle = \langle S^2_{MXC=x}(f)\rangle - S^2_{Offset}(f). \tag{6.50}$$

Finally the temperature values are derived from this spectra by averaging in the white noise regions.

Due to the inclusion of the base offset measurement, the uncertainties in final temperature values becomes more complicated. Using the Johnson-Nyquist relationship in Eq. 2.7 the relative uncertainty in temperature, $\frac{\delta T}{T}$, is given by,

$$\frac{\delta T}{T} = \sqrt{\left(\frac{\delta S^2_D}{S^2_D}\right)^2 + \left(\frac{\delta R}{R}\right)^2}. \tag{6.51}$$

The standard error in the resistance measurements gives, δR, while R is given by the average value. For the spectral density, δS^2_D is the standard error of the values

of the white noise frequency values. Since an offset is removed at every step, this must be taken into account. Following Eq.6.49, the error in both $S^2_{T=15mK}$ and S^2_{Base} must be addressed. The only error in $S^2_{T=15mK}$ is the error of the resistance at base. The error in S^2_{Base} is given by the standard error in the frequency values used. As such the total error in the offset value is given by δS^2_{Offset},

$$\frac{\delta S^2_{Offset}}{S^2_{Offset}} = \sqrt{\left(\delta\frac{S^2_{Base}}{S^2_{Base}}\right)^2 + \left(\frac{\delta R_{T=15\ mK}}{R_{T=15\ mK}}\right)^2}. \tag{6.52}$$

The error in each temperature measurement, S^2_M, is given by

$$\frac{\delta S^2_M}{S^2_M} = \sqrt{\left(\delta\frac{S^2_{T=x}}{S^2_{T=x}}\right)^2 + \left(\frac{\delta R_{T=x}}{R_{T=x}}\right)^2}. \tag{6.53}$$

6.3 Noise Temperature vs MXC temperature

6.3.1 Results

To validate noise thermometry, we measured the resistor's noise temperature and compared it to that of the MXC thermometers. The MXC temperature was increased from 100 mK to 8 K in twelve steps. The resistance was measured at each temperature to ensure that its value was well known. At each step spectra were recorded according to Section 6.2.2 The results of this experiment are shown in Fig. 6.11. Figure 6.11 a) demonstrates that at lower temperatures, increased averaging is required to sufficiently attenuate non-correlated noise and achieve the theoretical value. The theoretical amplitude spectral density (ASD) in this plot is derived from the Johnson-Nyquist formula, using the MXC temperature and a measured resistance value of R_M. Figure 6.11 b) shows the relative error (the ratio of the standard error to the average value) is inversely proportional to the square root of the number of averages. This relationship begins to deteriorate at higher values of n, due to the inclusion of the error in the offset spectral density value, which remains constant. Figure 6.11 c) indicates that the noise temperature agrees in general with the MXC temperature. Figure 6.11 d) illustrates that the relative

error in temperature is inversely proportional to the temperature, assuming that the Johnson-Nyquist ASD target noise is significantly lower than the ASD of the amplifier channel input. At elevated temperatures, this relationship deteriorates. Further details on the agreement with the MXC temperature is provided in Fig. 6.12. Although the noise temperature generally aligns with the MXC temperature, it is only beyond 200 mK that the measured values begin to fall within 10% of the MXC temperature. One way to reduce the overall uncertainty is by employing a resistor without a noise offset as this adds a constant value at every temperature step. Moreover, due to the noise offset, this approach can no longer be considered primary thermometry. This relies on the belief that the R_M thermalises at the base temperature of 15 mK, which cannot be confirmed with absolute certainty. However, at temperatures above 2 K, the total value of the Johnson-Nquist noise at 15 mK assumption accounts for less than $1\ \%$ of the overall value, meaning at higher temperatures the exact base temperature value has an increasingly minimal effect on the extracted temperature.

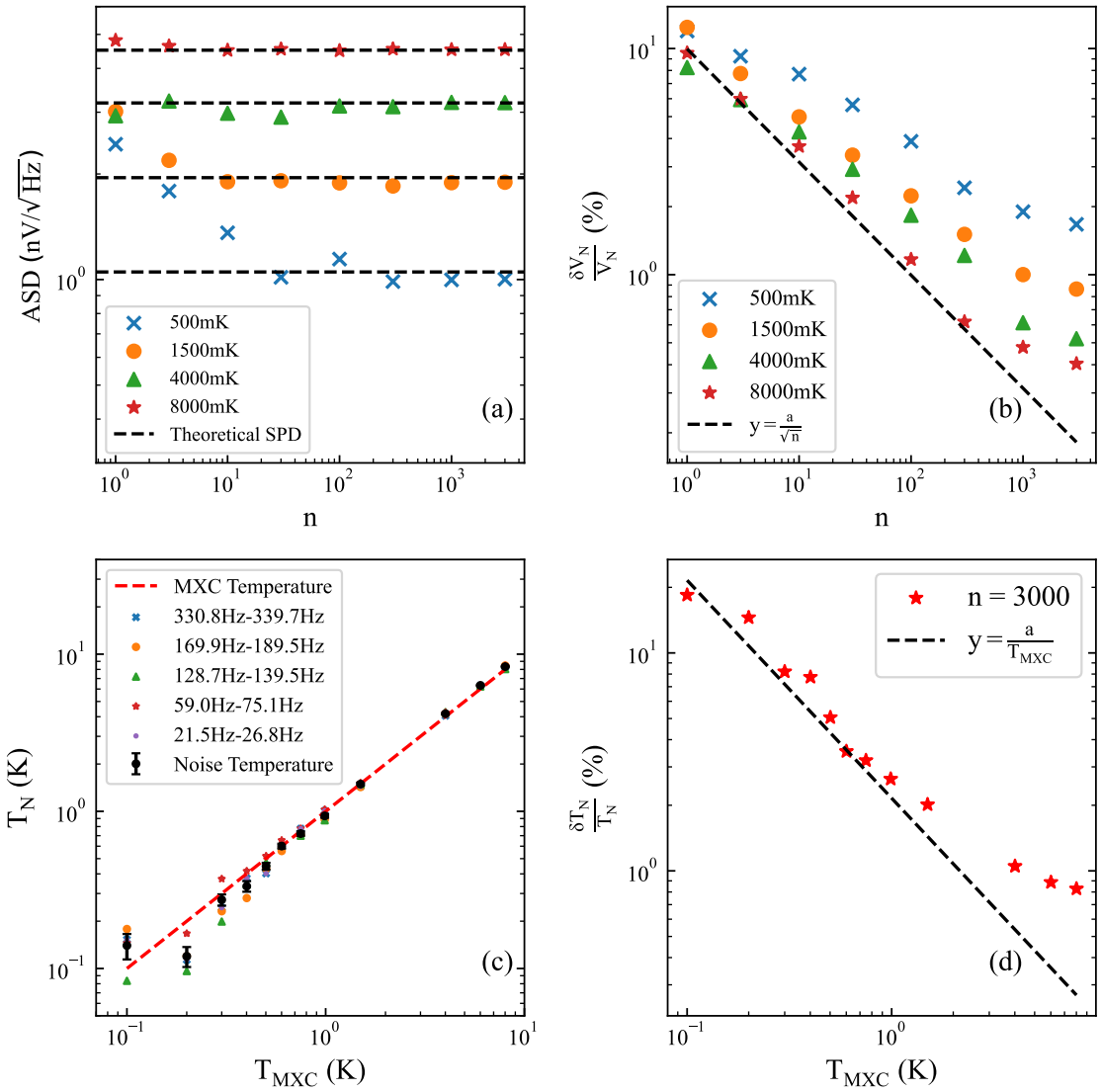

Figure 6.11: a) Amplitude Spectral Density (ASD) as a function of the number of averages for various temperatures. b) Relative error in voltage measurement as a function of the number of averages for different temperatures. c) Noise temperature versus MXC temperature. A linear fit of $T_N = \alpha T_{MXC} + \beta$ gives $\alpha = 1.053 \pm 0.005$ and $\beta = -5.8\,\mathrm{mK} \pm 1.7\,\mathrm{mK}$. The strong linear fit suggests the noise thermometer is well thermalised to the MXC. The negative y intercept indicates the noise thermometer being slightly undervalued. d) Relative error in temperature versus MXC temperature.

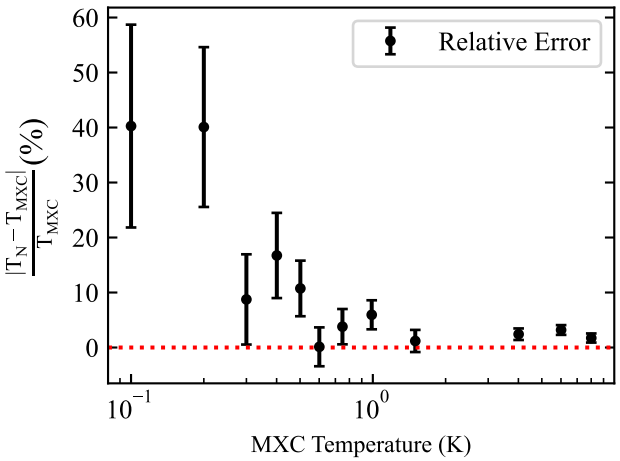

Figure 6.12: Relative error of the noise thermometry against the mixing chamber. After 300 mK the relative error is within two uncertainty values of the MXC temperature.

6.3.2 Discussion

The main drawback of this approach is that the relative uncertainty is inversely related to the square root of the number of averages and inversely related to the resistor's temperature, meaning at lower temperatures it will take longer to achieve the same uncertainties. For example, using 3000 averages (or 28 minutes), if we aim for a relative uncertainty below 2%, the highest measurable temperature is around 1.5 K. On the other hand, constraining the measurement time to 1 minute for faster measurements, means only 100 averages. In this context, to maintain a relative uncertainty of 2%, restricts the measurement to temperatures of 8 K or higher. Consequently, the primary constraint of this technique is the extended duration required for averaging to measure lower temperatures and reduced relative uncertainties. The main solutions to this problem can be summarised as:

1. Lower the input noise of the amplifiers.

2. Increase the measurement bandwidth.

3. Increase the effective number of averages taken.

One such alternative set up would be the use of cryogenic amplifiers. These come in many forms and include but are not limited to SQUID based pre-amps [151], HEMT based LNAs [152], GaAs based pre-amps [153] and SiGE based pre-amps [154]. The lower noise floor of the amplifiers would help first reduce the uncertainty, as shown in Eq. 6.43. Secondly, having cryo-amps would help negate the impact of the parasitic wire capacitance, which currently throttles the bandwidth of the measurement due to its 1/RC behaviour, by reducing the output impedance and providing gain to the output signal. In a suitable high-frequency setup, this would greatly increase the measurement bandwidth. Having a higher measurement bandwidth reduces the time per spectral and means more averages can be taken, both further reducing uncertainties (as per the Rice relation, Eq. 6.44) or lower the temperature possible to measure (as per Eq.6.47). Operating at a higher bandwidth away from the noisy DC areas of the frequency spectra should also help the overall accuracy of the experiment. Finally, we can increase the effective number of averages taken by employing a signal processing technique, frequency averaging, which is dealt with in the next section.

6.4 Frequency Averaging

The method used in this thesis to average cross-correlation spectra is time averaging. By this, we mean that we create an average spectra, $\langle S_{CC}(f)\rangle$ by averaging n different spectra,

$$\langle S_{CC}(f)\rangle = \frac{1}{n}\sum_{i=1}^{i=n} S_{CC-i}(f). \tag{6.54}$$

Once we have this spectra we then take its real part, and choose some frequency range $f_1 - f_2$ with m frequency points that we consider free of interference and average over this frequency range and convert to a single value to convert to a temperature, $\langle S_{CC}\rangle$,

$$\langle S_{CC}\rangle = \frac{1}{m}\sum_{i=f_1}^{i=f_2} \mathrm{Corr}\left[\langle S_{CC}(f_i)\rangle\right], \tag{6.55}$$

Where the Corr[] operator takes the magnitude of spectra to remove any complex components and also scales this to remove factors created by windowing the data. In this case, the total number averages performed $N_{avg} = n+m$, that is n . One such alternative to this way of averaging is frequency averaging. For an ideal thermal noise spectrum, S, which is white and Gaussian, the following is true,

$$\frac{1}{n}\sum_{i=1}^{i=n} S_i(f_0) \equiv \frac{1}{n}\sum_{i=f_1}^{i=f_2} S(f_i), \tag{6.56}$$

where S_i is the i'th independently measured spectra, f_0 is an arbitrary frequency, n is large and there are n frequency points between f_1 and f_2. This is because each value in all the spectra is statistically independent and as such all the values in all the spectra can be interchanged. Using Eq.6.56, we can increase the number of vector averages taken, keep the number of independent spectra taken the same, and converge the cross-correlation much faster [155]. This alternative method is the following,

$$\langle S_{CC} \rangle = \text{Corr}\left[\frac{1}{mn}\sum_{i=1}^{i=n}\sum_{j=f_1}^{j=f_2} S_{CC-i}(f_j)\right]. \tag{6.57}$$

Using this method, the number of averages is $N_{avg} = nm$. One of the drawbacks of this technique is that it does not resolve a full spectrum, and as such it cannot be a primary form of thermometry. Figure 6.13 visually describes this. As such, this technique may be suited to speed up repeated temperature measurements in a range in which the frequency response is already well defined. Figure 6.14 gives an example of this technique on low resistance resistors at room temperature.

6.4.1 Potential Utility of Frequency Averaging

One point of note is that for the three lowest resistance values tested here, the spread of the rolling average is high, and as such the uncertainty in the final value is high. This affects the utility of this technique. The main reason behind this is that many of the averages are 'used' converging the cross-correlation, rather than reducing the uncertainty. As such, if the averages after the convergence n

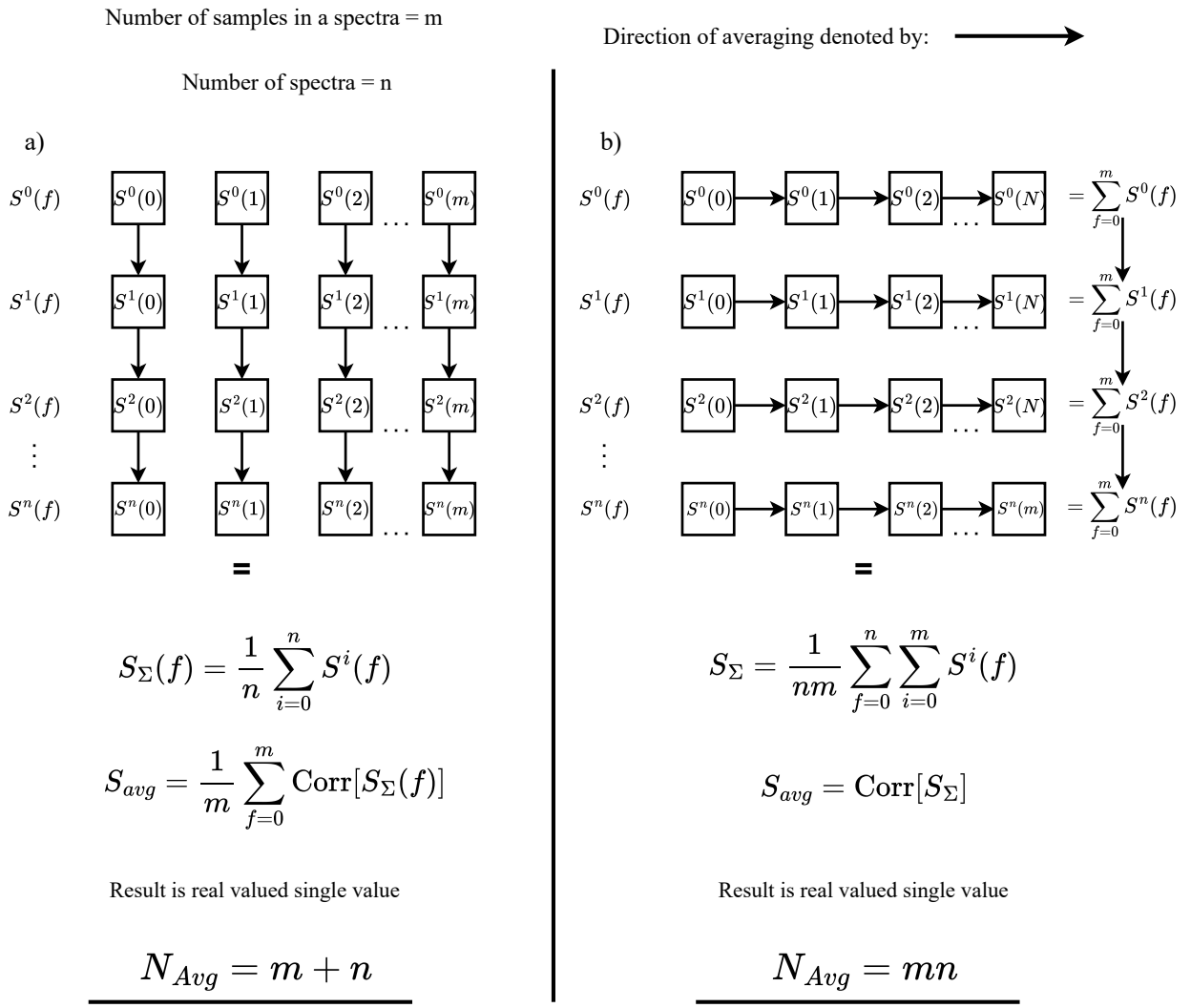

Figure 6.13: Illustration of the frequency averaging process. a) Is the 'normal' manner of averaging, which results in the total number of averages (N_{Avg}) which will determine the final standard deviation in the value, being the number of spectra taken (n), plus the number of values in a spectra m, $N_{Avg} = n + m$. The reason the number of averages adds instead of multiplies is after the Corr[] operator has been applied the correlation process stops, as you are no longer averaging vector values. As such, you average a total of n times during the averaging prior to the Corr[] operator and then finally another m times when generating a final value from a real valued spectra. b) Represents frequency averaging, where the total number of averages taken is equal to the product of the spectra taken and the number of values in the spectra taken to further average, $N_{Avg} = nm$. The product of n and m is used here as the Corr[] operator is used only at the final stage, so prior to this the averaging of vector values is taking place, and nm is the total number of points available to average. This increased number of total averages is used to accelerate the cross-correlation convergence.

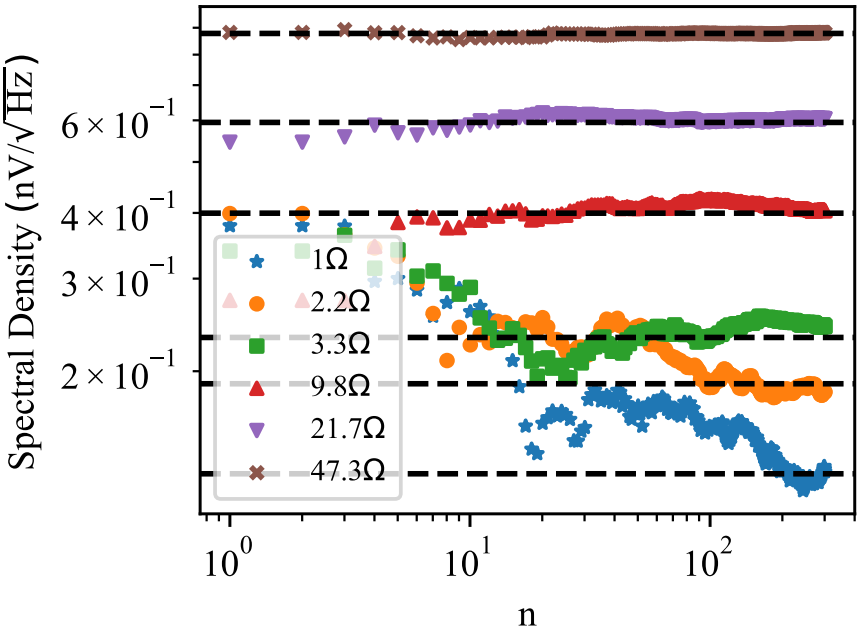

Figure 6.14: Rolling average spectral density against the number of spectra takenat room temperature. Dashed lines here are the Johnson-Nyquist predicted spectral densities at 295 K. Here the sampling rate was $f_{clock}/2^7$ and the number of samples taken is 2^{19}, which gives a time per spectra of 1.13 s. The resistors used are standard laboratory thin film carbon resistors. The frequency range which is averaged over is selected after taking 300 averages and viewing the whole spectra to ensure the noise is white within this frequency range. In descending order of resistances, the frequency ranges used are: 110-114 kHz, 110-114 kHz, 183-187 kHz, 105-110 kHz, 105-110 kHz, 121-125 kHz. In the case of the 1Ω, 5000 points were averaged in the frequency range 121-125 kHz, as this process was then repeated 300 times to give a total of 1,500,000 effective averages.

are high and as the uncertainty drops with $1/\sqrt{n}$, the subsequent averages reduce the uncertainty very slowly. Figures 6.15 and 6.16 demonstrate a simulation of the frequency averaging of a 3 Ω resistor and a 47.3 Ω resistor, with the same conditions (temperature, bandwidth, number of averages and amplifier input noise of the experiment) as in the experiment. The 47.3 Ω resistor, which has an extremely small theoretical number of averages required to converge, 34, quickly reduces its uncertainty to less than 1%. While the 3 Ω resistor takes around 7000 averages to converge, the uncertainty remains high. This could be partially mitigated by massively increasing the number of averages, but the dependence $1/\sqrt{n}$ on uncertainty will mean that this will have a limited effect. This highlights the fact that frequency averaging can be used most effectively to reduce the uncertainty of a measurement when the number of averages needed for convergence is low.

We can explore the effect of massively increasing the number of effective averages by applying frequency averaging to examples in the literature. Crossno *et al.* [46] demonstrated high-frequency analog cross-correlation noise thermometry at a frequency of 1 GHz in a bandwidth of 328 MHz, and achieved a benchmark uncertainty of 0.01% in a $50\ \Omega$ resistor at 50 K. During this work they produced a plot of their uncertainty in the noise value (calculated from 1000 averages) as a function of the integration time of their system. Using Eq. 6.43 we can check our theoretical understanding agrees with their measured results for their non-frequency averaging work first. In the setup, the amplifier used is 50 Ω matched LNA, the Caltech CITLF3, with a noise temperature, T_N, of 46 K in the frequency range of interest. Using the Johnson-Nyquist formula, this gives an amplifier spectral density of 0.354 $nV/\sqrt{Hz}$. In terms of load noise, this is simply the Johnson-Nyquist noise of a 50 Ω resistor at 50 K, 0.371 $nV/\sqrt{Hz}$. If we enter these values into 6.43 and convert n to integration time with Eq. 6.45 then we can plot the predicted uncertainty with the acquired data. This is plotted in Figure 6.17

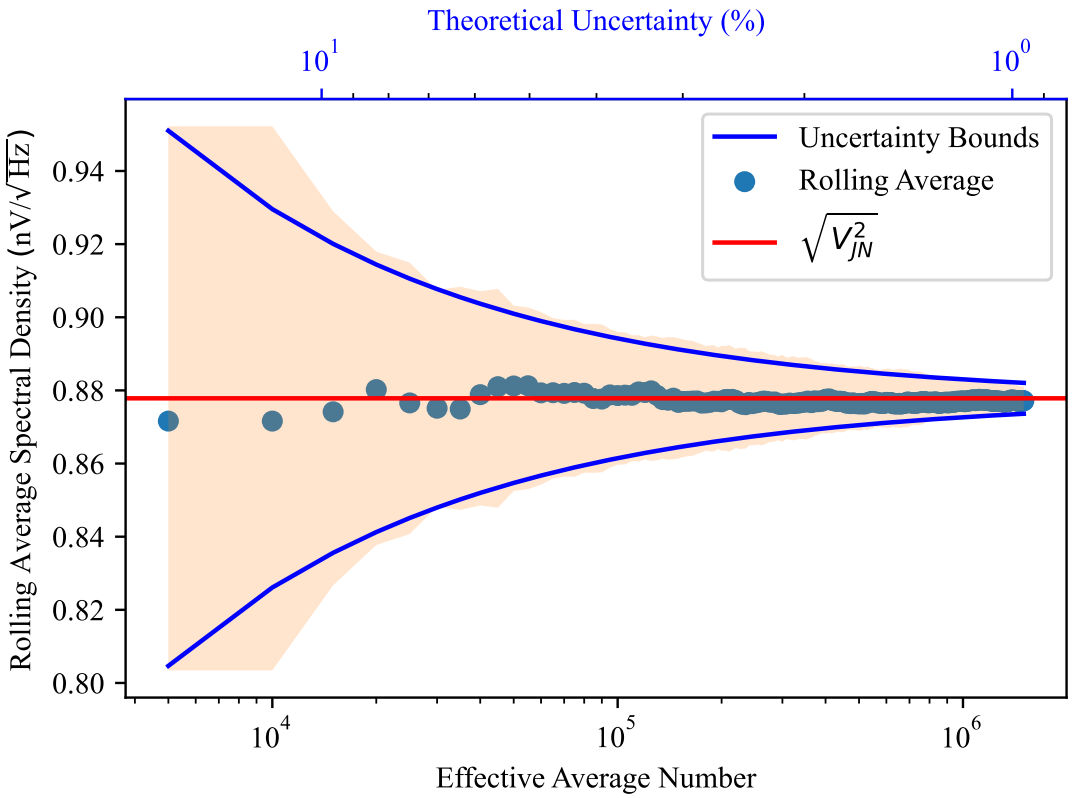

Figure 6.15: Simulation of the frequency averaging of 47.3 Ω resistor. Here the beige color is the calculated standard deviation of 30 repeats of the same experiment plus/minus the average value at a given rolling average number. The effective number of averages is the product of the real average number and the number of points averaged. Here 300 real averages are taken. The theoretical uncertainty bounds are calculated from Eq. 6.43.

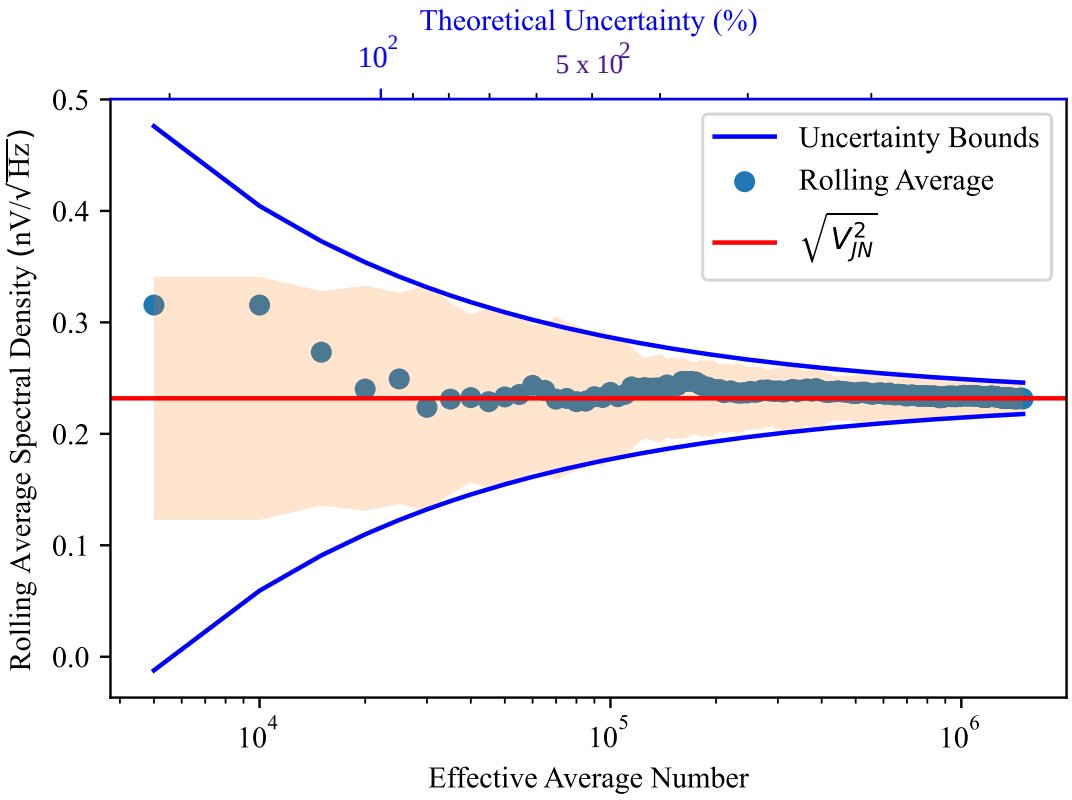

Figure 6.16: Simulation of the frequency averaging of a 3 Ω resistor. The beige color is the calculated standard deviation of 30 repeats of the same experiment plus/minus the average value at a given rolling average number. The effective number of averages is the product of the real average number and the number of points averaged. Here 300 real averages are taken. The theoretical uncertainty bounds are calculated from Eq. 6.43.

a). If frequency averaging with digital electronics were to be employed during this same setup, the decrease in uncertainty would be large in comparison to the normal averaging technique, primarily due to the number of samples collected.

To estimate the possible decrease in uncertainties in an experiment like this, we must first make some assumptions about the equipment needed to run the experiment. To use concrete numbers, we can take the example of using the Zurich Instruments GHFLI as the room temperature ADC, which has a scope sample rate of 4 G Sa/s and a scope memory of 524,288 samples. Firstly we can define our sample rate, $f_{sample} = 4\,\mathrm{GSa/s}$, which will give a total 2 GHz bandwidth, which amply allows the averaging to take place in a 328 Mz range at 1 GHz as in Crossno *et al*. Secondly, we can define N, the number of points per spectra as $N = 524,288$. The total number of points per spectra in the measurement bandwidth of interest, N_{BW}, can be given as

$$N_{BW} = \frac{N}{2}\frac{\Delta f}{f_{sample}} \tag{6.58}$$

where Δf is 328 MHz. Here N is initially divided by two, as half of the returned spectra will be negative frequencies, and in our analysis we only use the positive frequencies. The time per spectra, $\tau_{spectra}$ will be given by,

$$\tau_{spectra} = N/f_{sample}. \tag{6.59}$$

Finally, the total number of points collected in the frequency range of interest in an integration time τ_{Int} is given by,

$$N_{Tot} = \frac{\tau_{Int}}{\tau_{spectra}} N_{BW} = \tau_{Int}\frac{\Delta f}{2}. \tag{6.60}$$

We can now use this expression to examine the impact of frequency averaging upon the uncertainty, by substituting this value into Eq. 6.43 the results are plotted in Fig. 6.17 b). This could be further improved by using the Caltech CITLF3 at cryogenic temperatures, further reducing the noise temperature of the amplifier to between 2.5 K and 4 K [156]. With an amplifier temperature of 4 K it would

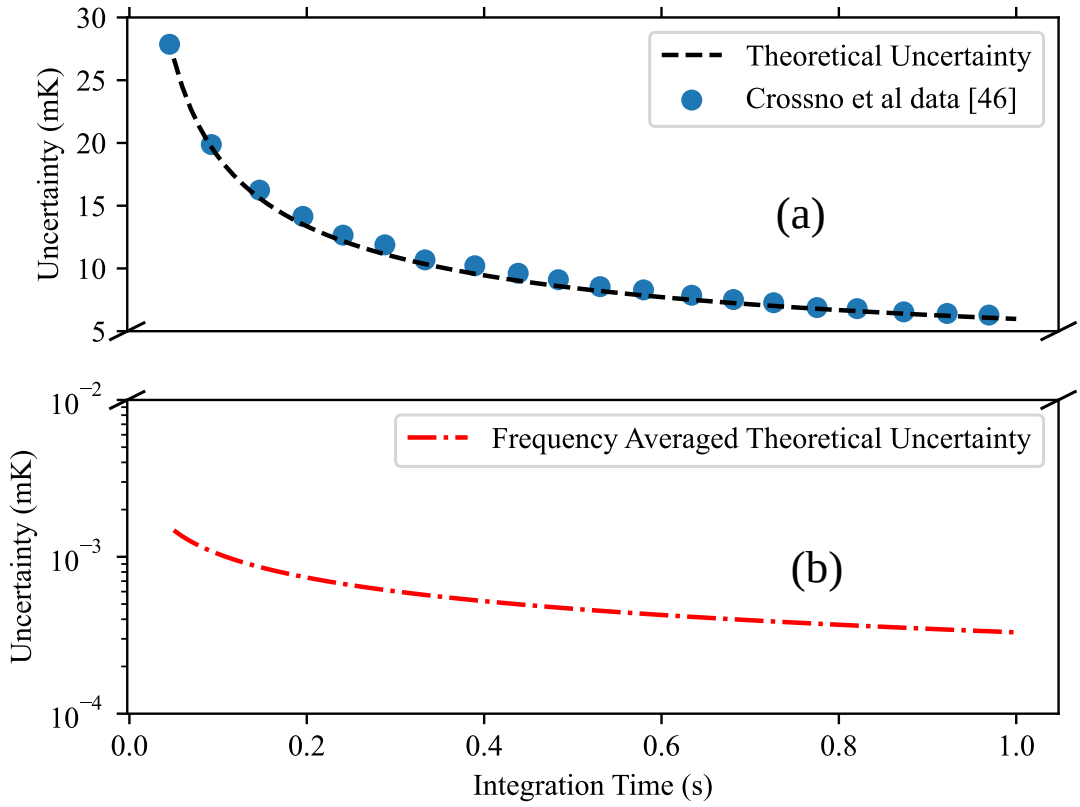

Figure 6.17: (a) Uncertainty in Crossno *et al* analog, cross-correlated noise measurement of a 50Ω resistor at 50 K in a 328 MHz bandwidth: Here the blue dots are data extracted from Crossno *et al* and the dotted line is the theoretical prediction give by Eq. 6.43. (b) Uncertainty in Crossno *et al* cross-correlated noise measurement of a 50Ω resistor at 50 K in a 328 MHz bandwidth if the cross-correlation had been taken digitally, and frequency averaging had been used, also based upon Eq. 6.43. The result is a drastic decrease in the uncertainty values.

be possible to measure the same 50Ω resistor at 100 mK to within $1\mu K$ theoretical uncertainty within an integration time of 1 s, given all the previous assumptions.

The caveat with extremely low uncertainty values is that they will eventually be limited by the crosstalk between the two amplification channels performing the cross-correlation. As such, while using frequency averaging can have a large impact on reducing uncertainties, ultimately the final uncertainty is likely to be bounded by the crosstalk.

6.5 Noise temperature vs power dissipation

To confirm the accuracy of noise thermometry, we performed *in-situ* tests where we supplied power within the IC and monitored the temperature. This validation is crucial because placing a power-dissipating element near R_M can result in cross-talk, which may lead to erroneous noise measurement results. We used an alternative in-IC method to compare with noise thermometry, specifically monitoring the resistance of R_M as a function of temperature. The temperature dependence characterised in Fig. 6.10 was used as calibration reference against the MXC. We first tested resistance thermometry in relation to power dissipation ranging from 600 nW to $100\ \mu\mathrm{W}$. Resistance measurements were taken at linearly spaced intervals and converted into temperature by the calibration. To evaluate noise thermometry against resistance thermometry, power was applied at seven different levels within the 600 nW to $100\ \mu\mathrm{W}$ range and spectra were documented. Moreover, a control spectra was recorded with the power resistor attached but not dissipating power, enabling re-calibration of the offset spectral density. This was necessary to mitigate any potential cross-talk from the power resistor that could come from the current source. The findings from both resistance thermometry and noise thermometry are presented in Fig. 6.18. Both sets of data display reasonable consistency with each other, indicating the utility of noise thermometry at these temperatures. The results suggest that this approach might be appropriate for use in integrated circuits with multiple power dissipating components at cryogenic temperatures.

6.6 Conclusion

We have established that noise thermometry is in good agreement with the MXC temperature range from 300 mK to 8 K. Furthermore, it shows substantial agreement with an independent thermometry technique when used to determine the IC temperature corresponding to a specific power dissipation. This form of

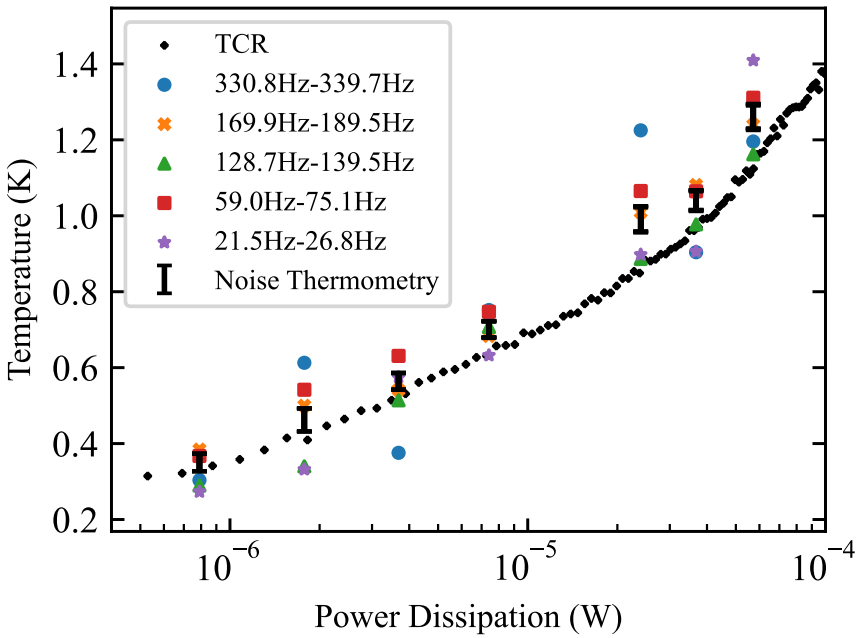

Figure 6.18: Temperature Coefficent of Resistance Thermometry (TCR) and Noise Thermometry as a Function of Power.

thermometry was made to be effective by the use of both cross-correlation and subtraction of the offset noise calculated from base temperature measurements. This work suggests that with the addition of these techniques, voltage noise thermometry could be broadly applicable to ICs developed with industrial CMOS processes. However, the offset noise does preclude the noise thermometry in this paper from being a primary method of thermometry. Employing a resistor devoid of additional noise would reduce the measurement uncertainties and retain the technique as a primary thermometry method. Although this work demonstrates the increase in the uncertainty of measurements at lower temperatures and the large measurement time, we describe how the use of cryo-amps could rectify both of these issues. We also describe frequency averaging, a technique that could be used to decrease the uncertainty of noise thermometry by massively increasing the number of effective averages taken. We discuss its drawbacks, such as its non-primary nature as and also use simulations to determine when it is most useful.

As the direction of quantum computing moves towards temperatures closer to 1 K to access higher cooling power, this method will require less averaging to attenuate uncorrelated noise. This will mean faster measurements and lower uncertainties. In addition, the implementation of this technique is straightforward and requires only standard instruments that are typically available in academic or commercial laboratories. Given that the devices used are only resistors, this method significantly reduces the time and resources required for the design of ICs, facilitating the placement of thermometers at multiple locations within an IC. Finally, we suggest that this technique is an excellent candidate for performing in-IC temperature measurements to map the thermal profile of operational quantum-classical circuitry because of its dual primary and dissipationless nature.

Chapter 7

Summary and Outlook

This thesis describes a suite of thermal management techniques for low temperature electronics. It has focused on two key areas of thermal management, reduction in the power consumption of the electronics, and control of the subsequent heat flow in the cryogenic environment.

For the first of these two areas, this work demonstrated practical techniques for the optimisation of differential amplifier performance as well the creation of low-threshold FETs at low temperatures through the concept of cryogenic threshold engineering. Experiments with differential amplifiers made from commercially available FETs show that *in-situ* testing of passive components such as resistors, with a potentiometer outside the cryostat, can help reduce the time required to optimise amplifier performance. It is also shown that the presence of freezeout related effects (such as the kink effect) and other thermal effects (the different threshold changes in n and p type transistors) contributes to the reduction in performance of the amplifiers. As for the concept of cryogenic threshold engineering, it was shown that by using FETs with the appropriate room temperature threshold (in our case -0.4 V at room temperature and -4.8 mV at 1 K), you can negate the impact of the increase in threshold voltage at low temperatures and make more efficient devices. This was demonstrated in a simple

common source amplifier, designed to correlate any increase in efficiency with changes in the threshold. This common source amplifier showed an increase in efficiency (bench marked by a FOM) of approximately an order of magnitude from 290 K to 4 K, which agreed with both analysis and simulations.

The ability to have low threshold bulk FETs at cryogenic temperatures, may open up the possibility of extremely low power supply electronics in bulk technologies, and give a viable alternative to backgated technologies such as FD-SOI. As such cryogenic threshold engineering may open up other alternative paths to low voltage supply, low power cryogenic electronics.

Thinking towards the future, tweaking FET designs in smaller nodes (which are known to be more resistant to freezeout effects) to negatively offset the threshold at room temperature could be a route forward for cryogenic threshold engineering. The eventual goal of which should be to create a CULVT (Cryogenic Ultra Low Voltage Threshold) device, which should be the cryogenic equivalent of a room temperature ULVT (Ultra Low Voltage Threshold) device, but retains all of the benefits of cryogenic operation, i.e. low leakage and increased drive currents. A decreased subthreshold swing would allow power savings in both dynamic and static power dissipation.

The second major area of this work, thermal management, is again split into two main sections, the management of thermal flows by material choice and geometry, and the delicate task of determining the temperature inside an IC. The main motivation for this part is that helping to understand thermal flows in and around power dissipating ICs at low temperatures can help to integrate the quantum and classical parts of a quantum computer.

Firstly, the management of thermal flows was demonstrated by tracking the

temperature of each of the components of a typical quantum computing setup as a function of the power dissipated in an IC. This includes the temperature of the silicon interposer, copper mount, PCB and IC as a function of power from 10 nW to 100μW in both zero field and 100 mT conditions. Qualitatively, this data reinforced several important points. The first being the importance of the metal-metal connection of the copper mount to the refrigerator cold plate. At millikelivin temperatures the impact of surface asperities and thermal boundary resistance means that even metal-metal boundaries can add large thermal impedance if not enough force is applied at the boundary. The second is that the silicon interposer maintains the highest temperature over all power dissipations, due to silicon's poor thermal conductivity and the large boundary resistance associated with insulator-metals at low temperatures. This puts into question the feasibility of using silicon interposers for scaling up quantum computers without serious thermal mitigation. Finally, PCB temperature tracks the copper holder temperature, so is well thermalised by strong mechanical connections to its ground planes. This is important as additional low pass filters are placed on and thermalised by the PCB. Quantitatively, these data were then used to form the basis of COMSOL thermal simulations carried out by researchers at Forschungszentrum Jülich, which allowed the spatial distribution of the temperature to be resolved. During this experiment, the temperature of a separate thermometer (designed to mimic a qubit connected to hot electronics) only connected to the IC via superconducting aluminium bonds and well thermalised to the cold plate by an annealed silver strip was measured. It was found that the thermometer was 30 mK cooler in the non-field case, which demonstrates that the superconducting nature of the bonds, helps shield the thermometer from the hot IC. The temperatures of the field on and field off cases converged at a power consumption that equated to approximately 0.9 K, which is close to the wirebonds predicted T_C of 1.2 K [157]. This suggests this technique could be improved by using superconducting bonds with a higher T_C such as niobium.

Looking forward, lessons learned in this section can be applied to the scaling of quantum computers for thermal management purposes. A push-pull technique can be applied to keep thermally sensitive devices such as qubits cold, while keeping them connected to the hot electronics needed to manipulate and read them out. The push here refers to pushing the power dissipated in the hot electronics, down other thermal paths than the wires that connect them to the hot electronics. In the short to medium term this ideally would be performed with high T_C wire bonds. In the long term this role may be played by superconducting TSVs. The pull approach refers to pulling the qubit device as close as possible to the cold plate temperature, by providing a low impedance thermal path to the MXC. In our setup this was achieved with the annealed silver. In more scalable environments, this will likely require potting the chips in an insulating material with high thermal conductivity at low temperatures.

As for the second part of the thermal management, this thesis demonstrates voltage noise thermometry in an IC developed in a 65 nm process in the range 300 mK to 8 K. At 500 mK the relative error in our measurements was less than 5%, and at temperatures higher than 3 K this reduces to less than 1%. The low temperatures reached were due to the use of cross-correlation to allow noise below the input noise of the amplifiers to be measured. This work also offers a detailed theoretical background on cross-correlation. This includes a derivation of the relative error in a cross-correlation measurement as a function of the number of averages, the spectral density of the DUT and the amplifier input noise, which, to the author's knowledge, is not explicitly laid out elsewhere in the literature. A technique for accelerating cross-correlation, frequency averaging, is also laid out, demonstrated, simulated, and has potential applications to fast thermometry discussed.

In the future, if cryogenic amplifiers and an appropriate 50 Ω matching circuit on PCB, could be added, then the reduction in amplifier noise and bandwidth increases would drastically lower the number of averages required to converge the cross-correlation. This could result in noise thermometry on the 100s of MHz to GHz scale. In combination with frequency averaging, this could provide exceptionally small uncertainties. This would allow for unparalleled sensing of the heating on the chip because of its primary and dissipationless nature.

Appendix A

Thermal Conductivity of Insulators at Low Temperatures

A.1 Thermal Conductivity of Insulators

Electrical insulators are commonly found in cryogenic set ups in items like PCB boards and as such its important to understand their thermal conducitvities in the limit that $T \rightarrow 0$. Electrical insulators such as plastics also can be used to provide good thermal isolation [26] as well as well as provide strength at cryogenic temperatures, this has lead some plastics to be used to connect the cold plates of modern dilution fridges. The thermal conductivity of electrical insulators is dominated by the interaction of its phonon population. This is primarily because there is no electron contribution as a result of the electrons being trapped in strong valence bonds within the atoms. In order to consider the conductivity of insulators at low temperatures, we will start from the assumption that our insulator can be modelled as a box with a gas of phonons inside of it. From the kinetic theory of gases this can be given as,

$$\kappa = \frac{1}{3} C \bar{v} l \tag{A.1}$$

where C is the specific heat per unit volume, $\bar{v}$ is the average velocity of the phonons and l is the mean free path of the phonons. In this analysis we will consider average phonon velocity as constant and not dependent on temperature. To use Eq. A.1 we must first consider the specific heat of phonons at cryogenic temperatures; for this, we will use the Debeye model. We first start with phonons; the quantum mechanical nature of phonons means that for any given mode of lattice vibration at some frequency, ω, the energy levels it occupies are discreet. That is, for the n-th energy level, the energy of vibration E is given by,

$$E_n = \left(n + \frac{1}{2}\right)\hbar\omega \tag{A.2}$$

where n is limited to integer values. To move closer to the thermal conductivity, we must also give an expression for the specific heat of the solid, this is given as the derivative of the internal energy, U with respect to temperature T at a constant volume V,

$$C_V = \left(\frac{\partial U}{\partial T}\right)_V. \tag{A.3}$$

In general, the internal energy of the system can be given by the sum of the energy of all its modes $(\text{with wave number } \mathrm{k})$ and polarisations p,

$$U = \sum_k \sum_p \left(\langle n_{k,p}\rangle + \frac{1}{2}\right)\hbar\omega_{k,p}, \tag{A.4}$$

where $\langle \mathrm{n_{k,p}} \rangle$ is the occupation of mode given by the Bose-Einstein distribution,

$$\langle n_{k,p}\rangle = \frac{1}{\exp\left(\frac{\hbar\omega_{k,p}}{k_B T} - 1\right)}. \tag{A.5}$$

Debeye's mdoel states that all of the vibrational modes in a system can be described by a linear dispersion relationship, $\omega = vk$, where v is the wave speed and k is the wave number. This model also states that there are only modes up to a frequency, ω_D, called the Debeye frequency. Hence, the sum of the modes up to Debeye frequency will equal the total number of modes. To properly account for the number of modes in the system, we should consider the density of states with

respect to the frequency of the modes, $D(\omega)$. In 3 dimensions this is given by

$$D\left(\omega\right) = \frac{3L^3k^2}{2\pi}\frac{\partial k}{\partial \omega}. \tag{A.6}$$

For a monotomic cubic lattice, inside a cube with volume L^3. The factor of 3 here is given to account for the fact for we have 3N modes for N atoms in a system to account for kinetic and potential degrees of freedom. From Eq. A.6 we can insert a value for the partial derivative and for k,

$$D(\omega) = \frac{3L^3\omega^2}{2\pi^2 v^3} \tag{A.7}$$

The integral of Eq. A.7 up to the Debeye frequency will give us the total density of modes, which will be given by $3N_d$, where N_d is the density of atoms in the system.

$$\int_0^{\omega_D} D(\omega)d\omega = \frac{L^3\omega_D^3}{2\pi^2 v^3} = 3N_d. \tag{A.8}$$

This expression can now be used to extract the Debeye frequency, ω_D. Next, by inspection using Eq. A.8 or by substitution we can now re-write $D(\omega)$ as a function of the ω_D,

$$D(\omega) = \frac{9N_d\omega^2}{\omega_D^3}. \tag{A.9}$$

Now we have a density of states as a function of ω, we can begin to compute the internal energy of the system, U. Equation B.3 gives the internal energy as the sum of the energy of each mode. This summation can be replaced by an integral of the product of $D(\omega)$ and the energy per state from 0 to ω_D, as by Debeye's definition this will contain all the states. This can be represented by

$$U = \int_0^{\omega_D} \left(\langle n\rangle + \frac{1}{2}\right)\hbar\omega D(\omega)d\omega. \tag{A.10}$$

Now, if we sub in Eq. A.9 as well as Eq. A.5 we arrive at,

$$U = \frac{9N_d}{\omega_D^3}\int_0^{\omega_D}\left(\frac{\hbar\omega}{2} + \frac{\hbar\omega}{\exp\left(\frac{\hbar\omega}{k_BT}\right) - 1}\right)\omega^2 d\omega, \tag{A.11}$$

which expands more fully into,

$$U = \frac{9N_d\hbar\omega_D}{8} + \frac{9N_d\hbar}{\omega_D^3}\int_0^{\omega_D}\left(\frac{\omega^3}{\exp\left(\frac{\hbar\omega}{k_BT}\right)-1}\right)d\omega. \tag{A.12}$$

Next, converting the internal energy to specific heat, by taking its derivative with respect to temperature at a constant volume, we arrive at

$$C_V = \left(\frac{\partial U}{\partial T}\right)_V = 9Nk_B\left(\frac{T}{\theta_D}\right)^3\int_0^{\theta_D/T}\frac{y^4\exp(y)}{(\exp(y)-1)^2}dy \tag{A.13}$$

where, θ_D is the Debeye temperature and is given by the relation $k_B\theta_D = \hbar\omega_D$. This integral has also been parameterised by $y = \frac{\hbar\omega}{k_BT}$. In the low temperature limit, $\theta_D/T \to \infty$, so we can now replace the integral with,

$$C_V = 9Nk_B\left(\frac{T}{\theta_D}\right)^3\int_0^{\infty}\frac{y^4\exp(y)}{(\exp(y)-1)^2}dy \tag{A.14}$$

in this limit the integral can be solved explicitly to give,

$$C_V = 9Nk_B\left(\frac{T}{\theta_D}\right)^3\left(\frac{4\pi^4}{15}\right). \tag{A.15}$$

Using the initial kinetic theory of gases model in Eq. A.1, we can see $\kappa \propto T^3$ in the low temperature regime, provided the mean free path,l, is temperature independent. This is true in the derivation we have just followed, i.e. in a crystalline insulator.

Appendix B

Thermal Conductivity of Metals at Low Temperatures

B.1 Thermal Conductivity of Metals at Low Temperatures

In considering the temperature dependence of metals at low temperatures, we start by supposing that the electrons can be modelled by a degenerate Fermi gas, and that this is the primary method through which conduction takes place. The starting place for this is the 3D electron density of states, $D(E)$ as a function of energy E, given by [109],

$$D(E) = \frac{(2m)^{\frac{3}{2}}\sqrt{E}}{2\pi^2\hbar^3}, \tag{B.1}$$

where m is the electron mass. This expression is derived from the solution of Schrodinger's equation for the electron gas in a box using period boundary conditions. The energy, E, in this equation is given in the Fermi-Dirac distribution,

$$f(E,T) = \frac{1}{\exp\left(\frac{(E-\mu)}{k_B T}\right) + 1} \tag{B.2}$$

where μ is the chemical potential and k_B is the Boltzmann constant. We can use both equations to calculate the internal energy of the system. The internal energy

per unit volume (u) is the product of the density of states, the occupation of the states (calculated by the Fermi-Dirac distribution), and the energy of the system. This is given formally by,

$$u = \int_0^\infty D(E) f(E,T) E dE. \tag{B.3}$$

which in the low temperature limit ($T \ll \frac{E_F}{k_B}$) this integral can be approximated to,

$$u\left(T\right) = \frac{3}{5} n k_B T_F + \frac{\pi^2}{4} \frac{n}{E_F} \left(k_B T\right)^2, \tag{B.4}$$

as there is no analytical solution to Eq. B.3. The specific heat at a constant volume, C_V, can then be easily extracted,

$$C_V^e = \left(\frac{\partial u}{\partial T}\right)_V = \frac{\pi^2}{2} \frac{n}{E_F} k_B^2 T = \gamma T, \tag{B.5}$$

where γ is known as the Sommerfeld coefficient and n is the charge carrier density. Continuing the assumption that the electrons are a gas, we can now start to calculate the thermal conductivity. Using the kinetic theory of gases, the thermal conductivity of the gas is given by,

$$\kappa = \frac{1}{3} C_V \bar{v} l, \tag{B.6}$$

where C_V is the specific heat of the gas, $\bar{v}$ is the average speed at which the particles in the gas are moving and l is the mean free path length. When we substitute Eq. B.5 into Eq. B.6 we arrive at,

$$\kappa = \frac{1}{3} \gamma T v_F l \tag{B.7}$$

where v_F is the Fermi velocity. The Sommerfeld coefficient, the Fermi velocity and the mean free path can be assumed to be temperature-independent in this analysis. Equation B.7 shows that in the low temperature limit the thermal conductivity of metals is proportional to temperature.

Appendix C

Amplifier Theory

C.1 Amplifier Sub-circuits

C.1.0.1 Differential Pair

Example of a MOSFET differential pair is given in Figure C.1. This is a simple differential amplifier. One of the key ideas behind the differential pair is that the whole circuit should be well balanced. By this, it is meant that $I_1 = I_2 = \frac{I_{Bias}}{2}$. Its also important to note that the sources of M_1 and M_2 are at the same potential. This will help to calculate the gain of this amplifier. In the case of a small AC voltage on the for V_{In1} and a grounded V_{In2}, the AC voltage will provoke a AC current response through R_1 and R_2. This is due to the fact that I_{Bias} is constant. If there is a larger gate-source potential on M_1 then this will correspond to a greater current through R_1 and therefore increase the potential at V_{Out1}. The opposite will then happen for R_B, as the total bias current remains constant, the current through R_B decreases by the same amount as it increases on R_A. This then decreases the potential at V_{Out2} by the same amount V_{Out1} increases. To estimate the gain we need to consider the size of the current response of the MOSFET given a small AC voltage on its gate, this is the transconductance g_m. In the case of a FET in

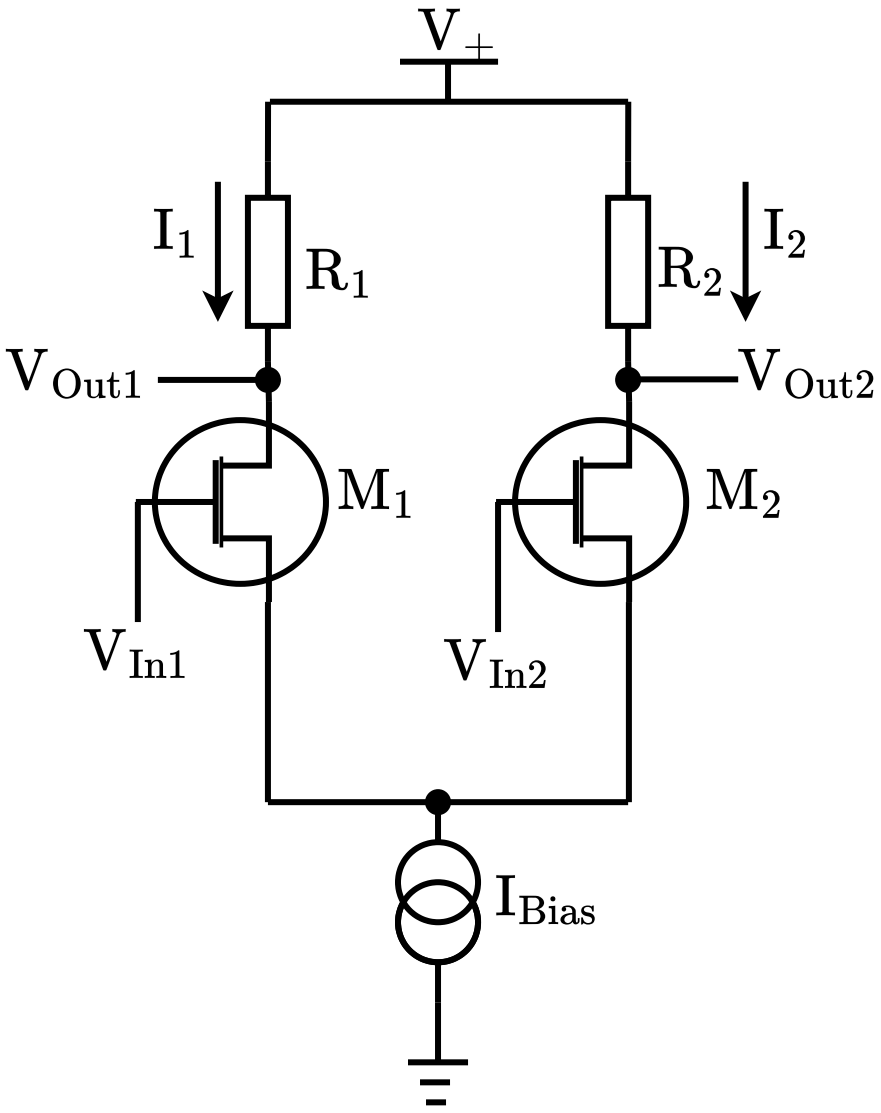

Figure C.1: Differential Pair Schematic: Resistors R_1 and R_2 set the drain voltage at FETS M_1 and M_2. These are critical to ensure the FETs stay in the saturation regime. The current bias usually would be some variant of the constant current source discussed previously. In this analysis it will be treated as an ideal current source.

saturation, this is defined as,

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{\partial}{\partial V_G}\left(\kappa\left[V_{GS} - V_{TH}\right]\right]^2\right) \tag{C.1}$$

which with further manipulation, adding back in the expression for the drain-source current, the following is arrived at,

$$g_m = \sqrt{2\kappa I_{DS}}. \tag{C.2}$$

Using this, we can express the gain for this amplifier. If $\mathrm{V_{In2}}$ is grounded then and we have a small AC voltage on V_{In1} then the gain, A_v will be expressed by,

$$A_v = \frac{V_{Out1} - V_{Out2}}{V_{In1}}. \tag{C.3}$$

This is can be further expanded,

$$A_v = \frac{\partial I_1}{\partial V_{V_{In1}}} R_1 + \frac{\partial I_2}{\partial V_{V_{In1}}} R_2 = 2\frac{\partial I_{Bias}}{2\partial V_{V_{In1}}} R_1 = g_m R_1, \tag{C.4}$$

as $R_1 = R_2$ and $I_1 \approx I_2 \approx \frac{I_{Bias}}{2}$. We can now verify this expression doing a SPICE simulation, using our example FET the ALD110800. Using the datasheet cite, for a FET in saturation where $V_{GS} - V_{Th} = 1\,V$ the drain-source current is approximately 0.25 mA. Using Equation 4.10 we can calculate an approximate value for κ of $0.25\ \frac{mA}{V^2}$. For a bias current of $33\ \mu$A, we can calculate the transconductance from C.2, which will be $128.5\ \mu$S. For resistor values $R_1 = R_2 = 100\ k\Omega$, this gives a gain of approximately 12.9. When simulated in LT SPICE this gives a gain value of 13.5, showing good agreement with the theory waveforms are shown in Figure C.2.

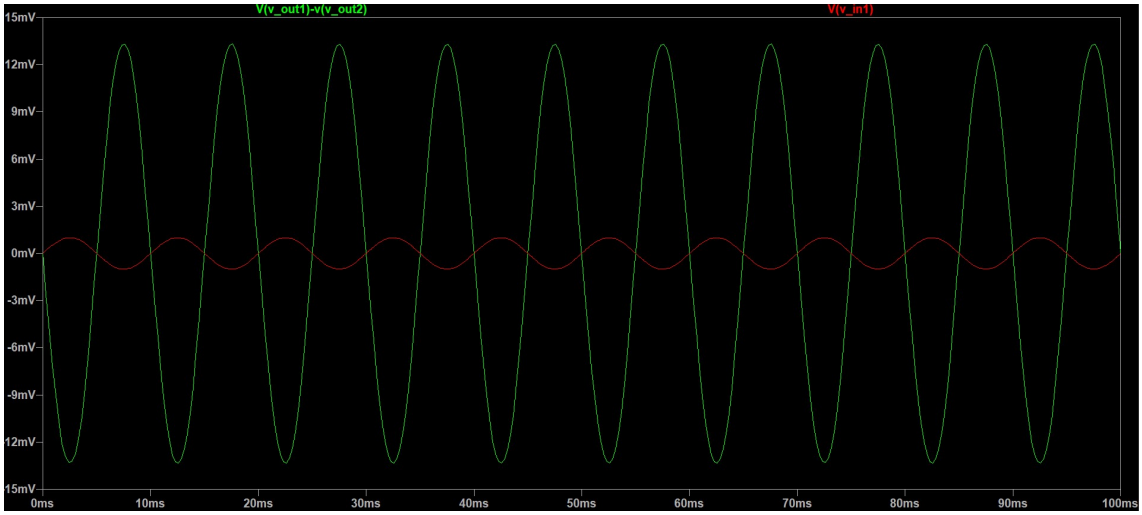

Figure C.2: LT SPICE waveform analysis of a single stage differential amplifier: Here the green waveform is the amplifier output, $V_{Out1} - V_{Out2}$ and the red is the input, V_{In}. Gain is approximately 13.

C.1.0.2 Constant Current Source

Figure C.3 shows the schematic of a constant current source. As the gate is tied to the drain potential for M_1, it means this FET is permanently in the saturation regime (providing $V_{Th} > 0$ and $V_+ > V_{Th}$). As in the saturation regime the resistance across the FET is low, the current through the drain will be determined by the R_L. For the second transistor, M_2, its gate us tied to the gate of M_1 and both sources are ground. As such they both have the same gate-source potential, and as M_1 is in saturation mode, if M_2 has the same gate-source potential then it also must be in saturation mode. The expression for the current across a FET in saturation is given approximately by (ignoring short channel effects),

$$I_{DS} = \kappa \left(V_{GS} - V_{Th}\right)^2 \tag{C.5}$$

where κ is the product of the oxide capacitance, carrier mobility and the length to width ratio of the FET. If M_1 and M_2 are identical then, $I_L = I_{Bias}$. This acts as a constant current source as the Equation C.5 doesn't depend upon the drain-source voltage, or in Figure C.3, V_x.

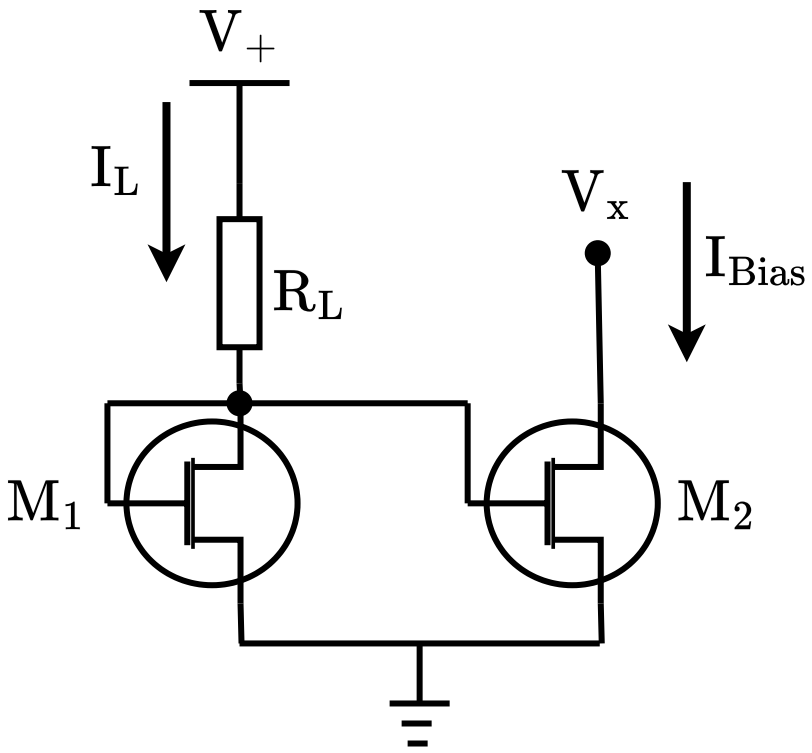

Figure C.3: Constant current source schematic: Here R_L sets I_L, which will be the drain current of the transistor M1. I_{Bias} is the current that the current source is supplying and V_x is the potential at that point.

C.1.0.3 Buffer

The common drain amplifier, or source follower, forms the buffer part of this circuit and a schematic of the common drain amplifier is shown in Fig. C.4. The aim of the buffer is to transform the output impedance of the differential amplifier, from high to low, and therefore increase the bandwidth (BW) of the amplifier. This is because the BW of the amplifier given by its low-pass filter behaviour,

$$BW \propto \frac{1}{R_{Out}C_{Load}} \tag{C.6}$$

where C_{Load} is the capacitive load, usually from the wiring of the fridge. We can calculate the gain once again for a small AC voltage on the input as the following,

$$A_v = \frac{V_{Out}}{V_{In}}. \tag{C.7}$$

The output voltage will be the product of the current response from the AC voltage input of the FET (its transconductance) and the resistance of the bias current source, R_0,

$$V_{Out} = g_m V_{GS} R_0. \tag{C.8}$$

While the input voltage, will be V_{GS} plus the voltage across the source to ground (as the input is referenced to ground, the same as the source), i.e.,

$$V_{In} = V_{GS} + g_m V_{GS} R_0. \tag{C.9}$$

As such,

$$A_v = \frac{g_m V_{GS} R_0}{V_{In} + g_m R_0 V_{In}} = \frac{g_m R_0}{g_m R_0 + 1} \approx 1, \tag{C.10}$$

when $g_m R_0 \gg 1$. The output impedance of this circuit can be given as $1/g_m$ cite, which if the transconductance is large can be 100 ohms, much smaller than a typical differential pair, for example.

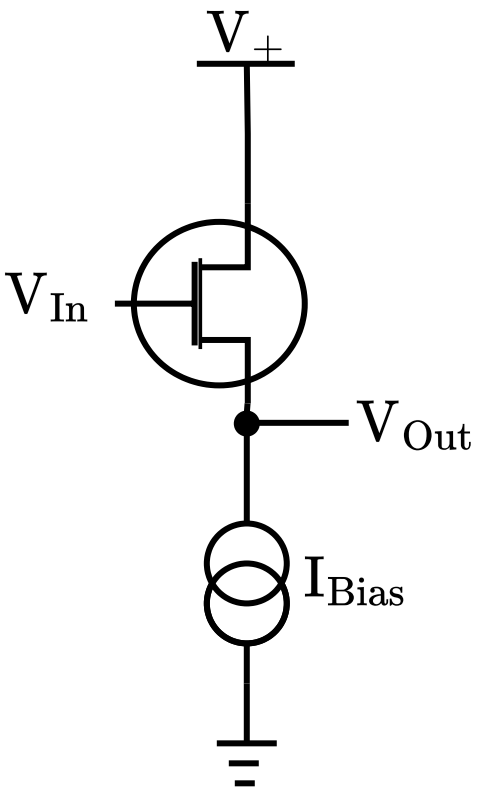

Figure C.4: Common drain amplifier schematic: Here I_{Bias} is typically a constant current source. The differential amplifier in this thesis uses two of these in order to drop the output resistance further.

Bibliography

[1] A. Guthrie, S. Kafanov, M. T. Noble, Y. A. Pashkin, G. R. Pickett, V. Tsepelin, A. A. Dorofeev, V. A. Krupenin, and D. E. Presnov, "Nanoscale real-time detection of quantum vortices at millikelvin temperatures," *Nature Communications*, vol. 12, p. 2645, May 2021. Number: 1 Publisher: Nature Publishing Group.

[2] M. D. Thompson, M. Ben Shalom, A. K. Geim, A. J. Matthews, J. White, Z. Melhem, Y. A. Pashkin, R. P. Haley, and J. R. Prance, "Graphene-based tunable SQUIDs," *Applied Physics Letters*, vol. 110, p. 162602, Apr. 2017.

[3] M. Ben Shalom, M. J. Zhu, V. I. Fal'ko, A. Mishchenko, A. V. Kretinin, K. S. Novoselov, C. R. Woods, K. Watanabe, T. Taniguchi, A. K. Geim, and J. R. Prance, "Quantum oscillations of the critical current and high-field superconducting proximity in ballistic graphene," *Nature Physics*, vol. 12, pp. 318–322, Apr. 2016. Number: 4 Publisher: Nature Publishing Group.

[4] J. Chawner, S. Barraud, M. Gonzalez-Zalba, S. Holt, E. Laird, Y. A. Pashkin, and J. Prance, "Nongalvanic Calibration and Operation of a Quantum Dot Thermometer," *Physical Review Applied*, vol. 15, p. 034044, Mar. 2021. Publisher: American Physical Society.

[5] J. R. Prance, C. G. Smith, J. P. Griffiths, S. J. Chorley, D. Anderson, G. A. C. Jones, I. Farrer, and D. A. Ritchie, "Electronic Refrigeration of a Two-Dimensional Electron Gas," *Physical Review Letters*, vol. 102, p. 146602, Apr. 2009. Publisher: American Physical Society.

[6] A. Ruffino, T.-Y. Yang, J. Michniewicz, Y. Peng, E. Charbon, and M. F. Gonzalez-Zalba, "A cryo-CMOS chip that integrates silicon quantum dots and multiplexed dispersive readout electronics," *Nature Electronics*, vol. 5, pp. 53–59, Jan. 2022. Number: 1 Publisher: Nature Publishing Group.

[7] K. Takeda, J. Kamioka, T. Otsuka, J. Yoneda, T. Nakajima, M. R. Delbecq, S. Amaha, G. Allison, T. Kodera, S. Oda, and S. Tarucha, "A fault-tolerant addressable spin qubit in a natural silicon quantum dot," *Science Advances*, vol. 2, p. e1600694, Aug. 2016. Publisher: American Association for the Advancement of Science.

[8] M. Friesen, P. Rugheimer, D. E. Savage, M. G. Lagally, D. W. van der Weide, R. Joynt, and M. A. Eriksson, "Practical design and simulation of silicon-based quantum-dot qubits," *Physical Review B*, vol. 67, p. 121301, Mar. 2003. Publisher: American Physical Society.

[9] G. Nicolí, P. Märki, B. A. Bräm, M. P. Röösli, S. Hennel, A. Hofmann, C. Reichl, W. Wegscheider, T. Ihn, and K. Ensslin, "Quantum dot thermometry at ultra-low temperature in a dilution refrigerator with a 4He immersion cell," *Review of Scientific Instruments*, vol. 90, p. 113901, Nov. 2019.

[10] J. Park, S. Subramanian, L. Lampert, T. Mladenov, I. Klotchkov, D. J. Kurian, E. Juarez-Hernandez, B. P. Esparza, S. R. Kale, A. B. K. T., S. P. Premaratne, T. F. Watson, S. Suzuki, M. Rahman, J. B. Timbadiya, S. Soni, and S. Pellerano, "A Fully Integrated Cryo-CMOS SoC for State Manipulation, Readout, and High-Speed Gate Pulsing of Spin Qubits," *IEEE Journal of Solid-State Circuits*, vol. 56, pp. 3289–3306, Nov. 2021. Conference Name: IEEE Journal of Solid-State Circuits.

[11] N. C. Dao, A. E. Kass, M. R. Azghadi, C. T. Jin, J. Scott, and P. H. W. Leong, "An enhanced MOSFET threshold voltage model for the 6–300K temperature range," *Microelectronics Reliability*, vol. 69, pp. 36–39, Feb. 2017.

[12] R. M. Incandela, L. Song, H. Homulle, E. Charbon, A. Vladimirescu, and F. Sebastiano, "Characterization and Compact Modeling of Nanometer CMOS Transistors at Deep-Cryogenic Temperatures," *IEEE Journal of the Electron Devices Society*, vol. 6, pp. 996–1006, 2018. Conference Name: IEEE Journal of the Electron Devices Society.

[13] W. Chakraborty, K. A. Aabrar, J. Gomez, R. Saligram, A. Raychowdhury, P. Fay, and S. Datta, "Characterization and Modeling of 22 nm FDSOI Cryogenic RF CMOS," *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits*, vol. 7, pp. 184–192, Dec. 2021. Conference Name: IEEE Journal on Exploratory Solid-State Computational Devices and Circuits.

[14] M. F. Gonzalez-Zalba, S. de Franceschi, E. Charbon, T. Meunier, M. Vinet, and A. S. Dzurak, "Scaling silicon-based quantum computing using CMOS technology," *Nature Electronics*, vol. 4, pp. 872–884, Dec. 2021. Number: 12 Publisher: Nature Publishing Group.

[15] F. Sebastiano, H. Homulle, B. Patra, R. Incandela, J. van Dijk, L. Song, M. Babaie, A. Vladimirescu, and E. Charbon, "Cryo-CMOS Electronic Control for Scalable Quantum Computing: Invited," in *Proceedings of the 54th Annual Design Automation Conference 2017*, DAC '17, (New York, NY, USA), pp. 1–6, Association for Computing Machinery, June 2017.

[16] J. Lisenfeld, A. Lukashenko, M. Ansmann, J. M. Martinis, and A. V. Ustinov, "Temperature Dependence of Coherent Oscillations in Josephson Phase Qubits," *Physical Review Letters*, vol. 99, p. 170504, Oct. 2007. Publisher: American Physical Society.

[17] S. A. Myers, H. Li, and G. A. Csáthy, "A ruthenium oxide thermometer for dilution refrigerators operating down to 5 mK," *Cryogenics*, vol. 119, p. 103367, Oct. 2021.

[18] R. C. Dhuley and S. W. Van Sciver, "Epoxy encapsulation of the Cernox™ SD thermometer for measuring the temperature of surfaces in liquid helium," *Cryogenics*, vol. 77, pp. 49–52, July 2016.

[19] W. B. Bloem, "A cryogenic fast response thermometer," *Cryogenics*, vol. 24, pp. 159–164, Mar. 1984.

[20] M. Seki and K. Sanokawa, "Characteristics of germanium thin film thermometers for use at low temperatures," *Cryogenics*, vol. 22, pp. 121–125, Mar. 1982.

[21] S. B. Roy, *Mott Insulators: Physics and applications*. IOP Publishing, July 2019.

[22] T. Nguyen, A. Tavakoli, S. Triqueneaux, R. Swami, A. Ruhtinas, J. Gradel, P. Garcia-Campos, K. Hasselbach, A. Frydman, B. Piot, M. Gibert, E. Collin, and O. Bourgeois, "Niobium Nitride Thin Films for Very Low Temperature Resistive Thermometry," *Journal of Low Temperature Physics*, vol. 197, pp. 348–356, Dec. 2019.

[23] R. Romestain, B. Delaet, P. Renaud-Goud, I. Wang, C. Jorel, J.-C. Villegier, and J.-P. Poizat, "Fabrication of a superconducting niobium nitride hot electron bolometer for single-photon counting," *New Journal of Physics*, vol. 6, p. 129, Oct. 2004.

[24] O. Bourgeois, E. André, C. Macovei, and J. Chaussy, "Liquid nitrogen to room-temperature thermometry using niobium nitride thin films," *Review of Scientific Instruments*, vol. 77, p. 126108, Dec. 2006.

[25] E. Dechaumphai and R. Chen, "Sub-picowatt resolution calorimetry with niobium nitride thin-film thermometer," *Review of Scientific Instruments*, vol. 85, p. 094903, Sept. 2014.

[26] J. M. A. Chawner, *New Low Temperature Techniques for Electron Thermometry and Thermal Isolation*. Ph.D., Lancaster University (United Kingdom), England, 2020. ISBN: 9798728295730.

[27] R. M. Hill, "Variable-range hopping," *Physica Status Solidi (a)*, vol. 34, pp. 601–613, Apr. 1976.

[28] B. I. Shklovskii and A. L. Efros, *Electronic Properties of Doped Semiconductors*. Springer Science & Business Media, Nov. 2013. Google-Books-ID: OZXsCAAAQBAJ.

[29] P. A. Lee and T. V. Ramakrishnan, "Disordered electronic systems," *Reviews of Modern Physics*, vol. 57, pp. 287–337, Apr. 1985. Publisher: American Physical Society.

[30] R. Rosenbaum, "Crossover from Mott to Efros-Shklovskii variable-range-hopping conductivity in ${\mathrm{In}}_{\mathit{x}}$${\mathrm{O}}_{\mathit{y}}$ films," *Physical Review B*, vol. 44, pp. 3599–3603, Aug. 1991. Publisher: American Physical Society.

[31] H. Liu, A. Pourret, and P. Guyot-Sionnest, "Mott and Efros-Shklovskii Variable Range Hopping in CdSe Quantum Dots Films," *ACS Nano*, vol. 4, pp. 5211–5216, Sept. 2010. Publisher: American Chemical Society.

[32] J. P. Pekola, K. P. Hirvi, J. P. Kauppinen, and M. A. Paalanen, "Thermometry by Arrays of Tunnel Junctions," *Physical Review Letters*, vol. 73, pp. 2903–2906, Nov. 1994.

[33] M. Palma, C. P. Scheller, D. Maradan, A. V. Feshchenko, M. Meschke, and D. M. Zumbühl, "On-and-off chip cooling of a Coulomb blockade thermometer down to 2.8mK," *Applied Physics Letters*, vol. 111, p. 253105, Dec. 2017.

[34] M. Meschke, J. Engert, D. Heyer, and J. P. Pekola, "Comparison of Coulomb Blockade Thermometers with the International Temperature Scale PLTS-2000," *International Journal of Thermophysics*, vol. 32, pp. 1378–1386, Aug. 2011.

[35] H. Grabert and M. H. Devoret, *Single Charge Tunneling: Coulomb Blockade Phenomena In Nanostructures*. Springer Science & Business Media, Nov. 2013. Google-Books-ID: l4TdBwAAQBAJ.

[36] A. T. Jones, *Cooling Electrons in Nanoelectronic Devices by On-Chip Demagnetisation*. Ph.D., Lancaster University (United Kingdom), England, 2019. ISBN: 9798691269356.

[37] M. Samani, C. P. Scheller, O. S. Sedeh, D. M. Zumbühl, N. Yurttagül, K. Grigoras, D. Gunnarsson, M. Prunnila, A. T. Jones, J. R. Prance, and R. P. Haley, "Microkelvin electronics on a pulse-tube cryostat with a gate Coulomb-blockade thermometer," *Physical Review Research*, vol. 4, p. 033225, Sept. 2022. Publisher: American Physical Society.

[38] D. I. Bradley, R. E. George, D. Gunnarsson, R. P. Haley, H. Heikkinen, Y. A. Pashkin, J. Penttilä, J. R. Prance, M. Prunnila, L. Roschier, and M. Sarsby, "Nanoelectronic primary thermometry below 4 mK," *Nature Communications*, vol. 7, p. 10455, Jan. 2016. Publisher: Nature Publishing Group.

[39] J. F. Qu, S. P. Benz, H. Rogalla, W. L. Tew, D. R. White, and K. L. Zhou, "Johnson noise thermometry," *Measurement Science and Technology*, vol. 30, p. 112001, Nov. 2019.

[40] A. Shibahara, O. Hahtela, J. Engert, H. van der Vliet, L. V. Levitin, A. Casey, C. P. Lusher, J. Saunders, D. Drung, and T. Schurig, "Primary current-sensing noise thermometry in the millikelvin regime," *Philosophical Transactions of the Royal Society A: Mathematical, Physical and Engineering Sciences*, vol. 374, p. 20150054, Mar. 2016. Publisher: Royal Society.

[41] A. Casey, F. Arnold, L. V. Levitin, C. P. Lusher, J. Nyéki, J. Saunders, A. Shibahara, H. van der Vliet, B. Yager, D. Drung, T. Schurig, G. Batey, M. N. Cuthbert, and A. J. Matthews, "Current Sensing Noise Thermometry: A Fast Practical Solution to Low Temperature Measurement," *Journal of Low Temperature Physics*, vol. 175, pp. 764–775, June 2014.

[42] A. Fleischmann, A. Reiser, and C. Enss, "Noise Thermometry for Ultralow Temperatures," *Journal of Low Temperature Physics*, vol. 201, pp. 803–824, Dec. 2020.

[43] H. B. Callen and T. A. Welton, "Irreversibility and Generalized Noise," *Physical Review*, vol. 83, pp. 34–40, July 1951.

[44] H. Nyquist, "Thermal Agitation of Electric Charge in Conductors," *Physical Review*, vol. 32, pp. 110–113, July 1928. Publisher: American Physical Society.

[45] J. B. Johnson, "Thermal Agitation of Electricity in Conductors," *Physical Review*, vol. 32, pp. 97–109, July 1928. Publisher: American Physical Society.

[46] J. Crossno, X. Liu, T. A. Ohki, P. Kim, and K. C. Fong, "Development of high frequency and wide bandwidth Johnson noise thermometry," *Applied Physics Letters*, vol. 106, p. 023121, Jan. 2015. arXiv:1411.4596 [cond-mat].

[47] M. M. Atalla, E. Tannenbaum, and E. J. Scheibner, "Stabilization of Silicon Surfaces by Thermally Grown Oxides*," *Bell System Technical Journal*, vol. 38, no. 3, pp. 749–783, 1959.

_eprint: https://onlinelibrary.wiley.com/doi/pdf/10.1002/j.1538-7305.1959.tb03907.x.

[48] G. E. Moore, "Cramming more components onto integrated circuits," vol. 38, no. 8, 1965.

[49] R. Dennard, F. Gaensslen, H.-N. Yu, V. Rideout, E. Bassous, and A. LeBlanc, "Design of ion-implanted MOSFET's with very small physical dimensions," *IEEE Journal of Solid-State Circuits*, vol. 9, pp. 256–268, Oct. 1974. Conference Name: IEEE Journal of Solid-State Circuits.

[50] W. Cao, H. Bu, M. Vinet, M. Cao, S. Takagi, S. Hwang, T. Ghani, and K. Banerjee, "The future transistors," *Nature*, vol. 620, pp. 501–515, Aug. 2023. Publisher: Nature Publishing Group.

[51] A. K. Jonscher, "p-n junctions at very low temperatures," *British Journal of Applied Physics*, vol. 12, pp. 363–371, Aug. 1961.

[52] A. Jonscher, "Semiconductors at cryogenic temperatures," *Proceedings of the IEEE*, vol. 52, pp. 1092–1104, Oct. 1964. Conference Name: Proceedings of the IEEE.

[53] C. G. Rogers, "Low frequency noise in MOST's at cryogenic temperatures," *Solid-State Electronics*, vol. 11, pp. 1099–1104, Dec. 1968.

[54] G. A. Swartz, "Low-temperature hall coefficient and conductivity in heavily doped silicon," *Journal of Physics and Chemistry of Solids*, vol. 12, pp. 245–259, Feb. 1960.

[55] R. R. Wagner, P. T. Anderson, and B. Bertman, "Junction Field Effect Transistors at 4.2 K," *Review of Scientific Instruments*, vol. 41, pp. 917–919, July 1970.

[56] L. L. Ananév, A. M. Pozharov, and N. V. Egorov, "A cooled amplifier with field effect transistors having a noise temperature of 1K," *Cryogenics*, vol. 18, pp. 308–309, Jan. 1978. ADS Bibcode: 1978Cryo...18..308A.

[57] H. R. Wampach and N. S. Sullivan, "Low-dissipation tunable rf preamplifier for low temperature NMR applications," *The Review of Scientific Instruments*, vol. 49, p. 1622, Dec. 1978.

[58] R. J. Prance, A. P. Long, T. D. Clark, and F. Goodall, "UHF ultra low noise cryogenic FET preamplifier," *Journal of Physics E: Scientific Instruments*, vol. 15, pp. 101–104, Jan. 1982.

[59] M. G. Rao and R. G. Scurlock, "Cryogenic Instrumentation with Cold Electronics — a Review," in *Advances in Cryogenic Engineering: Volume 31* (R. W. Fast, ed.), Advances in Cryogenic Engineering, pp. 1211–1220, Boston, MA: Springer US, 1986.

[60] M. C. M. Atkinson and R. G. Scurlock, "Use of precision low noise monolithic instrumentation amplifiers at low temperatures," *Cryogenics*, vol. 25, pp. 393–394, July 1985.

[61] E. C. Hannah, "Low temperature magnetic cores and a preamp for low impedance cryogenic sources," *Review of Scientific Instruments*, vol. 52, pp. 1087–1091, July 1981.

[62] D. W. Alderman, "Liquid Helium Temperature cw NMR S/N Improvement Using a MOSFET rf Amplifier," *Review of Scientific Instruments*, vol. 41, pp. 192–197, Feb. 1970.

[63] J. H. Goebel, "Liquid helium-cooled MOSFET preamplifier for use with astronomical bolometer," 2024.

[64] F. J. Low, "Application Of JFets To Low Background Focal Planes In Space," in *Infrared Astronomy: Scientific/Military Thrusts and Instrumentation*, vol. 0280, pp. 56–60, SPIE, July 1981.

[65] E. Tward and R. Kirschman, "Proceedings of the Cold Electronics Workshop," pp. 3–4, Nov. 1984. Conference Name: Workshop held in Pasadena ADS Bibcode: 1984pasadwork....3T.

[66] M. S. Shur and L. F. Eastman, "Near ballistic electron transport in GaAs devices at 77°K," *Solid-State Electronics*, vol. 24, pp. 11–18, Jan. 1981.

[67] A. Kamgar, "Subthreshold behavior of silicon MOSFETs at 4.2 K," *Solid-State Electronics*, vol. 25, pp. 537–539, July 1982.

[68] R. Maddox, "p-MOSFET parameters at cryogenic temperatures," *IEEE Transactions on Electron Devices*, vol. 23, pp. 16–21, Jan. 1976. Conference Name: IEEE Transactions on Electron Devices.

[69] T. Wade, A. van der Ziel, E. Chenette, and G. Roig, "Noise effects in bipolar junction transistors at cryogenic temperatures: Part I," *IEEE Transactions on Electron Devices*, vol. 23, pp. 998–1007, Sept. 1976. Conference Name: IEEE Transactions on Electron Devices.

[70] M. F. Bocko, "Noise characteristics of a cryogenically cooled GaAs metal semiconductor field effect transistor at 4 MHz," *Review of Scientific Instruments*, vol. 55, pp. 256–257, Feb. 1984.

[71] D. Carlson, D. Sullivan, R. Bach, and D. Resnick, "The ETA 10 liquid-nitrogen-cooled supercomputer system," *IEEE Transactions on Electron Devices*, vol. 36, pp. 1404–1413, Aug. 1989. Conference Name: IEEE Transactions on Electron Devices.

[72] G. Ghibaudo and F. Balestra, "Low temperature characterization of silicon CMOS devices," *Microelectronics Reliability*, vol. 37, pp. 1353–1366, Sept. 1997.

[73] Y. Liu, L. Lang, Y. Chang, Y. Shan, X. Chen, and Y. Dong, "Cryogenic Characteristics of Multinanoscales Field-Effect Transistors," *IEEE Transactions on Electron Devices*, vol. 68, pp. 456–463, Feb. 2021. Conference Name: IEEE Transactions on Electron Devices.

[74] A. Akturk, M. Peckerar, M. Dornajafi, N. Goldsman, K. Eng, T. Gurrieri, and M. S. Carroll, "Impact Ionization and Freeze-Out Model for Simulation of Low Gate Bias Kink Effect in SOI-MOSFETs Operating at Liquid He Temperature," in *2009 International Conference on Simulation of Semiconductor Processes and Devices*, pp. 1–4, Sept. 2009. ISSN: 1946-1577.

[75] Y. Feng, P. Zhou, H. Liu, J. Sun, and T. Jiang, "Characterization and modelling of MOSFET operating at cryogenic temperature for hybrid superconductor-CMOS circuits," *Semiconductor Science and Technology*, vol. 19, p. 1381, Oct. 2004.

[76] H. Zhao and X. Liu, "Modeling of a standard 0.35m CMOS technology operating from 77K to 300K," *Cryogenics*, vol. 59, pp. 49–59, Jan. 2014.

[77] A. Beckers, F. Jazaeri, A. Grill, S. Narasimhamoorthy, B. Parvais, and C. Enz, "Physical Model of Low-Temperature to Cryogenic Threshold Voltage in MOSFETs," *IEEE Journal of the Electron Devices Society*, vol. 8, pp. 780–788, 2020. Conference Name: IEEE Journal of the Electron Devices Society.

[78] P. A. T Hart, M. Babaie, E. Charbon, A. Vladimirescu, and F. Sebastiano, "Subthreshold Mismatch in Nanometer CMOS at Cryogenic Temperatures," *IEEE Journal of the Electron Devices Society*, vol. 8, pp. 797–806, 2020. Conference Name: IEEE Journal of the Electron Devices Society.

[79] A. Grill, V. John, J. Michl, A. Beckers, E. Bury, S. Tyaginov, B. Parvais, A. V. Chasin, T. Grasser, M. Waltl, B. Kaczer, and B. Govoreanu, "Temperature Dependent Mismatch and Variability in a Cryo-CMOS Array with 30k Transistors," in *2022 IEEE International Reliability Physics Symposium (IRPS)*, pp. 10A.1–1–10A.1–6, Mar. 2022. ISSN: 1938-1891.

[80] B. C. Paz, L. L. Guevel, M. Casse, G. Billiot, G. Pillonnet, A. Jansen, S. Haendler, A. Juge, E. Vincent, P. Galy, G. Ghibaudo, M. Vinet, S. D. Franceschi, T. Meunier, and F. Gaillard, "Integrated Variability Measurements of 28 nm FDSOI MOSFETs down to 4.2 K for Cryogenic CMOS Applications," in *2020 IEEE 33rd International Conference on Microelectronic Test Structures (ICMTS)*, (Edinburgh, UK), pp. 1–5, IEEE, May 2020.

[81] K. Das and T. Lehmann, "Effect of deep cryogenic temperature on silicon-on-insulator CMOS mismatch: A circuit designer's perspective," *Cryogenics*, vol. 62, pp. 84–93, July 2014.

[82] P. A. 'T Hart, M. Babaie, E. Charbon, A. Vladimirescu, and F. Sebastiano, "Characterization and Modeling of Mismatch in Cryo-CMOS," *IEEE Journal of the Electron Devices Society*, vol. 8, pp. 263–273, 2020. Conference Name: IEEE Journal of the Electron Devices Society.

[83] A. Grill, E. Bury, J. Michl, S. Tyaginov, D. Linten, T. Grasser, B. Parvais, B. Kaczer, M. Waltl, and I. Radu, "Reliability and Variability of Advanced CMOS Devices at Cryogenic Temperatures," in *2020 IEEE International Reliability Physics Symposium (IRPS)*, pp. 1–6, Apr. 2020. ISSN: 1938-1891.

[84] T. Chen, C. Zhu, L. Najafizadeh, B. Jun, A. Ahmed, R. Diestelhorst, G. Espinel, and J. D. Cressler, "CMOS reliability issues for emerging cryogenic Lunar electronics applications," *Solid-State Electronics*, vol. 50, pp. 959–963, June 2006.

[85] I. Byun, D. Min, G. Lee, S. Na, and J. Kim, "A Next-Generation Cryogenic Processor Architecture," *IEEE Micro*, vol. 41, pp. 80–86, May 2021. Conference Name: IEEE Micro.

[86] E. Charbon, F. Sebastiano, A. Vladimirescu, H. Homulle, S. Visser, L. Song, and R. M. Incandela, "Cryo-CMOS for quantum computing," in *2016 IEEE International Electron Devices Meeting (IEDM)*, (San Francisco, CA, USA), pp. 13.5.1–13.5.4, IEEE, Dec. 2016.

[87] B. Patra, R. M. Incandela, J. P. G. van Dijk, H. A. R. Homulle, L. Song, M. Shahmohammadi, R. B. Staszewski, A. Vladimirescu, M. Babaie, F. Sebastiano, and E. Charbon, "Cryo-CMOS Circuits and Systems for Quantum Computing Applications," *IEEE Journal of Solid-State Circuits*, vol. 53, pp. 309–321, Jan. 2018. Conference Name: IEEE Journal of Solid-State Circuits.

[88] Y. Guo, Q. Liu, T. Li, N. Deng, Z. Wang, H. Jiang, and Y. Zheng, "Cryogenic CMOS RF Circuits: A Promising Approach for Large-Scale Quantum Computing," *IEEE Transactions on Circuits and Systems II: Express Briefs*, pp. 1–1, 2023.

[89] M. Mehrpoo, B. Patra, J. Gong, J. Van Dijk, H. Homulle, G. Kiene, A. Vladimirescu, F. Sebastiano, E. Charbon, and M. Babaie, "Benefits and Challenges of Designing Cryogenic CMOS RF Circuits for Quantum Computers," in *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*, (Sapporo, Japan), pp. 1–5, IEEE, May 2019.

[90] M. T. Rahman and T. Lehmann, "A cryogenic DAC operating down to 4.2K," *Cryogenics*, vol. 75, pp. 47–55, Apr. 2016.

[91] P. Vliex, C. Degenhardt, C. Grewing, A. Kruth, D. Nielinger, S. Van Waasen, and S. Heinen, "Bias Voltage DAC Operating at Cryogenic Temperatures

for Solid-State Qubit Applications," *IEEE Solid-State Circuits Letters*, vol. 3, pp. 218–221, 2020.

[92] H. Zhao and X. Liu, "A low-power cryogenic analog to digital converter in standard CMOS technology," *Cryogenics*, vol. 55-56, pp. 79–83, May 2013.

[93] Y. Creten, P. Merken, W. Sansen, R. Mertens, and C. Van Hoof, "A Cryogenic ADC operating Down to 4.2K," in *2007 IEEE International Solid-State Circuits Conference. Digest of Technical Papers*, (San Francisco, CA, USA), pp. 468–616, IEEE, Feb. 2007.

[94] H. Homulle, S. Visser, B. Patra, G. Ferrari, E. Prati, F. Sebastiano, and E. Charbon, "A reconfigurable cryogenic platform for the classical control of quantum processors," *Review of Scientific Instruments*, vol. 88, p. 045103, Apr. 2017.

[95] I. D. Conway Lamb, J. I. Colless, J. M. Hornibrook, S. J. Pauka, S. J. Waddy, M. K. Frechtling, and D. J. Reilly, "An FPGA-based instrumentation platform for use at deep cryogenic temperatures," *Review of Scientific Instruments*, vol. 87, p. 014701, Jan. 2016.

[96] S. K. Bartee, W. Gilbert, K. Zuo, K. Das, T. Tanttu, C. H. Yang, N. D. Stuyck, S. J. Pauka, R. Y. Su, W. H. Lim, S. Serrano, C. C. Escott, F. E. Hudson, K. M. Itoh, A. Laucht, A. S. Dzurak, and D. J. Reilly, "Spin Qubits with Scalable milli-kelvin CMOS Control," July 2024. arXiv:2407.15151 [cond-mat, physics:quant-ph].

[97] D. J. Ibberson, J. Kirkman, J. J. L. Morton, M. F. Gonzalez-Zalba, and A. Gomez-Saiz, "A multi-module silicon-on-insulator chip assembly containing quantum dots and cryogenic radio-frequency readout electronics," May 2024. arXiv:2405.04104 [cond-mat, physics:quant-ph].

[98] "Intel's Millikelvin Quantum Research Control Chip Provides Denser Integration with Qubits," June 2024. Section: Data Center.

[99] C. Luo, Z. Li, T.-T. Lu, J. Xu, and G.-P. Guo, "MOSFET characterization and modeling at cryogenic temperatures," *Cryogenics*, vol. 98, pp. 12–17, Mar. 2019.

[100] A. Beckers, F. Jazaeri, H. Bohuslavskyi, L. Hutin, S. De Franceschi, and C. Enz, "Characterization and modeling of 28-nm FDSOI CMOS technology down to cryogenic temperatures," *Solid-State Electronics*, vol. 159, pp. 106–115, Sept. 2019.

[101] A. Ortiz-Conde, F. J. Garcıa Sánchez, J. J. Liou, A. Cerdeira, M. Estrada, and Y. Yue, "A review of recent MOSFET threshold voltage extraction methods," *Microelectronics Reliability*, vol. 42, pp. 583–596, Apr. 2002.

[102] Y. Tsividis and C. McAndrew, *Operation and Modeling of the MOS Transistor*. Oxford University Press, 2011. Google-Books-ID: oYmYPwAACAAJ.

[103] D. P. Foty, "Impurity ionization in MOSFETs at very low temperatures," *Cryogenics*, vol. 30, pp. 1056–1063, Dec. 1990.

[104] Y. P. Varshni, "Temperature dependence of the energy gap in semiconductors," *Physica*, vol. 34, pp. 149–154, Jan. 1967.

[105] H. D. Barber, "Effective mass and intrinsic concentration in silicon," *Solid-State Electronics*, vol. 10, pp. 1039–1051, Nov. 1967.

[106] A. Beckers, F. Jazaeri, and C. Enz, "Theoretical Limit of Low Temperature Subthreshold Swing in Field-Effect Transistors," *IEEE Electron Device Letters*, vol. 41, pp. 276–279, Feb. 2020. Conference Name: IEEE Electron Device Letters.

[107] L. Deferm, E. Simoen, and C. Claeys, "The importance of the internal bulk-source potential on the low temperature kink in NMOSTs," *IEEE Transactions on Electron Devices*, vol. 38, pp. 1459–1466, June 1991. Conference Name: IEEE Transactions on Electron Devices.

[108] "Characterization and Compact Modeling of Nanometer CMOS Transistors at Deep-Cryogenic Temperatures | IEEE Journals & Magazine | IEEE Xplore."

[109] C. Enss and S. Hunklinger, *Low-Temperature Physics*. Springer Science & Business Media, Dec. 2005. Google-Books-ID: ufM7sPMTGdAC.

[110] J. Kondo, "Resistance Minimum in Dilute Magnetic Alloys," *Progress of Theoretical Physics*, vol. 32, pp. 37–49, July 1964.

[111] F. Pobell, *Matter and Methods at Low Temperatures*. Berlin, Heidelberg: Springer, 2007.

[112] P. L. Kapitza, "Heat Transfer and Superfluidity of Helium II," *Physical Review*, vol. 60, pp. 354–355, Aug. 1941. Publisher: American Physical Society.

[113] R. Peterson and A. Anderson, "Acoustic-mismatch model of the Kaptiza resistance," *Physics Letters A*, vol. 40, pp. 317–319, July 1972.

[114] E. T. Swartz and R. O. Pohl, "Thermal boundary resistance," *Reviews of Modern Physics*, vol. 61, pp. 605–668, July 1989. Publisher: American Physical Society.

[115] G. Ridgard, J. Prance, M. Thompson, A. Graham, and B. Yager, "MEASUREMENT Application note,"

[116] "LTspice Information Center | Analog Devices," Jan. 2025.

[117] N. Simon, "Cryogenic Properties of Inorganic Insulation Materials for ITER Magnets: A Review," Tech. Rep. NISTIR-5030, 761710, Dec. 1994.

[118] Y. Zhang, T. Lu, W. Wang, Y. Zhang, J. Xu, C. Luo, and G. Guo, "Characterization and Modeling of Native MOSFETs Down to 4.2 K,"

IEEE Transactions on Electron Devices, vol. 68, pp. 4267–4273, Sept. 2021. Conference Name: IEEE Transactions on Electron Devices.

[119] T. Inaba, H. Asai, J. Hattori, K. Fukuda, H. Oka, and T. Mori, "Importance of source and drain extension design in cryogenic MOSFET operation: causes of unexpected threshold voltage increases," *Applied Physics Express*, vol. 15, p. 084004, July 2022. Publisher: IOP Publishing.

[120] N. G. Dhere, D. G. Vaiude, and W. Losch, "Composition and temperature coefficient of resistance of Ni-Cr thin films," *Thin Solid Films*, vol. 59, pp. 33–41, Apr. 1979.

[121] "Probing quantum devices with radio-frequency reflectometry | Applied Physics Reviews | AIP Publishing."

[122] F. Mallet, F. R. Ong, A. Palacios-Laloy, F. Nguyen, P. Bertet, D. Vion, and D. Esteve, "Single-shot qubit readout in circuit quantum electrodynamics," *Nature Physics*, vol. 5, pp. 791–795, Nov. 2009. Publisher: Nature Publishing Group.

[123] N. Crescini, S. Cailleaux, W. Guichard, C. Naud, O. Buisson, K. W. Murch, and N. Roch, "Evidence of dual Shapiro steps in a Josephson junction array," *Nature Physics*, vol. 19, pp. 851–856, June 2023. Publisher: Nature Publishing Group.

[124] X. P. A. Gao, G. Zheng, and C. M. Lieber, "Subthreshold Regime has the Optimal Sensitivity for Nanowire FET Biosensors," *Nano Letters*, vol. 10, pp. 547–552, Feb. 2010.

[125] M. Dini, A. Romani, M. Filippi, and M. Tartagni, "A Nanocurrent Power Management IC for Low-Voltage Energy Harvesting Sources," *IEEE Transactions on Power Electronics*, vol. 31, pp. 4292–4304, June 2016. Conference Name: IEEE Transactions on Power Electronics.

[126] A. Vladimirescu, *The Spice book*. New York: J. Wiley, 1994.

[127] R. Asanovski, A. Grill, J. Franco, P. Palestri, A. Beckers, B. Kaczer, and L. Selmi, "Understanding the Excess 1/f Noise in MOSFETs at Cryogenic Temperatures," *IEEE Transactions on Electron Devices*, vol. 70, pp. 2135–2141, Apr. 2023. Conference Name: IEEE Transactions on Electron Devices.

[128] P. Horowitz, *The art of electronics*. New York, NY: Cambridge University Press, third edition ed., 2015.

[129] "ALD NanoPower MOSFET Technology."

[130] H. Homulle and E. Charbon, "Performance characterization of Altera and Xilinx 28 nm FPGAs at cryogenic temperatures," in *2017 International Conference on Field Programmable Technology (ICFPT)*, pp. 25–31, Dec. 2017.

[131] H. Rucker, J. Korn, and J. Schmidt, "Operation of sige HBTs at cryogenic temperatures," in *2017 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, (Miami, FL), pp. 17–20, IEEE, Oct. 2017.

[132] N. Beev and M. Kiviranta, "Fully differential cryogenic transistor amplifier," *Cryogenics*, vol. 57, pp. 129–133, Oct. 2013.

[133] H.-C. Han, Z. Zhao, S. Lehmann, E. Charbon, and C. Enz, "Novel Approach to FDSOI Threshold Voltage Model Validated at Cryogenic Temperatures," *IEEE Access*, vol. 11, pp. 56951–56957, 2023. Conference Name: IEEE Access.

[134] D. Kang and S. Yu, "Cryo-CMOS design-technology co-optimization of low noise amplifier for silicon qubit readout," *Microelectronic Engineering*, vol. 262, p. 111837, June 2022.

[135] H. Bohuslavskyi, S. Barraud, V. Barral, M. Cassé, L. Le Guevel, L. Hutin, B. Bertrand, A. Crippa, X. Jehl, G. Pillonnet, A. G. M. Jansen, F. Arnaud, P. Galy, R. Maurand, S. De Franceschi, M. Sanquer, and M. Vinet,

"Cryogenic Characterization of 28-nm FD-SOI Ring Oscillators With Energy Efficiency Optimization," *IEEE Transactions on Electron Devices*, vol. 65, pp. 3682–3688, Sept. 2018. Conference Name: IEEE Transactions on Electron Devices.

[136] P. Galy, J. Camirand Lemyre, P. Lemieux, F. Arnaud, D. Drouin, and M. Pioro-Ladrière, "Cryogenic Temperature Characterization of a 28-nm FD-SOI Dedicated Structure for Advanced CMOS and Quantum Technologies Co-Integration," *IEEE Journal of the Electron Devices Society*, vol. 6, pp. 594–600, 2018. Conference Name: IEEE Journal of the Electron Devices Society.

[137] R. W. J. Overwater, M. Babaie, and F. Sebastiano, "Cryogenic-Aware Forward Body Biasing in Bulk CMOS," *IEEE Electron Device Letters*, vol. 45, pp. 152–155, Feb. 2024. Conference Name: IEEE Electron Device Letters.

[138] J. Burr, "Cryogenic ultra low power CMOS," in *1995 IEEE Symposium on Low Power Electronics. Digest of Technical Papers*, pp. 82–83, Oct. 1995.

[139] L. Giacoletto, "Diode and transistor equivalent circuits for transient operation," *IEEE Journal of Solid-State Circuits*, vol. 4, pp. 80–83, Apr. 1969. Conference Name: IEEE Journal of Solid-State Circuits.

[140] N. Yurttagül, M. Kainlauri, J. Toivonen, S. Khadka, A. Kanniainen, A. Kumar, D. Subero, J. Muhonen, M. Prunnila, and J. S. Lehtinen, "Millikelvin Si-MOSFETs for Quantum Electronics," Oct. 2024. arXiv:2410.01077 [cond-mat, physics:physics].

[141] D. R. Smith and F. R. Fickett, "Low-Temperature Properties of Silver," *Journal of Research of the National Institute of Standards and Technology*, vol. 100, no. 2, pp. 119–171, 1995.

[142] P. Zhao, Y. D. Lim, H. Y. Li, G. Luca, and C. S. Tan, "Advanced 3D Integration Technologies in Various Quantum Computing Devices," *IEEE Open Journal*

of Nanotechnology, vol. 2, pp. 101–110, 2021. Conference Name: IEEE Open Journal of Nanotechnology.

[143] S. Caplan and G. Chanin, "Critical-Field Study of Superconducting Aluminum," *Physical Review*, vol. 138, pp. A1428–A1433, May 1965. Publisher: American Physical Society.

[144] M. G. Latorre, *Chip-Based Magnetic Levitation of Superconducting Microparticles*. Ph.D., Chalmers Tekniska Hogskola (Sweden), Sweden, 2022. ISBN: 9798377680178.

[145] W. Feng, K. Kikuchi, M. Hidaka, H. Yamamori, Y. Araga, K. Makise, and S. Kawabata, "Thermal management of a 3D packaging structure for superconducting quantum annealing machines," *Applied Physics Letters*, vol. 118, p. 174004, Apr. 2021.

[146] I. Filippov, A. Anikanov, A. Rykov, A. Mumlyakov, M. Shibalov, I. Trofimov, N. Porokhov, Y. Anufriev, and M. Tarkhov, "Superconducting TSV contact for cryoelectronic devices," *Superconductor Science and Technology*, vol. 37, p. 015018, Dec. 2023. Publisher: IOP Publishing.

[147] E. Rubiola and V. Giordano, "On the 1/f Frequency Noise in Ultra-Stable Quartz Oscillators," Feb. 2006. arXiv:physics/0602110.

[148] S. O. Rice, "Mathematical analysis of random noise," *The Bell System Technical Journal*, vol. 23, pp. 282–332, July 1944. Conference Name: The Bell System Technical Journal.

[149] D. R. White, R. Galleano, A. Actis, H. Brixy, M. D. Groot, J. Dubbeldam, A. L. Reesink, F. Edler, H. Sakurai, R. L. Shepard, and J. C. Gallop, "The status of Johnson noise thermometry," *Metrologia*, vol. 33, p. 325, Aug. 1996.

[150] M. J. Deen, S. Rumyantsev, and J. Orchard-Webb, "Low frequency noise in heavily doped polysilicon thin film resistors," *Journal of Vacuum*

Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena, vol. 16, pp. 1881–1884, July 1998.

[151] C. P. Lusher, J. Li, V. A. Maidanov, M. E. Digby, H. Dyball, A. Casey, J. Nyéki, V. V. Dmitriev, B. P. Cowan, and J. Saunders, "Current sensing noise thermometry using a low Tc DC SQUID preamplifier," *Measurement Science and Technology*, vol. 12, p. 1, Jan. 2001.

[152] E. Cha, N. Wadefalk, G. Moschetti, A. Pourkabirian, J. Stenarson, and J. Grahn, "A 300-μW Cryogenic HEMT LNA for Quantum Computing," in *2020 IEEE/MTT-S International Microwave Symposium (IMS)*, pp. 1299–1302, Aug. 2020. ISSN: 2576-7216.

[153] Y. Hibi, H. Matsuo, H. Ikeda, M. Fujiwara, L. Kang, J. Chen, and P. Wu, "Cryogenic ultra-low power dissipation operational amplifiers with GaAs JFETs," *Cryogenics*, vol. 73, pp. 8–13, Jan. 2016.

[154] S. Montazeri, W.-T. Wong, A. H. Coskun, and J. C. Bardin, "Ultra-Low-Power Cryogenic SiGe Low-Noise Amplifiers: Theory and Demonstration," *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, pp. 178–187, Jan. 2016. Conference Name: IEEE Transactions on Microwave Theory and Techniques.

[155] J. Wei, "Fast convergence of white noise cross-correlation measurement archived by vector average in both frequency and time domain," May 2004. arXiv:physics/0405041.

[156] "CITLF3 | CMT, Inc.."

[157] G. Ventura, A. Bonetti, L. Lanzi, I. Peroni, A. Peruzzi, and G. Ponti, "Thermal conductivity of the normal and superconducting Al/Si 1% alloy," *Nuclear Physics B - Proceedings Supplements*, vol. 61, pp. 576–581, Feb. 1998.