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Low-Voltage Control Circuits of Formula Student Electric Racing Cars

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Abstract: Formula Student (FS) competitions aim to prepare and encourage engineering students to participate in the progression of automotive and motorsport industries. The built racing cars adhere to strict regulations set by competition guidelines to ensure the safety of both teams and spectators. For electric racing cars, the high-voltage (HV) battery system usually operates within a voltage range between 100 V to 600 V to supply the motor and its controller with the required electrical power. It is essential to ensure that these components are operating effectively to minimize battery and motor current as well as to ensure efficient and reliable performance throughout the race. A low-voltage control system (LVCS), usually operating at 12 V, is used to coordinate a wide array of critical operational and safety functions to control the HV system. These functions include: (1) turning on/off procedures, (2) monitoring speed, voltage, and current, (3) interfacing with pedals, (4) controlling dashboard features, (5) managing lighting, (6) facilitating data communication, and (7) implementing safety protocols. The design and operation of the LVCS are crucial for compliance with safety regulations and enhancing the FS electric racing car (FSERC) performance. This details and discusses the design procedures of the LVCS, using the Lancaster E-Racing (LER) FSERC as a case study. The LER car employs a 400 V battery system to power a 68-kW permanent manet synchronous motor (PMSM) using a three-phase voltage source inverter. Using mathematical analysis, SIMULINK/MATLAB® computer simulations, and the experimental real-data results provided by the LER FSERC, this study seeks to offer valuable insights regarding the LVCS practical implementation and optimization.

Keywords: electric vehicles; battery management systems; control systems; formula student; electronic design

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1. Introduction

Driven by the international desire to electrify transportation, there has been a notable surge in the number of electric racing cars participating in Formula Student (FS) competitions worldwide. As a part of their degree-level project, engineering students in different universities participate in the FS competition which supports them in transition from university studies to automotive and motorsport sectors. Thus, the project is backed and sponsored by industry to provide the newly graduate engineers with practical engineering experience as well as softs skills especially project management. In the UK, specifically in the FSUK competition managed by the Institution of Mechanical Engineers (IMechE), electric cars formed more than two-thirds of the participant vehicles in 2023, with this figure anticipated to rise in subsequent years [1–4]. This trend is not only driven by the economic and environmental advantages of electric racing cars but also by their exceptional

dynamic performance characteristics, including torque, speed, and power, which surpass those of traditional petrol racing cars [1–4].

Formula Student electric racing cars (FSERCs) are powered by electrical energy derived from a primary power source typically composed of series and parallel configurations of lithium-ion (Li-ion) battery cells [5,6]. The fundamental electrical components of an FSERC are illustrated in Figure 1 including:

1. The accumulator: This comprises the battery cells, high-voltage (HV) cables, protection devices, and the battery management system (BMS) which is responsible for monitoring and managing the batteries. Typically, the accumulator voltage is in the range of 100 V to 600 V based on the designed value of the DC-link voltage and hence the nominal voltage of the selected motor and its controller.
2. The motor controller (traction inverter): Typically, this component is a DC-AC inverter for AC motors or a DC-DC chopper for DC motors.
3. The electric motor: In the 2023 FSUK, all FSERCs utilized AC machines, either synchronous or induction. AC machines are favoured for their enhanced efficiency, compact size, higher power density, and the absence of carbon brushes, which require servicing every six months of operation [6]. Brushless DC (BLDC) motors utilize permanent magnet synchronous machines (PMSM) to generate a trapezoidal-shaped AC back electromotive force (EMF), which simplifies the modulation of the motor controller.
4. The HV system: This system encompasses the HV cables situated outside the accumulator, along with the protection fuses and the HV disconnect (HVD) interlocks. Its primary function is to manage the connection, disconnection, and safeguarding of electric current flow from the accumulator to the motor through the motor controller. It includes all components connected to the motor, inverter, the accumulator, and the DC-link between them.
5. The low-voltage (LV) system: This comprises the electronic system responsible for operating and controlling the HV systems within the FSERC. It usually operates at low voltage (LV) levels ranging from 6V to 24 V, with 12 V being a common value. The LV control system (LVCS) consists of various electronic circuits (ECs) assigned to different functions within the FSERC. These ECs are distributed across nearly every subsystem to fulfil a range of tasks, including toggling operations on/off, issuing warnings, transmitting data, or executing safety routines.

Comprehensive analyses and design methodologies relevant to FS competitions have been presented in [7–10]. The hardware and software components essential for developing a competitive FSERC are covered in [7]. The work discusses the selection of microcontrollers, analog signal acquisition circuits, and the design of a bespoke BMS and safety electronics, all of which are crucial for complying with competition rules. Additionally, the report introduces a modular software architecture that leverages an open-source bootloader for efficient firmware management and updates via a PC-hosted software tool, thereby enhancing the system's flexibility and robustness. The distribution of inverters and the redesign of electronic components within the accumulator container are discussed in [8]. The report provides detailed insights into the electric powertrain and BMS, emphasizing their critical roles in optimizing vehicle performance and ensuring operational safety. The design and development of the motor controller (MC) for FS competition vehicles is provided in [10]. It details the various stages of MC development, introducing innovative methodologies for phase current sensing and control strategy improvements. These innovations aim to achieve simplicity, robustness, and cost-effectiveness. The thorough evaluation of the MC in laboratory settings ensures its readiness for integration into the vehicle, paving the way for future enhancements in control strategies and overall vehicle performance.

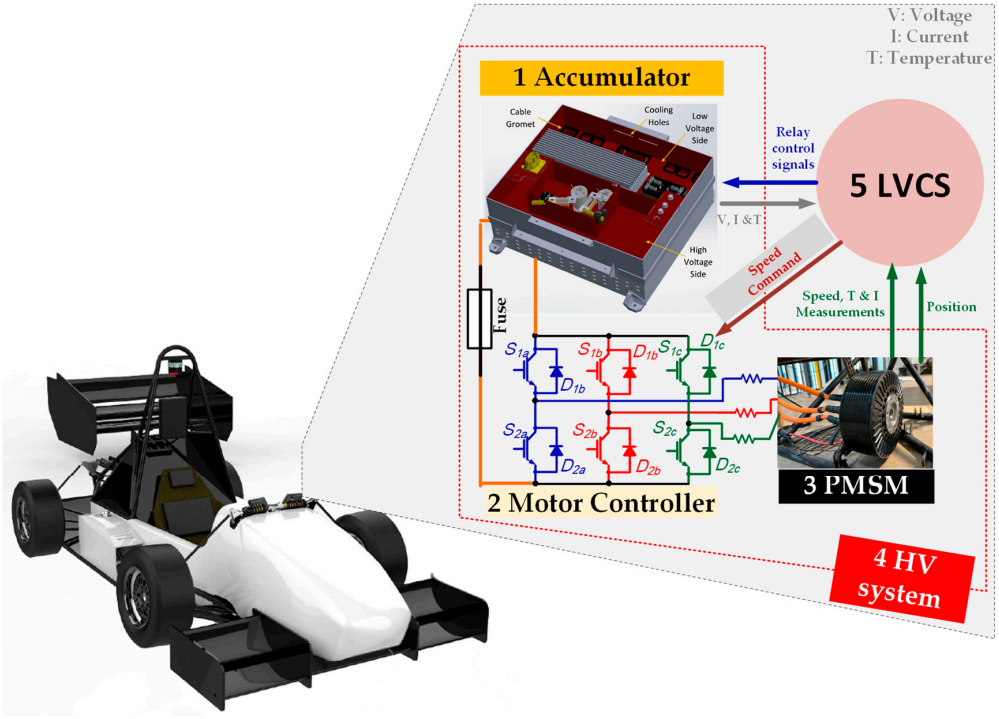


Figure 1. Main electrical systems of the FSERC.

This paper outlines the design process of the ECs within the LVCS of the 2022 FSERC developed by the Lancaster E-Racing (LER) team. Additionally, the paper illustrates the operation of these ECs and discusses their impact on the FSREC's performance. Section 2 provides a brief overview of the requirements and functions of each EC within the LVCS aided by mathematical analyses and computer simulations. Section 3 delves into the detailed configuration of individual ECs, elucidating the rationale behind their design. This section draws upon SIMULINK/MATLAB® R2024a software and experimental data to elucidate the ECs' operation. Section 4 presents the real designs with listing the components employed to build and manufacture the ECs. In Section 5, experimental results from the FSERC constructed and designed by the LER team are presented to demonstrate the overall performance of the LVCS. Finally, Section 6 summarizes the main conclusions drawn from this work and suggests potential enhancements for the developed ECs.

2. Design Overview

The LVCS is designed to function at a voltage of 12 V and is powered by a low voltage battery (LVB). For this study, a 50 Ah LiFePO4 Lithium battery was selected as the LVB due to its remarkable durability, capable of enduring over 3000 cycles. Its high energy density and lightweight makes it an ideal choice for integration within the FSERC. The capacity of the battery is selected to endure the race period without exceeding a voltage of 1 V to ensure that the functionality of the LVCS is not affected. The next subsections will detail the primary components comprising the LVCS.

2.1. Shutdown Line

The shutdown (SD) line serves as the central component of the LVCS, facilitating the connection of LV power to various ECs via control switches and interlocks. Usually, the automotive connection relays have 12 V normally open (NO) coils and hence it is preferable to keep the SD line at the same voltage. Figure 2 shows the electrical connection of the ECs, switches, and interlocks as well as their physical locations in the FSERC chassis. The main purpose of the SD line is to ensure that all safety requirements are met before activating the HV system which means that battery voltage becomes present outside the accumulator.

Beside the ECs to be presented in the following subsection, the components of the SD line are:

(a) LV master switch (LVMS): this is an NO switch responsible for linking the LVB to the remainder of the line. The first EC connected to the SD line is the brake system plausibility device (BSPD), which will be presented alongside the other ECs in subsequent subsections.

(b) SD switches: these are three normally closed (NC) manual emergency switches fitted in the cockpit, as well as on the right and left sides of the FSERC. The users can disconnect the SD line by pressing any of these three switches.

(c) Inertia switch: this is an NC switch employed to safeguard the FSERC by detecting the sudden deceleration indicative of an accident and hence trip the SD line. The inertia switch is connected in series with the SD line following the three manual SD switches.

(d) Brake over travel switch (BOTS): this is an NC switch located physically beyond the brake pedal and is used to trip the SD line when the driver exceeds the permissible range for pressing the pedal.

(e) HVD interlock: this is a NC contact integrated within the HVD connector but electrically isolated from the HV path. The main function of the HVD interlock is to guarantee that the SD line is disconnected whenever the HVD plug is removed. This will ensure that the battery voltage will not be present at the terminals of the HVD if the plug is removed for any reason.

(f) Tractive system master switch (TSMS): this NO manual switches should be the final connector in the SD line which will be switched on when the FSERC is ready to operate. Activating the TSMS signifies that the accumulator of the FSERC is prepared to be connected to the DC-link of the motor controller. The HV circuit will be closed by the activation logic (AL) EC which is responsible for turning the accumulator insulation relays (AIRs) on. It is worth noting that the negative terminal of the HV system is left floating while the ground of the LV system is connected to all conductive parts in the chassis.

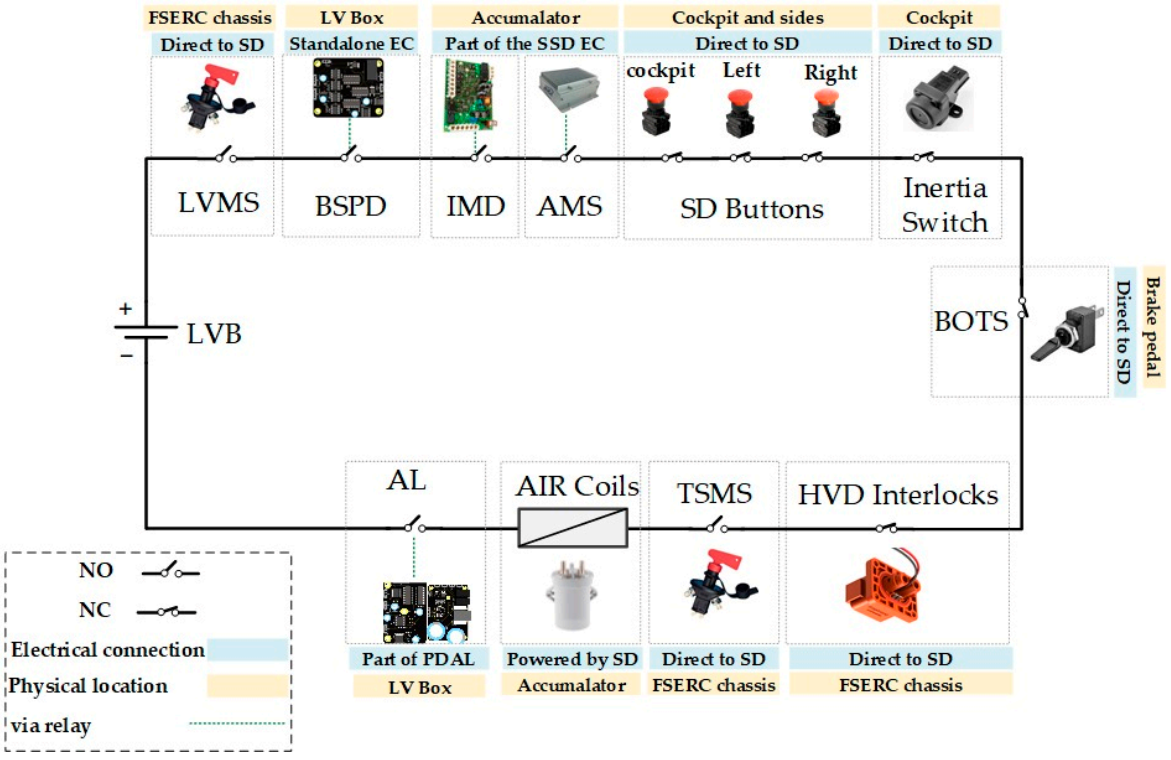


Figure 2. Schematic of the SD line.

2.2. BSPD Circuit

The main goal of the BSPD EC is to protect the electric motor from the danger of fires during hard braking when the driver tends to brake harshly during emergencies or cornering. A simple schematic for the motor connection is shown in Figure 3. The rms value of the motor current will increase significantly if the driver brakes the wheels when the MC is still generating three-phase voltage at the terminals of the PMSM stator. This leads the back emf to be lowered and the generated voltages will be subject to the low phase resistance and inductance in the motor circuit.

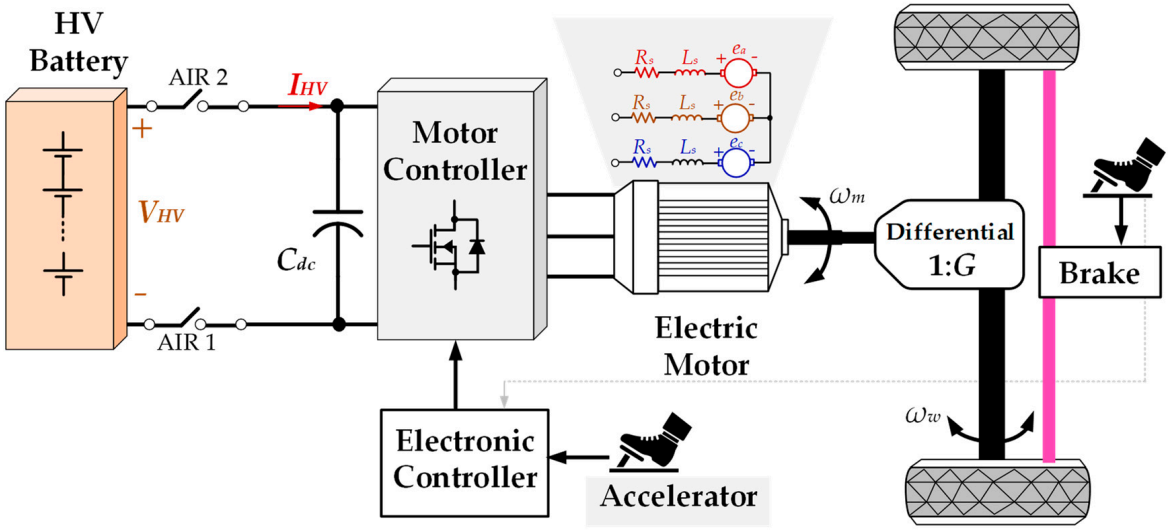


Figure 3. Electric motor circuit.

Figure 4 shows the SIMULINK/MATLAB simulation results for the FSERC drive system during hard braking with the parameters listed in Table 1. In the top graph, the driver increases the linear speed of the car using the accelerator pedal which transfers the 0–5 V analogue voltage command to the MC to control the output voltage and hence the motor's speed. During the period 1 s to 6 s, the current of the PMSM is high in the range of 80 A to generate the high torque required for acceleration. Once the top speed is reached, the PMSM current follows the reduced torque and falls below 40 A. The 1-s period between t_1 = 8s and t_2 = 9 s shows the case when hard braking occurred without releasing the accelerator pedal. In this duration, the motor's current increases to exceed the maximum permissible current for the system of 160 A which can cause a dangerous situation for the driver and other persons in the surrounding. Therefore, it is necessary and required by the safety rules that the overlap duration between the accelerator and brake pedals' signals is reduced. The BSPD EC is designed to disconnect the DC-link of the HV system by tripping the AIRs if the overlap exceeds 500 ms. It is worth mentioning that the 500-ms duration is a guiding value and the exact value of the permissible overlap may be reduced further based on the calculations and the results obtained from the computer simulations or actual testing.

The PMSM model can be expressed as [11]:

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} R_s & 0 \\ 0 & R_s \end{bmatrix} \begin{bmatrix} I_d \\ I_q \end{bmatrix} + \begin{bmatrix} L_d & 0 \\ 0 & L_q \end{bmatrix} \frac{d}{dt} \begin{bmatrix} I_d \\ I_q \end{bmatrix} + \omega \left(\begin{bmatrix} 0 & -L_q \\ L_d & 0 \end{bmatrix} \begin{bmatrix} I_d \\ I_q \end{bmatrix} + \begin{bmatrix} 0 \\ \lambda \end{bmatrix} \right) \quad (1)$$

$$\omega = P\omega_m \quad (2)$$

$$T_e = \frac{3}{2} P\lambda I_q, \quad (3)$$

where V_d and V_q are the stator voltage expressed in the synchronous frame dq coordinates, I_d and I_q are the stator dq currents, ω is the electrical frequency of the stator voltage, ω_m

is the rotational speed of the motor, λ is the flux linkage of the PMSM, R_s is the stator windings resistance, L_d and L_q are the dq components of the stator windings inductance, T_e is the developed electromechanical torque and P is the number of pair of poles. Figure 5 shows the PMSM developed torque when the driver applies the full braking torque T_{br} at the time instant t_0. Prior to t_0, the PMSM was controlled to generate the torque T_0 which covers the load and friction torques which can be calculated from [12]:

$$T_0 = \frac{mgr(\mu_{rr} + \sin(\psi))}{G} + \frac{1}{2G^3}\rho A C_d \omega_m{}^2 r^3, \quad (4)$$

where μ_{rr}, ψ, g, and ρ are the rolling resistance coefficient, the inclination of road surface, acceleration due to gravity, and density of air, respectively. The parameters m, G, A, C_d, and r also represent the vehicle mass, gearbox ratio, frontal area, drag coefficient, and wheel's radius, respectively. As the racing track is usually flat, it can be considered that $\psi = 0°$. The PMSM developed torque continues to increase until the driver releases the brake pedal of the BSPD EC trips the TS system, whichever is sooner. If this did not occur and the system continued to operate at full voltage under hard braking, the developed torque will continue to increase until it reaches the maximum value T_f as:

$$T_f = T_0 + T_{br} \quad (5)$$

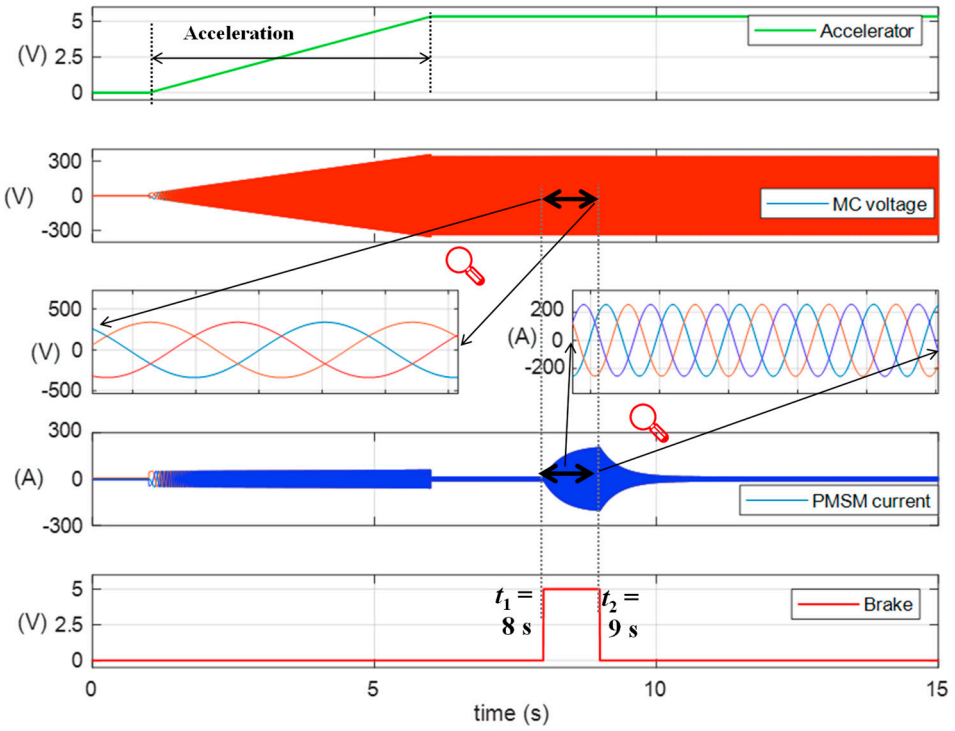


Figure 4. Hard braking of the FSERC motor at t = 8 s.

Table 1. System paramater values in the MATLAB simulations.

Paramater	Value
Nominal DC-link voltage	400 V
Motor	PMSM
No. of poles	10
Motor phase inductance	$L_d = L_q$ = 0.28 mH
Motor phase resistance	R_s = 0.2 Ω
EV mass	300 kg
Differential ratio	1:4
Wheel radius	r = 30 cm

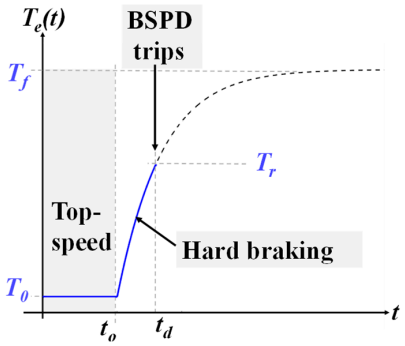


Figure 5. PMSM developed torque during hard braking.

Accordingly, the maximum value of the PMSM q-axis current can be obtained from:

$$I_{qf} = \frac{2T_f}{3P\lambda} \tag{6}$$

It can be seen from Figure 5 that adjusting the braking delay time t_d is critical to ensure that the PMSM torque does not exceed the permissible value T_r determined in the PMSM datasheet specifications.

Meanwhile, the FSERC is decelerating and the speed of the PMSM is reducing as shown in Figure 6. The PMSM top speed at the instance of braking is calculated from:

$$\omega_0 = \frac{v_{top}}{r} G, \tag{7}$$

where v_{top} is the top linear speed of the car. The final speed of the PMSM ω_f, which will be reached if the hard braking continues, can be calculated from (8). As the field-oriented control (FOC) is applied, V_q equals the peak value of the PMSM phase voltage.

$$\omega_f = \frac{R_s\left(-P\lambda \pm \sqrt{(P\lambda)^2 - 4\left(RI_{q_f} - V_q\right)\left(\frac{L_q L_d P^2 I_{q_f}}{R}\right)}\right)}{2L_q L_d P^2 I_{q_f}} \tag{8}$$

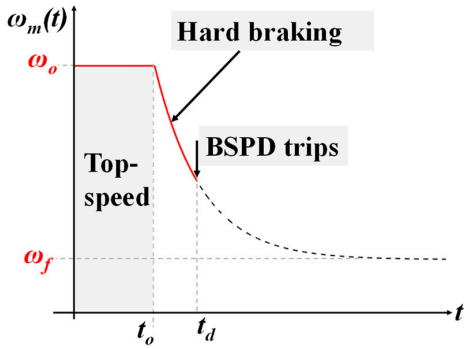


Figure 6. PMSM speed during hard braking.

Figure 7 shows the power of the FSERC during braking from top speed. It is essential to ensure that the time delay t_d is designed by the BSPD EC, so the power does not exceed the peak instantaneous power of the full system P_{max} either at the battery or the motor sides.

The instantaneous PMSM power is obtained from:

$$P(t) = (T_o + T_{br})\omega_f + \left[(T_o + T_{br})\left(\omega_o - \omega_f\right) - T_{br}\omega_f\right]e^{\frac{-t}{\tau}} - T_{br}\left(\omega_o - \omega_f\right)e^{\frac{-2t}{\tau}}, \tag{9}$$

where J_m and τ are the inertia and the time constant of the mechanical system and can be calculated from:

$$J_m = \frac{mr^2}{G^2} \tag{10}$$

$$\tau = \frac{J_m\left(\omega_o - \omega_f\right)}{T_{br}} \tag{11}$$

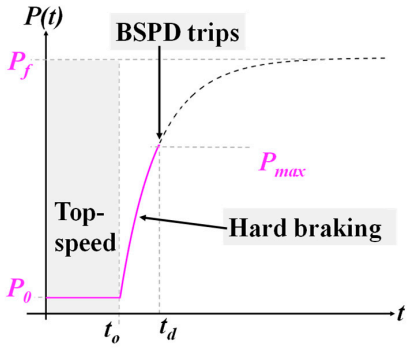


Figure 7. PMSM power during braking.

Equations (9)–(11) are used to determine the delay t_d to trip the SD line when before the power reaches the peak permissible value determined in the datasheet. As this power is originally absorbed from the HV battery, the delay t_d should be considered for the battery protection fuse selection as well.

The BSPD EC is designed to detect the hard braking when the brake and accelerator pedals are applied simultaneously. The BSPD EC will trip the SD line when this situation occurs for the designed period, t_d < 500 ms, which will in turn disconnect the HV circuit by turning the AIRs off. As shown in Figure 8, the dc-link current I_{HV} is continuously measured and compared to a threshold value I_{th} to check when a considerable current is flowing into the motor. The brake position sensor checks for the hard braking condition which is usually set to 30% of the brake travel. If the two conditions are present simultaneously and exceeded the allowed period t_d, the BSPD relay coil will be deenergised and the contact will trip the SD line to disconnect the HV circuit. It should be noted that the block diagram in Figure 8 is meant to explain the logic of the BSPD while the in-detail design will be presented in the next section.

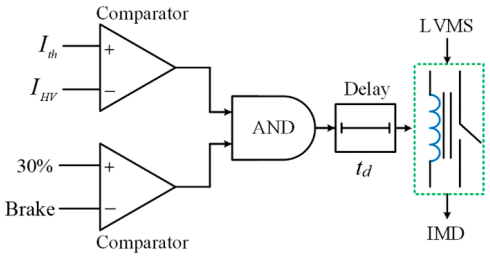


Figure 8. BSPD EC logic.

2.3. IMD and AMS

Physically situated within the accumulator box, the insulating monitoring device (IMD) is connected electrically after the BSPD and before the accumulator management system (AMS). The primary role of the IMD is to continually assess the insulation between the LV and HV systems and trip the SD line if insulation falls below a specified threshold. The AMS, typically an output from the BMS, is responsible for tripping the SD line should any battery parameters exceed acceptable limits. The IMD and AMS signals are critical to ensure the safety of the FSERC. The IMD detects any wrong or loose connection between the HV and LV systems. As the LV ground is connected to the chassis of the car, the IMD

measures the ohmic resistance between the chassis and the terminals of the HV systems. As long as this insulation resistance is higher than certain threshold (calculated as a function of the TS voltage), the IMD generates 12 VDC on its output pin. Once the insulation resistance falls below the threshold value, the output pin will generate 0 V instead.

The AMS signal can be programmed by the ORION BMS software to detect for several errors such as battery cells min/max limits, cells temperatures, cells current. . .etc. Similar to the IMD, the BMS should be programmed to give 12 V at one of its outputs when the system is error-free. If any error is detected, this voltage should fall to 0 V. It should be noted that several BMSs allow the user to toggle the logic of the error signal to generate 12 V when the error is detected and 0V otherwise. This is not preferred in this application as the operation will not be fail-safe in case when the connection between the BMS and the detecting EC is broken for any reason. Figure 9 shows the basic logic of the IMD and BMS errors detection and interface with the SD line. The outputs of the comparators associated with the IMD and AMS circuits are incorporated in the safety shutdown (SSD) EC.

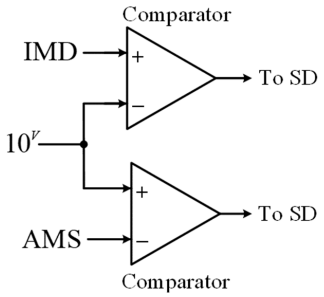


Figure 9. IMD/BMS ECs logic.

2.4. SSD Circuit

The SSD EC is responsible for incorporating the error signals from the BSPD, IMD, AMS, as well as the tractive system active light (TSAL) plausibility signal. The TSAL control will be presented in a following subsection. The SSD EC should guarantee that the SD line will not be activated without the intervention of the electrical safety officer (ESO) if a temporary error occurs and disappears. This is done by latching-off the output of the SSD EC as shown in Figure 10.

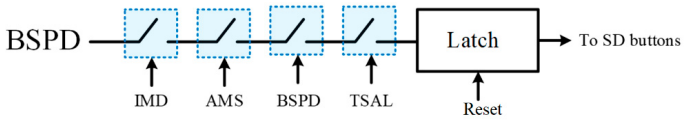


Figure 10. SSD schematic.

The ESOs are authorised to reset the SSD circuit if they are confident that the error signals have been cleared correctly. The SSD circuit is also responsible for sending the signals to the light indicators in the cockpit and other places in the chassis of the FSERC. When all error signals are cleared and the four stages are closed, the output voltage of the SSD EC will be 12VDC which will be directed to the SD buttons as shown in Figure 2.

2.5. Pre Charge/Discharge/Activation Logic Circuit

The pre-charge/discharger/activation logic (PDAL) EC is the most critical control circuit because it is responsible for turning the FSERC on and off by connecting the accumulator HV to the tractive system (TS) DC-link. To perform that safely, the PDAL is responsible for three main functions as follows:

2.5.1. Pre-Charge

The PDAL ensures that the connection between the accumulator and the TS dc-link occurs in a smooth and safe operation. At the beginning of the operation, the dc-link

voltage v_{dc} starts from zero and the capacitor C_{dc} in Figure 11 should be empty of charge at the beginning of operation and therefore closing the two AIRs (AIR_1 and AIR_2) can cause a large inrush current as:

$$I_{HV} = C_{dc}\, dv_{dc}/dt \tag{12}$$

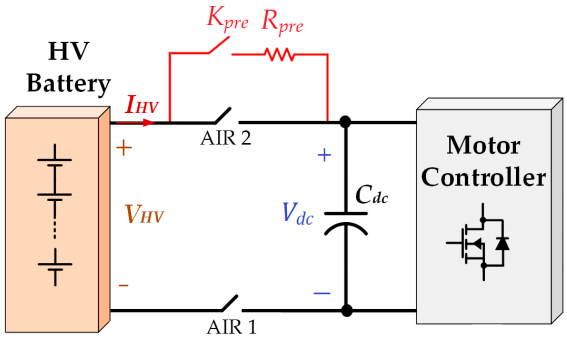


Figure 11. AIRs and pre-charge relay circuit.

Accordingly, the dc-link capacitor needs to be charged via the top circuit with the NC relay (K_{pre}) and the pre-charge resistor (R_{pre}). Once the dc-link voltage reaches 95% of the accumulator voltage (V_{HV}), the dc-link is allowed to be connected to the accumulator directly to start the operation normally.

Figure 12 shows the main logic of the Pre-charge part in the PDAL circuit. When the driver turns the system on and the AL voltage is high enough (e.g., above 6 V), the dc-link voltage is compared with the accumulator voltage to measure if it is below or above 95%. The time t_{dpre} is meant to delay turning off K_{pre} until AIR_1 is connected to ensure a proper overlap in between the two circuits. Once the pre-charge operation is done, the motor controller sees the full accumulator voltage and the FSERC is ready to start the operation.

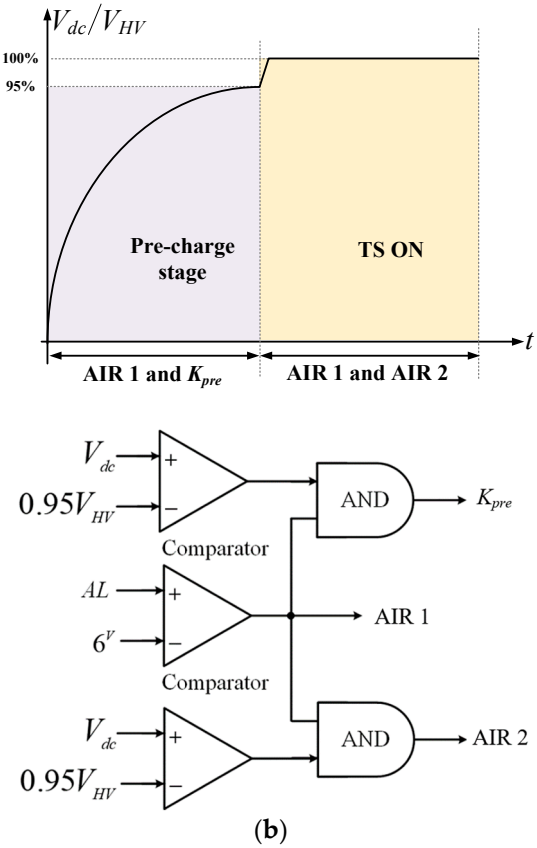


Figure 12. Pre-charge logic in the PDAL: (**a**) DC-link voltage and (**b**) pre-charge logic.

2.5.2. Discharge

This is the second part of the PDAL EC with a responsibility to ensure that the dc-link capacitor is completely discharged and accordingly its voltage is zero when the TS is disconnected from the accumulator. The TS can be disconnected in purpose by the driver or due to any error resulting in tripping the SD line. Figure 13 shows the logic for the discharge EC when the discharge resistor R_{dis} is connected across the dc-link capacitor via the contact of a NC relay controlled by the input AL which comes from the activation logic EC.

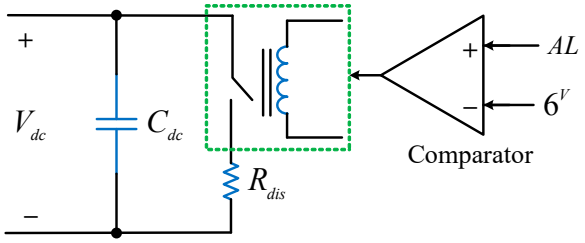


Figure 13. Discharge logic in the PDAL.

2.5.3. Activation Logic

The AL function is very critical in the operation of the FSERC and should be designed carefully. This part is responsible for main four functions:

(1) Turn on the TS when the driver is ready to start racing using a START button within the cockpit. This should start with the pre-charge stage as discussed in Section 2.5.1. For safety reason, the START button should be of a push-release type and therefore the PDAL should latch this command.

(2) Turn off the TS when driver wants to disconnect the TS system using a STOP button within the cockpit. This should be followed by the discharge routine in Section 2.5.2 to ensure that the dc-link capacitor is completely discharged.

(3) The PDAL should disconnect the TS when any error signal arises, an emergency button is pressed, or any switch is opened as shown in Figure 2. In this case, the PDAL should not allow for a re-start without clearing the error and resetting the SD line by the ESOs.

(4) If the TS is needed to be disconnected as in (2) or (3), a delay should be given between the command and the action to allow the motor controller to turn off the PMSM rotating magnetic field (RFE) before disconnecting the TS circuit. This is to protect the semiconductor devices (such as IGBTs or MOSFETs) from the voltage and current spikes that may occur. Usually, a time delay of around 200 ms should be sufficient to ensure the safe operation of the motor controller.

A simple logic diagram for the AL functions in the PDAL circuit is shown in Figure 14. To ensure the safety of the operation, the PDAL controls the AIRs at the low side of the coils as shown in Figure 2. This adds to the design complexity of the PDAL EC especially with the necessity of the off delay t_{dPDAL} as explained in point (4) above and when the resistance of the high current AIR coils are usually low (around 10 Ω) in the automotive market.

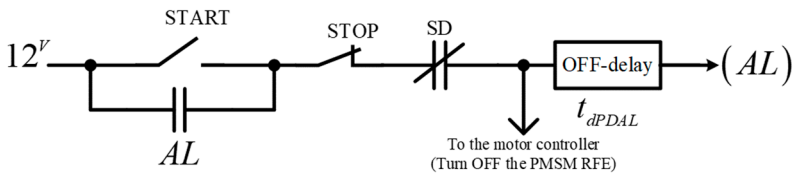
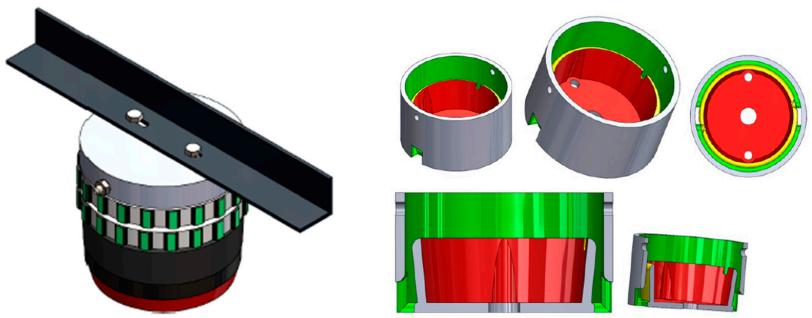


Figure 14. A simple logic diagram for the AL sub-circuit.

2.6. Tractive System Active Light

The main function of TSAL system is to indicate the TS status so the users know when the HV is present outside the accumulator. The TSAL EC controls a beacon fitted at the

top of the chassis. The beacon, as shown in Figure 15, is created as a two-part assembly to show constant green and flashing red lights.



(**a**) (**b**)

Figure 15. TSAL beacon: (**a**) assembly and (**b**) bottom section.

The red light is flashing continuously with a 50% duty cycle ratio and a frequency of 4 Hz. Both green and red lights are controlled by 12 V signals to meet the following requirement:

- The TSAL light is green when only the LV is present at the vehicle side by turning the LVMS on. This indicates to the users that the FSERC is safe to approach and scrutinize.
- The TSAL light is flashing red when any of the following is true:
  - (1) AIR 1 or AIR 2 is on
  - (2) K_{pre} is on
  - (3) V_{dc} > 60 VDC

The actual (mechanical) status of the AIRs and the relays are considered in the design of the TSAL EC. This is because it might be possible that the intentional states of the coils are off while the contacts are closed due to any mechanical failure which means that HV maybe present while the users are not aware of the hazard. The discrepancy between the intentional and the mechanical state of any AIR or the pre-charge relay should be considered seriously and therefore the red light should be latched on until the ESOs check the issue. The truth table summarising the TSAL inputs and outputs is shown in Table 2.

Table 2. Truth table for the TSAL inputs and outputs.

Intentional			Actual			Results in Discrepancy	Voltage Measure >60	Green Light	Red Light
AIR 2	AIR 1	PRE	AIR 2	AIR 1	PRE				
0	0	0	0	0	0	0	0	ON	OFF
×	×	0	×	×	1	1	×	OFF	Latch
×	0	×	×	1	×	1	×	OFF	Latch
0	×	×	1	×	×	1	×	OFF	Latch
×	×	1	×	×	0	1	×	OFF	Latch
×	1	×	×	0	×	1	×	OFF	Latch
1	×	×	0	×	×	1	×	OFF	Latch
×	×	×	×	×	×	0	1	OFF	Flashing
1	×	×	1	×	×	0	×	OFF	Flashing
×	1	×	×	1	×	0	×	OFF	Flashing
×	×	1	×	×	1	0	×	OFF	Flashing

0: OFF state; 1: ON state; ×: Can be both ON and/or OFF states.

2.7. Power Distribution Board

The power distribution board (PDB) aims to reduce the LVB energy consumption when the cooling system is on. As shown in Figure 16, the PDB will be activated when the temperatures of the accumulator and motor are above the threshold demanding the fans and the pump to be turned on. Meanwhile, the LVB will be limited to supplying energy to the rest of the LVCS ECs.

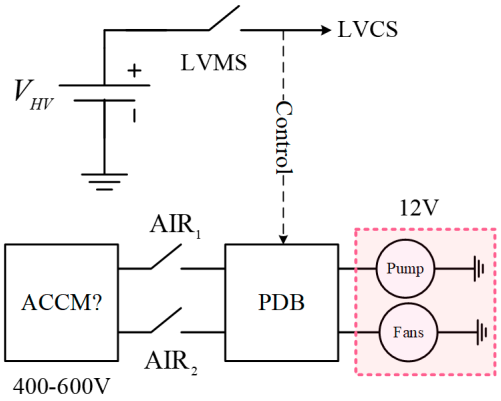


Figure 16. PDB connection between the accumulator and the LV system.

The PDB is designed to have a high efficiency and to provide a galvanic isolation between its inputs and outputs which is necessary to keep the HV and the LV systems isolated. If the galvanic isolation is not maintained, the IMD will sense a connection between the two systems resulting in tripping the SD line as mentioned in Section 2.5. To meet this requirement, the isolated DC/DC converter shown in Figure 17 is used to step down the HV to the 12 VDC required by the pump and fans.

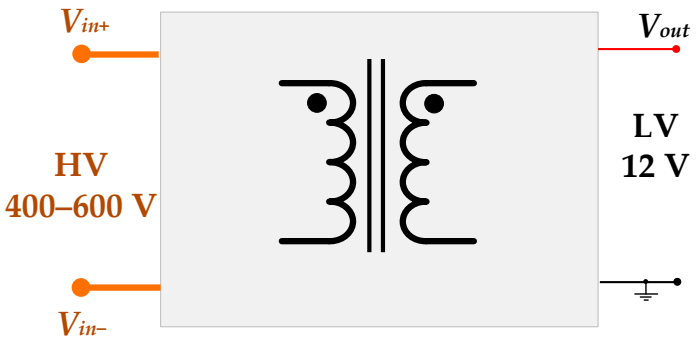


Figure 17. Isolated DC/DC converter in the PDB.

2.8. Electronic Control Unit

The electronic control unit (ECU) hosts the micro-controller (µC) and provides the required interface with several systems in the FSERC such as the acceleration pedal positioning system (APPS), brake system (BS), and the motor controller. This involves transforming the driver commands from the pedals to a torque demand request input into the motor controller, along with initialising and shutting down the motor controller, where necessary, via the enable signals as shown in the block diagram in Figure 18. The main input signals to the ECU are:

- *APPS and Brake sensors*: these are analogue input voltages in the range 0–5 V.
- *Ready-to-drive* (*RTD*) *button*: this is a push-release button connected to the 5 V rail. The driver presses the RTD button with the brake pedal to awake the FSERC program providing that the TS is active, and the pre-charge stage has passed.
- *PDAL input*: the status of the AL is sent to the ECU to inform the motor controller when the TS is about to be disconnected and accordingly the RFE of the motor should

be shut down as explained earlier in Section 2.5.3. As the PDAL EC operates at 12 V, this signal needs to be stepped down to 5 V to be compatible with the µC analogue-to-digital (A2D) inputs.

The main output signals of the ECU are:

- *Brake light control*: the required voltage to turn on the red brake light at the back of the FSERC chassis. As the digital outputs (DOs) of the µC provide 5 V output voltages, opto-couplers are employed to provide the required 12 V voltage to the brake light circuit.
- *RTD Buzzer*: to control the buzzer which gives an audible sound to the personnel indicating that the FSERC is ready to race.
- *Enable signals:* 12 V signals to start and stop the motor controller.
- *Motor controller torque/speed command*: this is an analogue 12 V signal to control the torque/speed of the motor.

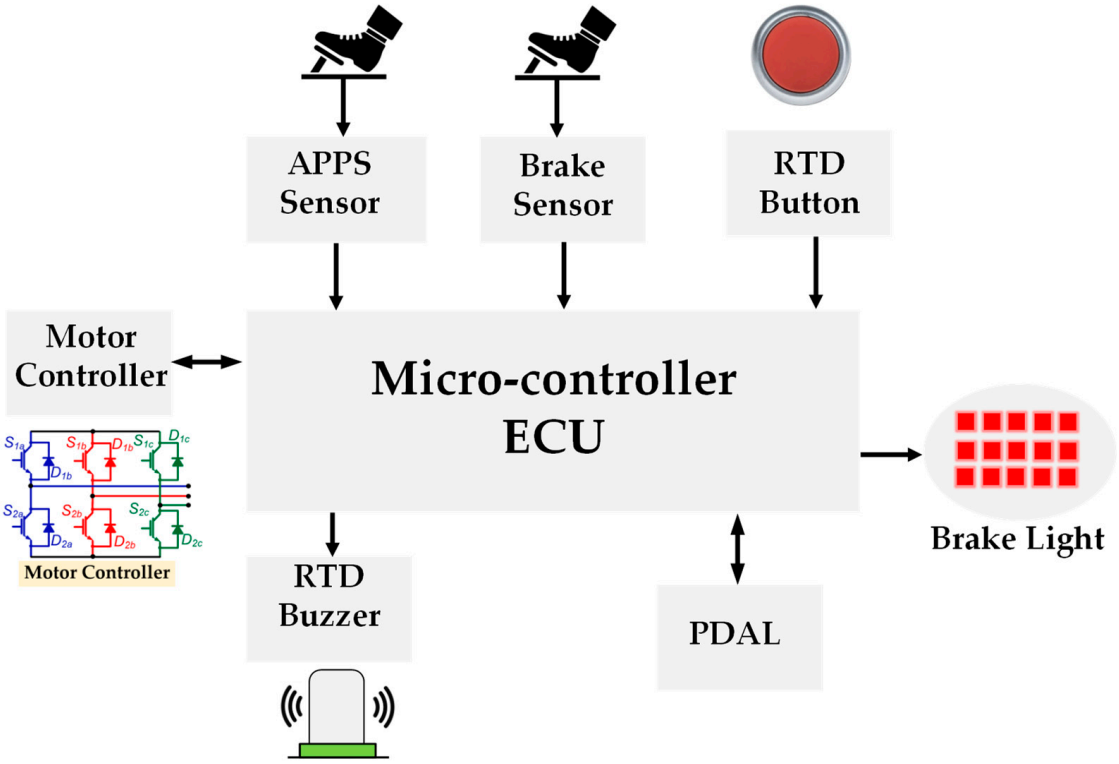


Figure 18. ECU block diagram.

3. Build Instructions

It is important to design the EC printed circuit boards (PCBs) in the simplest possible way to ease the testing, soldering, and troubleshooting them when there is any fault. The PCB schematics are designed using KiCad®(2024) as it is an open source and free software which facilitate the design and simulation process. Each circuit was designed and tested separately. However, some amendments were necessary when issues occurred during the interface process.

3.1. BSPD

The detailed schematic for the BSPD EC is provided in the Supplementary Files of the paper. Connector J1 receives the measurement from the current sensor as an analogue signal between 0–5 V which represents the accumulator output current between 0–200 A. J2 is connected to the brake sensor to detect the hard braking. Connectors J4 and J6 are sending output signals to the SSD and PDAL ECs to inform about the status of the BSPD.

Figure 19 shows a simplified diagram for the overall schematic which consists of the three main stages that will be explained in the following subsections.

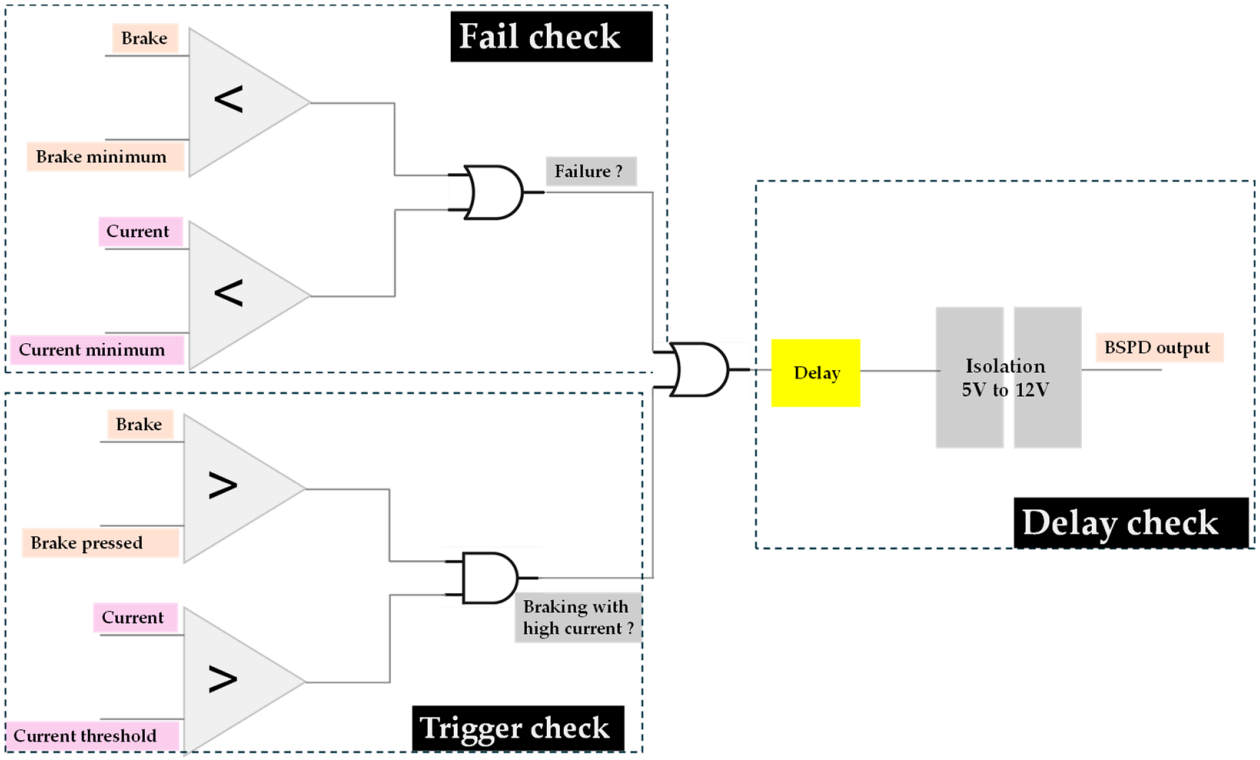
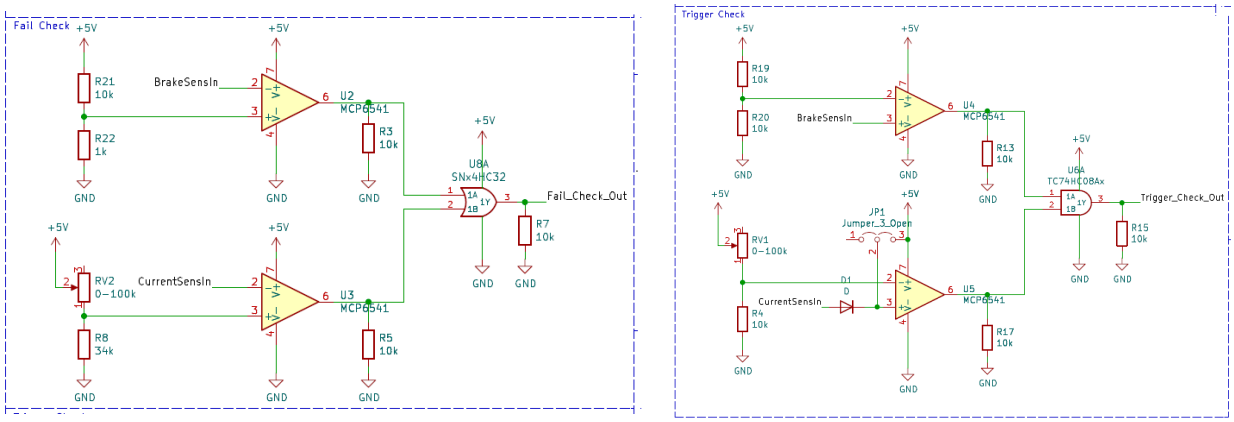


Figure 19. A simplified schematic of the BSPD circuit.

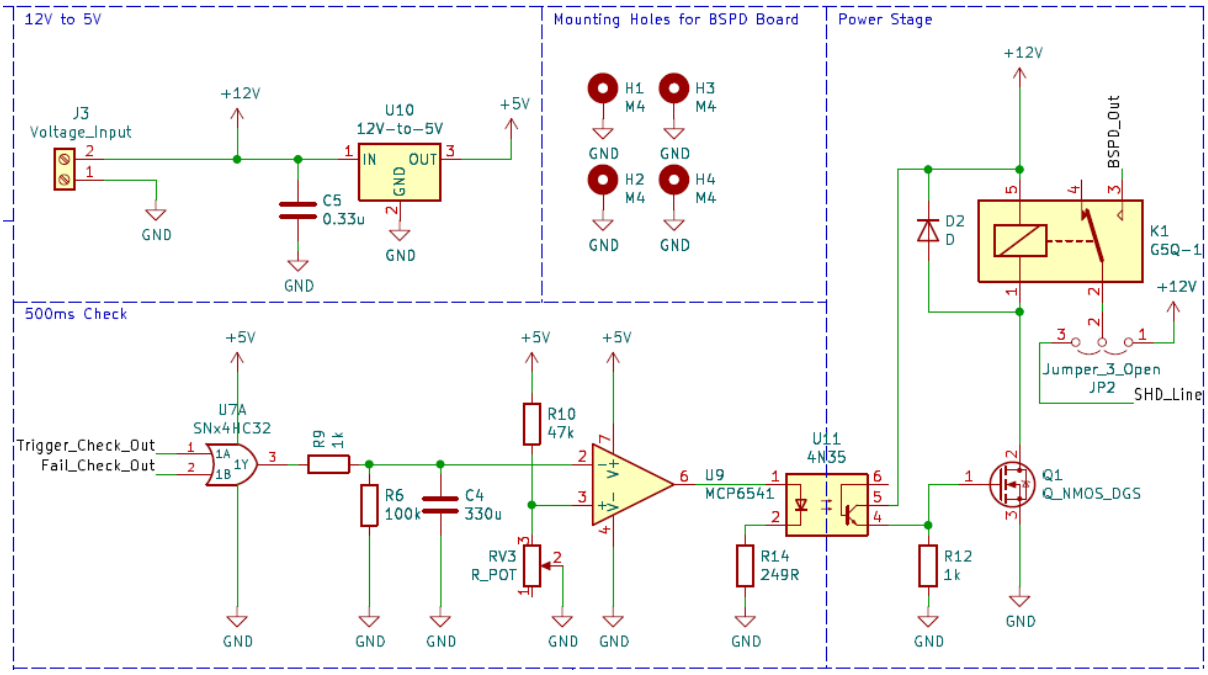
3.1.1. Fail Check

This part is responsible for checking that the received signals from the current and brake sensors are intact and kept with the expected range. To ensure a fail-safe operation, it is important to ensure that the readings are not low due to any cut in the wires between the brake pedals and the BSPD circuit. As shown in Figure 20a, high-speed differential comparators are employed to ensure that that the measurements do not fall below a specific threshold which can be pre-set using potentiometers in the voltage divider circuits. If any of the conditions is violated, the output of the stage will be high (≈5 V).



(**a**) (**b**)

Figure 20. *Cont.*



(**c**)

Figure 20. BSPD stages: (**a**) fail check, (**b**) trigger check, and (**c**) power/delay.

3.1.2. Tigger Check

The input signals, if healthy, will be compared with the threshold voltages to check if the two conditions are high together using an AND gate as shown in Figure 20b.

3.1.3. Power and Delay Stage

The NO contact of relay K_1 is connected in series with the SD line and will be closed only if pin 1 in K1 is pulled down to the ground (GND). To pull pin 1 to GND, device Q1, which is an n-type metal–oxide–semiconductor field-effect transistor (MOSFET), is used. This condition will be satisfied only if the inputs from the fail-check and trigger-check stages are both low because they are connected as inputs to the OR gate U7A. The RC circuit composed of R9, R6, and C4 is designed to delay the tripping in case if the driver released the brake pedal with the 500 ms period.

3.2. SSD

Figure 21 shows the overall schematic of the SSD EC while the detailed is provided in the Supplementary Files of the paper. To simplify the design process, the four stages use the same modular power stage which is controlled by a 12 V control signal.

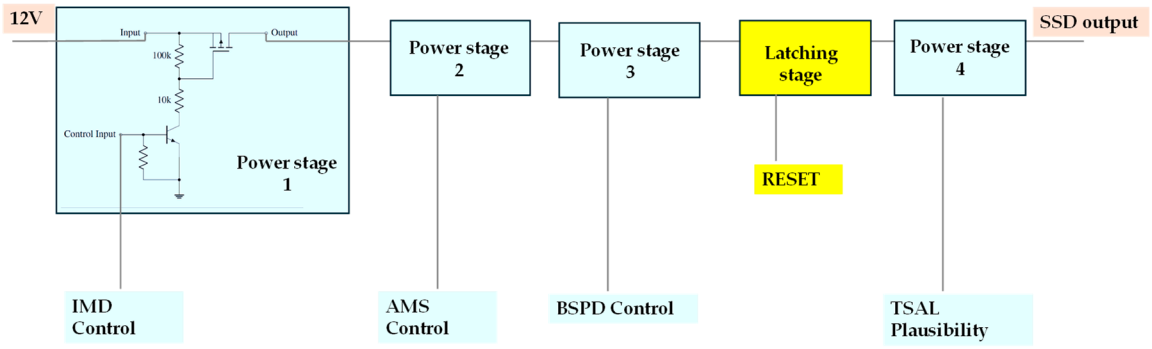


Figure 21. A simplified schematic of the SSD circuit.

The control section is detailed in Figure 22a with the three identical series stages. The modular design of each stage, shown in Figure 22b, consists of p-type MOSFET and npn bipolar junction transistor (BJT) with their drive resistors. If the control input is high (≈12 V), the BJT will be on keeping the gate voltage of the MOSFET will be below the threshold. Thus, the MOSFET will conduct the SD current to the next stage and the output voltage will be 12 V. When the control input falls, the BJT will be turned off and the MOSFET gate voltage will be increased to 12 V. Consequently, the MOSFET will be turned off and the SD line will be disconnected at this stage. After the IMD, AMS, and the BSPD stages, the latching relay will keep the SD line disconnected in case of any error until the ESOs reset the line again provided that the three stages are fault-free. The TSAL stage come after the latching relay and therefore is allowed to clear itself.

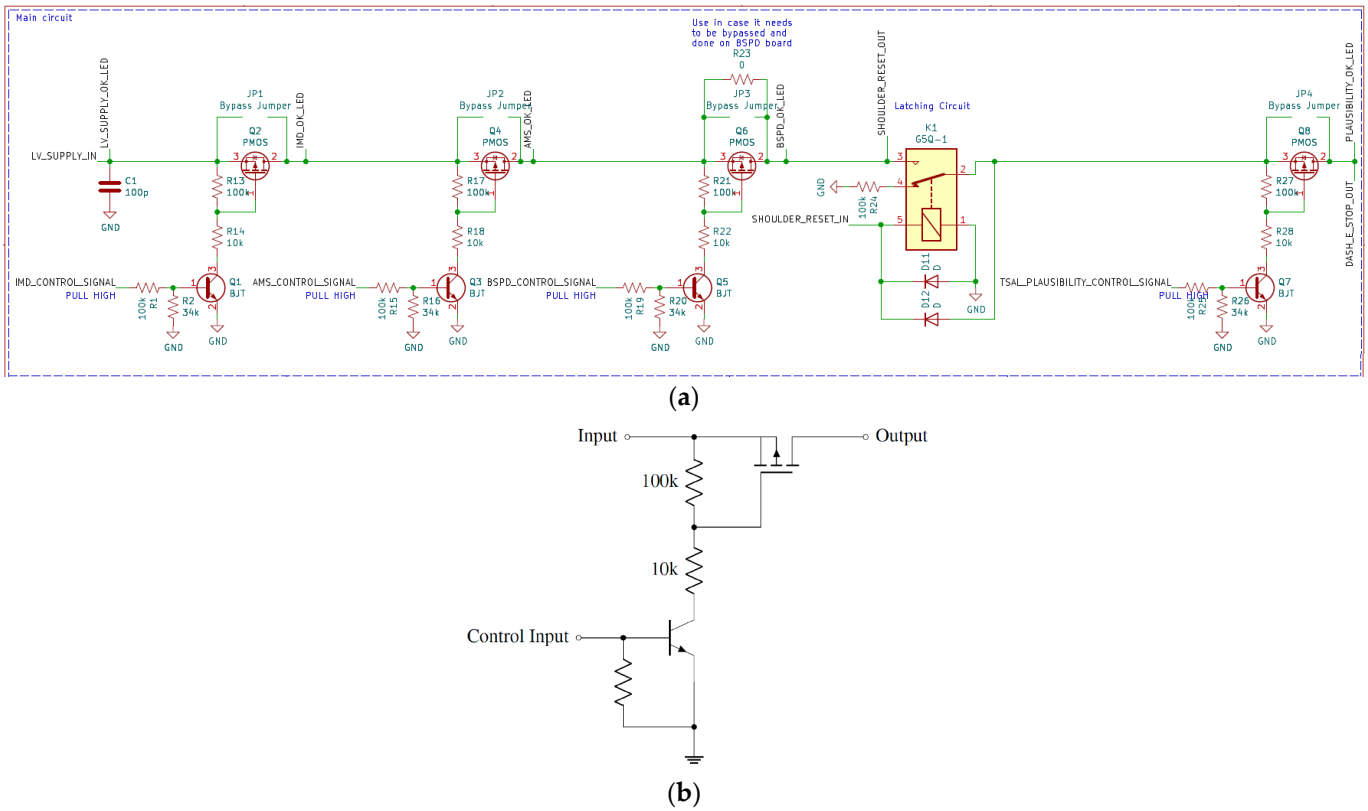
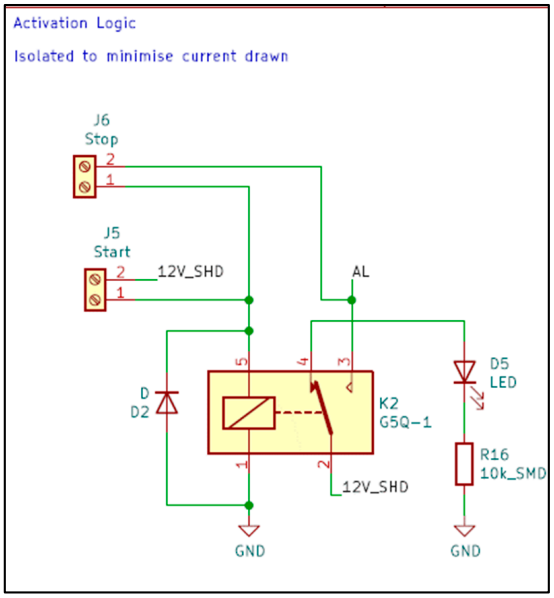


Figure 22. SSD: (**a**) main control section, and (**b**) modular power stage.

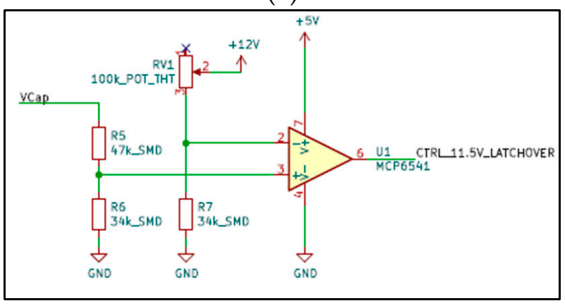
3.3. PDAL

The detailed schematic of the PDAL EC is provided in the Supplementary Files of this paper. The top left part of the circuit receives the signals from the start and stop push-release buttons that are installed in physically in the cockpit. The breakdown of the PDAL stages is shown in Figure 23. Figure 23a shows the AL part. If the start button at J5 is pressed when the SD line is healthy, the relay K_2 will latch the 12 V input from the SD line at pin 2 to the AL output at pin 3. The AL will be latched at 12 V until the driver presses the stop button connected to connector J6 or the 12 V supply at pin 2 is cut due to an error or disconnection in the SD line. Figure 23b shows the process for charging two parallel capacitors C_1 and C_2 that through the resistor R_3. It should be noted that this is different to the pre-charging stage for the dc-link capacitor which is connected to the MC. C_1 and C_2 are responsible for creating a time delay in the SD path which is responsible for protecting the MC. This delay is required to inform the MC that the SD line is going to disconnect so the rotating magnetic field is turned off using the RFE signal from the PDAL circuit to the MC. The comparison in Figure 23c will latch C_1 and C_2 to the SD line once a threshold voltage has been exceeded. The comparison in Figure 24d will disconnect the

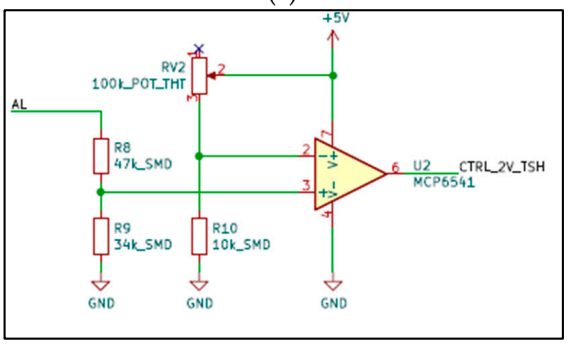
AIRs when the voltage falls below a certain threshold. The comparison in Figure 23d will disconnect the AIRs when the voltage falls below a certain threshold. The battery voltage is compared to the dc-link capacitor voltage as shown in the pre-charge stage in Figure 23e. When the dc-link voltage exceeds 95%, the control signal of the positive relay (AIR_2) turns is high while the control signal of the pre-charge relay is low. The low-pass filter C_4 and R_{14} creates a short delay to ensure a proper overlap between the relays to avoid arcing during transition. The coils of the AIRs and pre-charge relays are connected to connector J1 while the information about the states is sent through the other connectors.



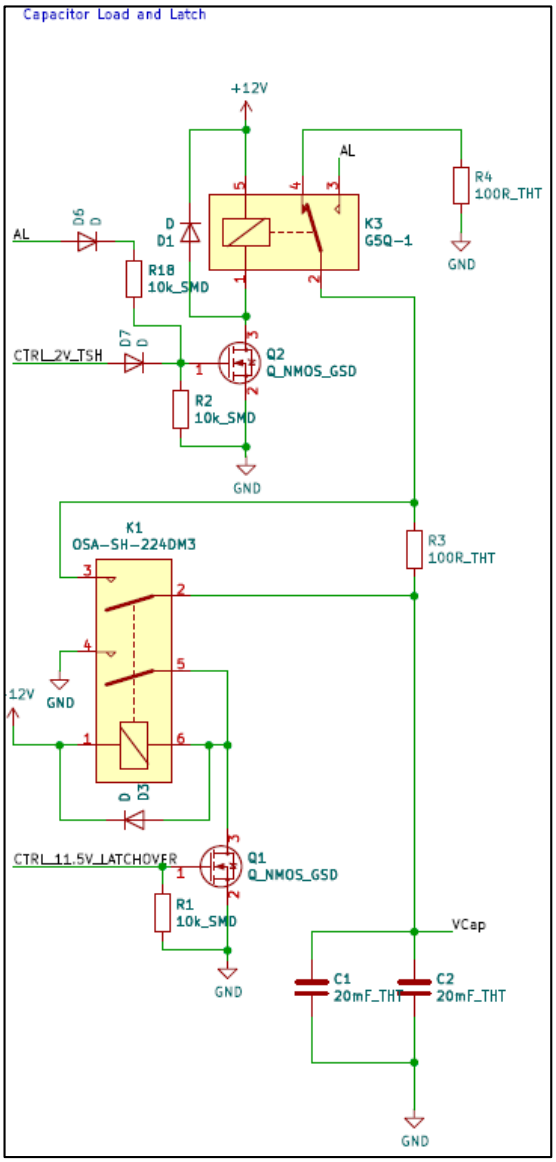
(**a**)



(**c**)

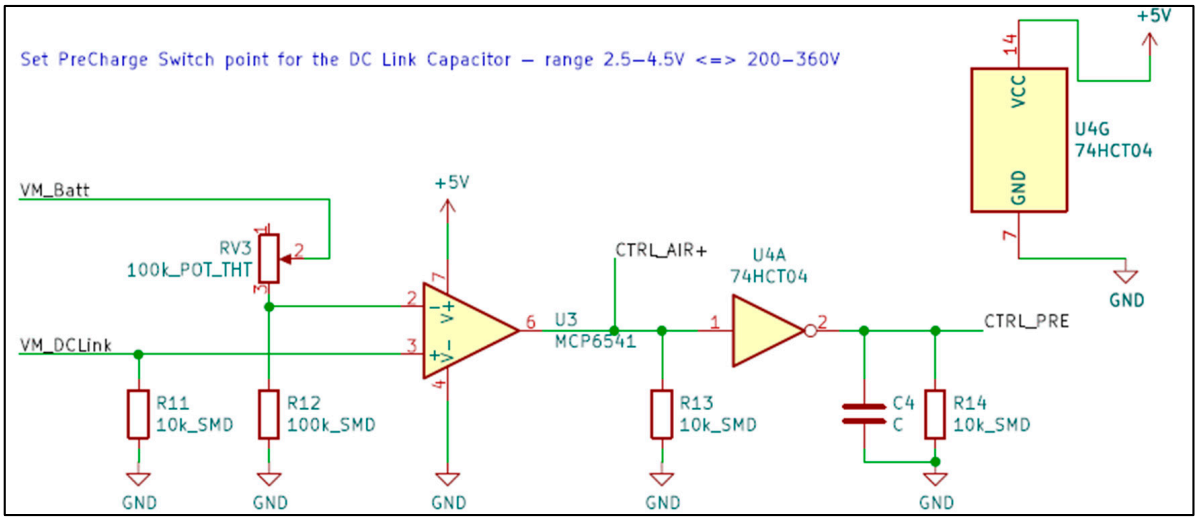


(**d**)



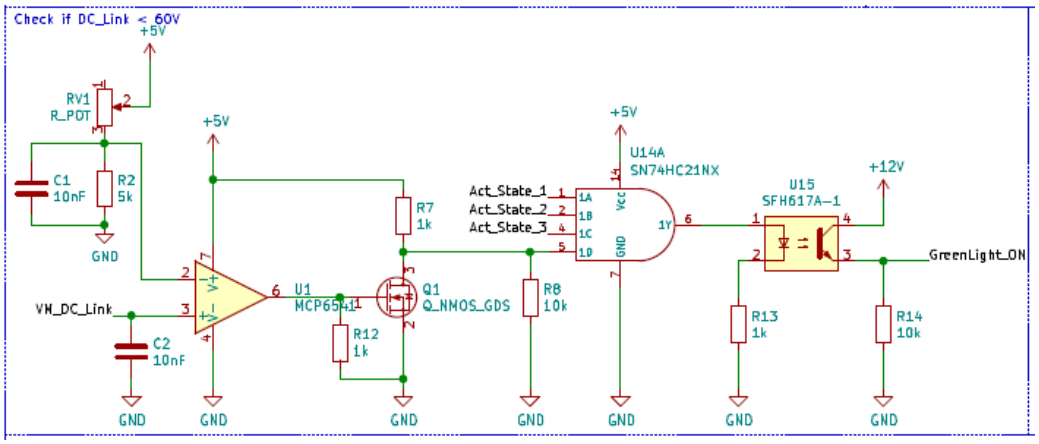
(**b**)

Figure 23. *Cont.*

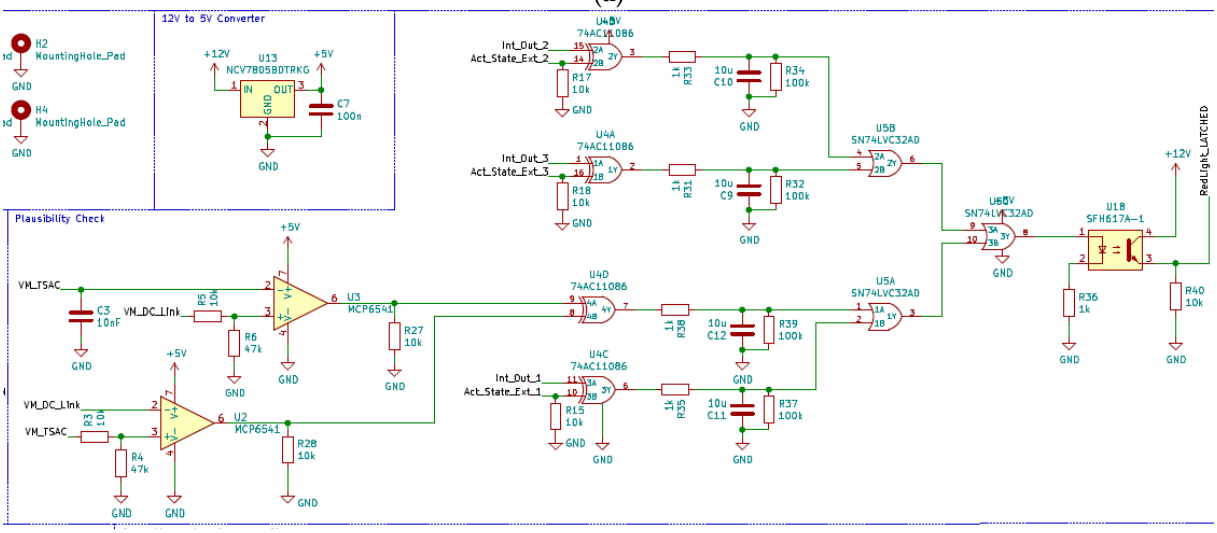


(**e**)

Figure 23. Main stages of the PDAL EC: (**a**) activation logic input, (**b**) capacitor charging and latching, (**c**) latching threshold calculation, (**d**) turn off threshold calculation, and (**e**) DC-link voltage comparison with the battery voltage.



(**a**)



(**b**)

Figure 24. Main stages of the TSAL EC: (**a**) Green light control and (**b**) plausibility check.

3.4. TSAL

The detailed schematic of the TSAL EC is provided in the Supplementary Files of this paper. The top left part of the circuit receives the actual states of the AIRs at connectors J4 and J6 which are connected to the auxiliary contacts of the AIRs. The intentional states of the AIRs, generated by the PDAL circuit, are connected to connector J8. The TSAL also needs information about the dc-link and accumulator voltages as well as the status of the SD line. The TSAL outputs the control signals for the red and green LEDs at J2 and J3 respectively. The main stages of the TSAL circuit are explained in the following subsections.

3.4.1. Green Light Control

The control signal will be activated only if the three AIRs are off, and the dc-link voltage is below the threshold (60 V in this case). This is to guarantee that there is no HV present outside of the accumulator box and turn on the green light accordingly. As shown in Figure 24a, the optocoupler U15 will be activated with output voltage $\approx$ 12 V when the output of the AND gate U14A at pin 6 is high. This is achieved when the outputs of the AIRs actual states, indicating AIRs are off, and the voltage comparison at U1, indicating no HV presence, are all high. If any of these four conditions are violated, the green light control signal will be low ($\approx$0 V).

3.4.2. Red Light Control

The plausibility check in Figure 24b is designed to achieve the truth table in Table 2.

If this part senses any implausibility between the actual and the intended states of the AIRs, the red light will be turned on and latched until the ESOs checks the issue.

3.4.3. Green and Red Lights Power Stage

Finally, this part will convert the control signals to the power signals with the suitable currents to power the LEDs. Relay K_2 will latch the red light on and report the error to the SSD circuit in case of any implausibility while K_1 switches the lights between green and red during normal operation.

3.5. PDB

As shown in the schematic in Figure 25, the control signal for the PDB is connected to pin 2 at connector J2. This can be either a manual signal in the cockpit where the driver can turn the system on and off or it can be an automatic signal connected to the MC. The automatic signal can be programmed by the MC STM32 software where the voltage becomes high when a certain temperature is exceeded. When the motor's temperature exceeds the threshold, which was set to 45°, the U2 optocoupler will be activated and turn the n-type MOSFET Q1 on. Accordingly, the relay K_1 will be turned on and hence the power will be flow from the TS to the LV system.

3.6. ECU

The ECU, which its schematic is provided in the Supplementary Files, is designed to interface the signals from the APPS, BS, RTD button, and the Buzzer to the Nucleo-F303RE µC. The ECU will also interface the output signals of the µC at 5 V to the rest of the LVCS at usually 12 V. The signals of APPS1, APPS2, and BS potentiometers are connected to the analogue inputs A0, A1, and A2 of the µC. MOSFETS Q1 and Q2 are used to power the brake light at the back of the FSERC and the Buzzer at 12 V. Optocouplers U4-U5 are used to convert the 5V digital outputs from the µC to the 12V RFE, BTB, RUN, and pulse-width modulation (PWM) signals required to operate the MC [13]. The ECU also interfaces the controller area network (CAN)-bus which is a good option to control and get useful data from the MC about the speed, torque, voltage. . .etc. The ECU has several LEDs and test points that are needed for monitoring and troubleshooting.

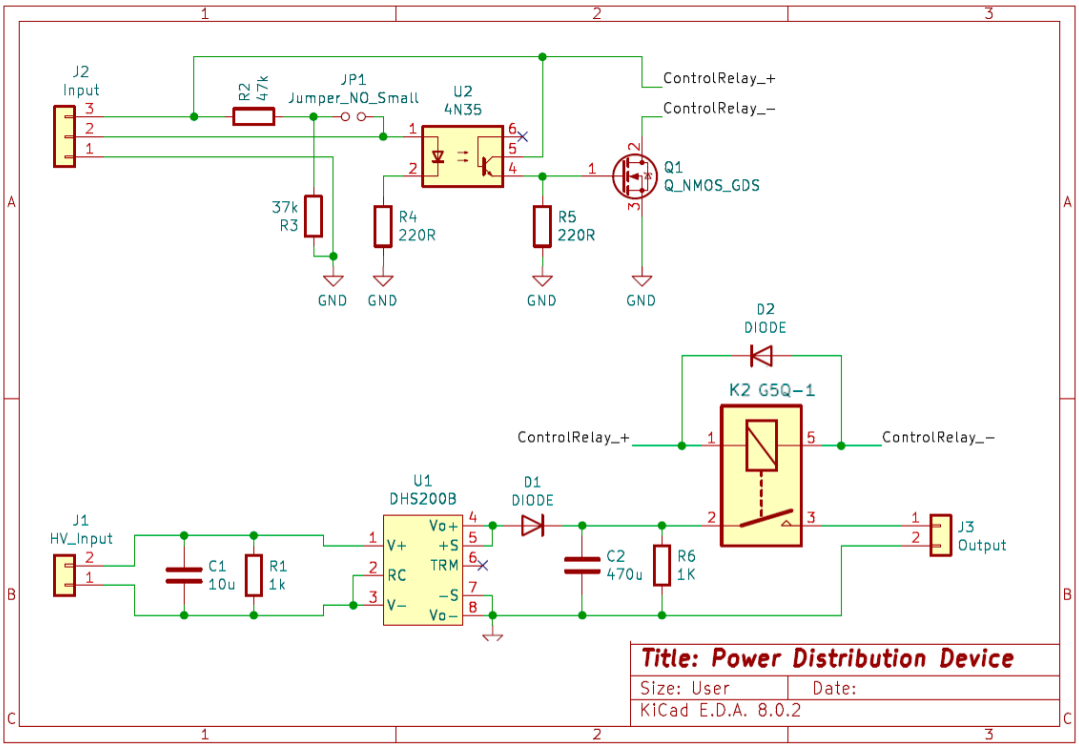


Figure 25. PDB EC.

4. Operating Instructions

The designs in the schematics presented in Section 3 are converted to Gerber format files using the KiCad® software so the PCBs can be manufactured and operated.

4.1. BSPD

The BSPD PCB are shown in Figure 26. The circuit is powered by the 12 V rail and then it supplies the integrated circuits (ICs) through a 12 V-to-5 V regulator. It should be noted that the traces connected to the K1 relay's contact should be designed according to the value of the SD line current required to energise the coils of the AIRs and the pre-charge relay. The main electronic components required to build the circuit are listed in Table 3.

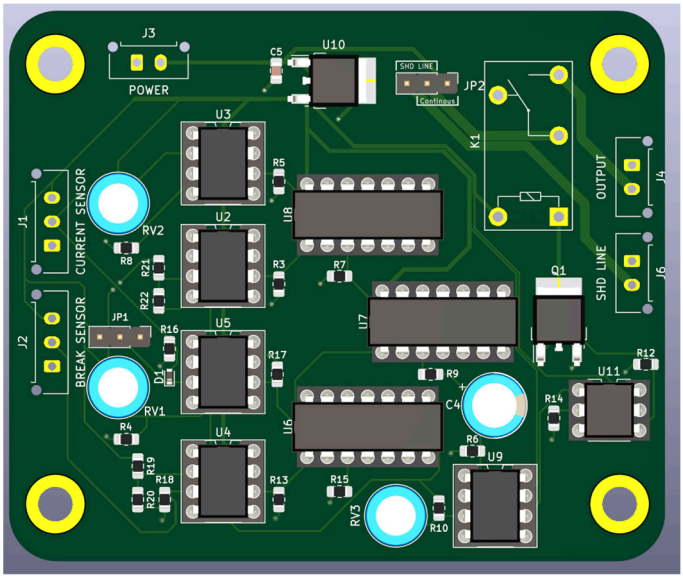


Figure 26. BSPD PCB.

Table 3. Main components of the BSPD EC.

Component	Part No.	Description
U2, U3, U4, U5, U9	MCP6541	Push-Pull Output Sub-Microamp Comparators
U7 and U8	SN54HC32	4-channel, 2-input 2–6 V OR gate
U6	TC74HC08A	Quad 2-Input AND Gate
U11	4N35	Optocoupler with Phototransistor Output
Q1	PJA3404	30 V N-Channel Enhancement Mode MOSFET
K1	653-G5Q-1A-HADC12	General Purpose PCB Power Relay Mini 1-pole 10A

4.2. SSD

The SSD PCB are shown in Figure 27. The circuit is powered by 12 V from the LV input. The push-release reset button is connected in series with the shoulder input. The three control signals for the IMD, AMS, and BSPD are fed from the signal connector at the left. The LEDs on the PCBs are added to inform about which stage is faulty. The electronic components required to build the circuit are listed in Table 4.

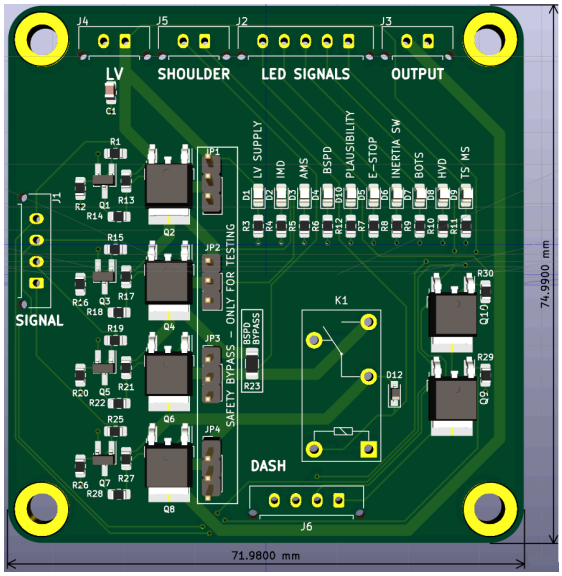


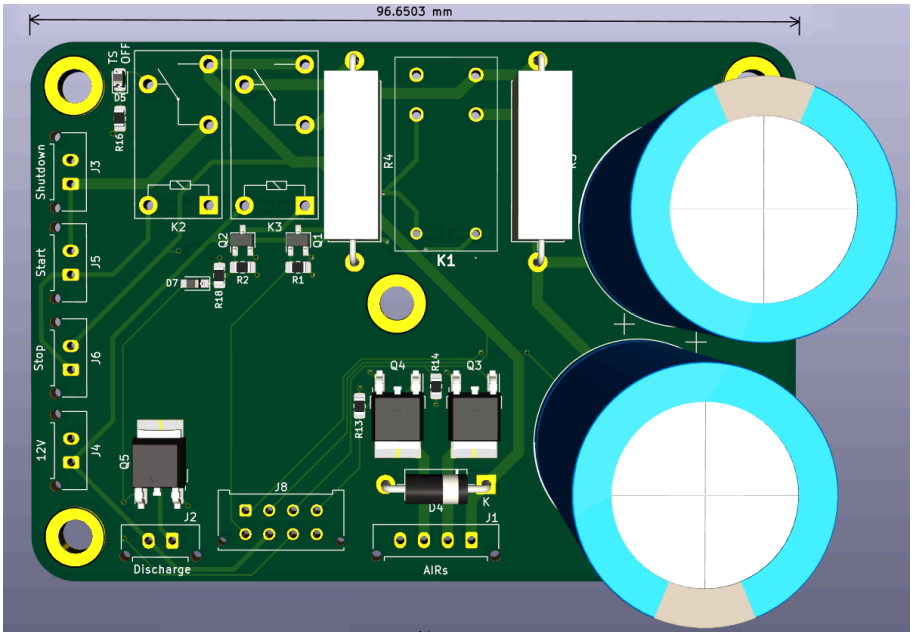
Figure 27. SSD PCB.

Table 4. Main components of the SSD EC.

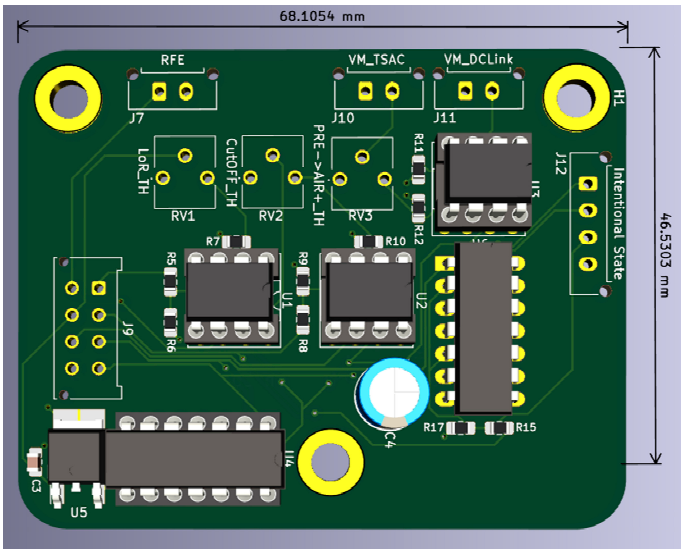
Component	Part No.	Description
Q1, Q3, Q5,Q7	MMBT3904VL	NPN switching transistor
Q2, Q4, Q6, Q8	RSD160P05	45 V Drive P-channel MOSFET
Q9,Q10	H6327	P-Ch −20 V MOSFET −630 mA
K1	653-G5Q-1A-HADC12	General Purpose PCB Relay Mini 1-pole 10 A

4.3. PDAL

The PDAL PCB are shown in Figure 28. The bottom part has the comparators and logic gates while the top part has the parallel capacitors and latching relays. The connection between the two parts is made possible using wires soldered at the back of the top part and the front of the bottom part. The main electronic components required to build the circuit are listed in Table 5.



(**a**)



(**b**)

Figure 28. PDAL PCB: (**a**) top part and (**b**) bottom part.

Table 5. Main components of the PDAL EC.

Component	Part No.	Description
K1	OSA-SH-224DM	General Purpose PCB Relay
K2, K3	653-G5Q-1A-HADC12	General Purpose Power Relay Mini 1-pole 10 A
Q1–Q5	PJA3404	30 V N-Channel Enhancement Mode MOSFET
U1–U4	MCP6541	Push-Pull Output Sub-Microamp Comparators
U5	LT1086CT-12	Low Dropout Positive 12 V/5 V Regulator
U6	TC74HC08A	QUAD 2-INPUT AND GATE

4.4. TSAL

The front and back of the TSAL PCB are shown in Figure 29. The main electronic components required to build the circuit are listed in Table 6.

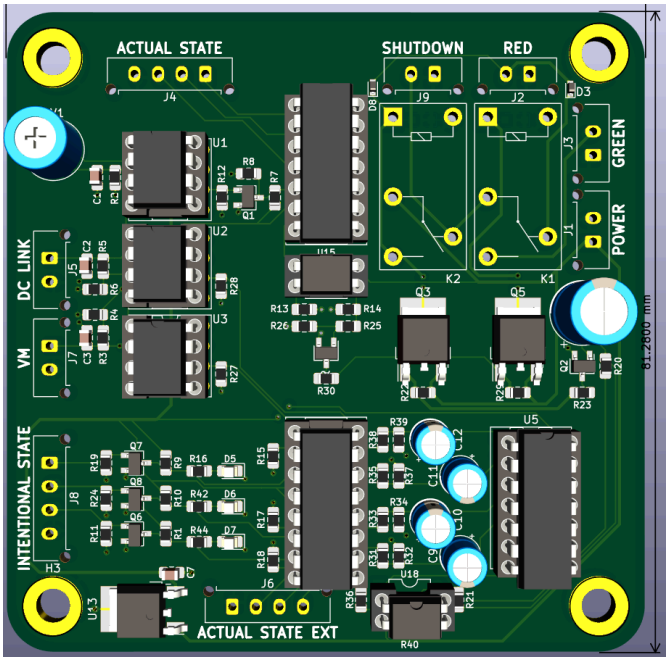


Figure 29. TSAL PCB.

Table 6. Main components of the TSAL EC.

Component	Part No.	Description
U15, U18	SFH617A	Phototransistor Output Optocoupler, Through Hole, 4-Pin DIP
K1, K2	653-G5Q-1A-HADC12	General Purpose Power Relay Mini 1-pole 10 A
Q1, Q2, Q4, Q6, Q7, Q8	PJA3404	30 V N-Channel Enhancement Mode MOSFET
Q3, Q5	RSD160P05	45 V Drive P-channel MOSFET
U1–U3	MCP6541	Push-Pull Output Sub-Microamp Comparators
U13	NCV7805BDTRKG	Linear Voltage Regulator 700 mA, 5 V
U6	SN74HC08N	Dual 4-Input AND Gate

4.5. PDB

The front and back of the TSAL PCB are shown in Figure 30. The main electronic components required to build the circuit are listed in Table 7.

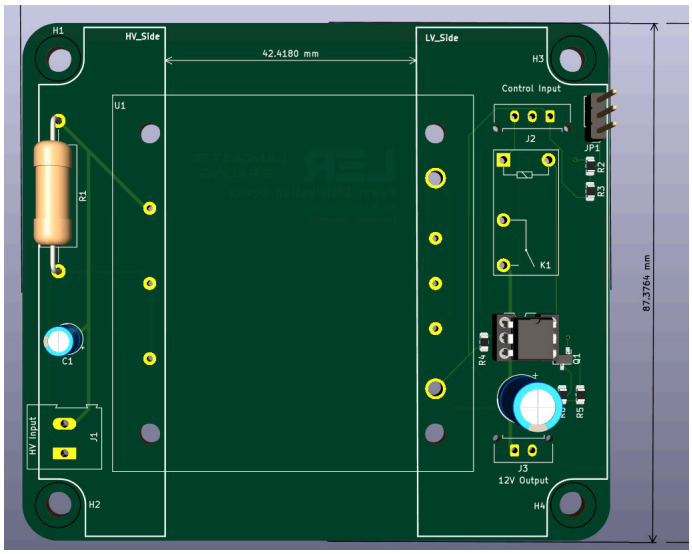


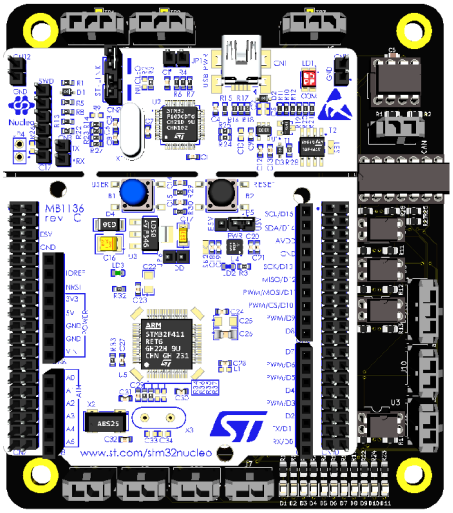
Figure 30. PDB PCB.

Table 7. Main components of the PDB EC.

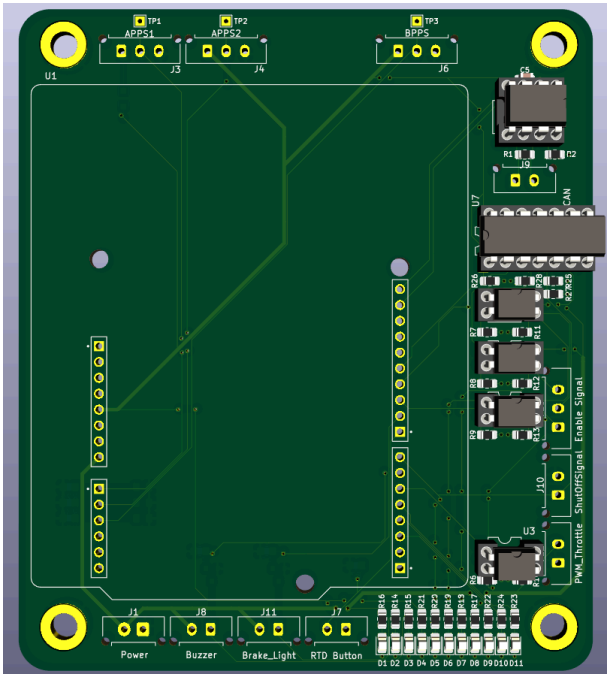
Component	Part No.	Description
K1	653-G5Q-1A-HADC12	General Purpose Power Relay 1-pole 10 A
U1	DHS250B15	400 V/12 V Isolated DC-DC Converter
U2	4N35	Phototransistor Optocoupler

4.6. ECU

Figure 31 shows the final design for the ECU circuit where the board was designed to allow either an Arduino Uno R3 or the Nucleo Board to be mounted with space in the top side to allow a connector to be plugged in while mounted on the PCB. The two µCs have been chosen because they both shave the same analogue and digital inputs and outputs. The components were placed in a way to minimise the size of the board as the Arduino and Nucleo boards are already quite big, restricting the minimum size of the board. The main electronic components required to build the circuit are listed in Table 8.



(**a**)



(**b**)

Figure 31. ECU: (**a**) PCB with Nucleo-F303RE Board and (**b**) without the MC.

Table 8. Main components of the ECU EC.

Component	Part No.	Description
U1	F303RE	STM32F303RET6 microcontroller 3.6 V—72 MHz—51 GPIO
U2	MCP2551-I/SN	CAN Transceiver 1Mbps, 8-Pin
U3, U4, U5, U6	EL817	4 PIN DIP PHOTOTRANSISTOR PHOTOCOUPLER
U7	TC74HC08A	Quad 2-Input AND Gate
Q1, Q2	PJA3404	30 V N-Channel Enhancement Mode MOSFET

5. Validation

To validate the LVCS, the different PCBs are connected to each other with the system as shown in Figure 32. Several tests are conducted to show the operation of the ECs when they are integrated together.

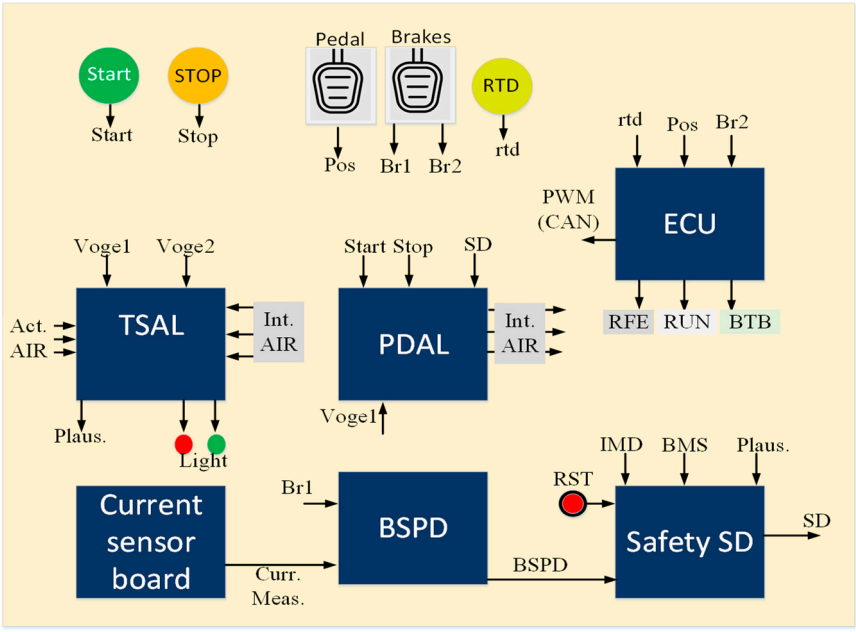


Figure 32. Block diagram of the LVCS connection.

5.1. BSPD

The operation of the BSPD is shown in Figure 33 when it was connected to the brake current sensor. In the top graph, the dc-link current was controlled to be around 15 A when the AIRs are closed. The second graph shows the brake signals when they are pressed two times at t_1 = 2.2 s and t_2 = 5.1 s. As shown in the third graph, the driver released the brake before the RC delay circuit voltage reaches the threshold which is set by the voltage divider to be around 2.8 V. In the second time, the driver kept the brake pressed for longer than the allowed period which is set to 300 ms and hence the coils of relay K1 are de-energised leading the SD line voltage in the bottom graph to be zero which will need to be restarted and the ESO to recycle the power.

5.2. SSD

Figure 34 shows the operation of the SSD when it starts without errors and therefore all control signals are high (≈12 V). The IMD error is simulated at t_1 = 2.1 s by disconnecting the control signal and therefore the output voltage of the SSD EC falls to 0 V. The IMD error was cleared at t_2 = 4.2 s but the output voltage of the SSD will not go to 12 V until the ESO reset the SSD manually at t_3 = 4.95 s. The SSD will then be active until another error happens.

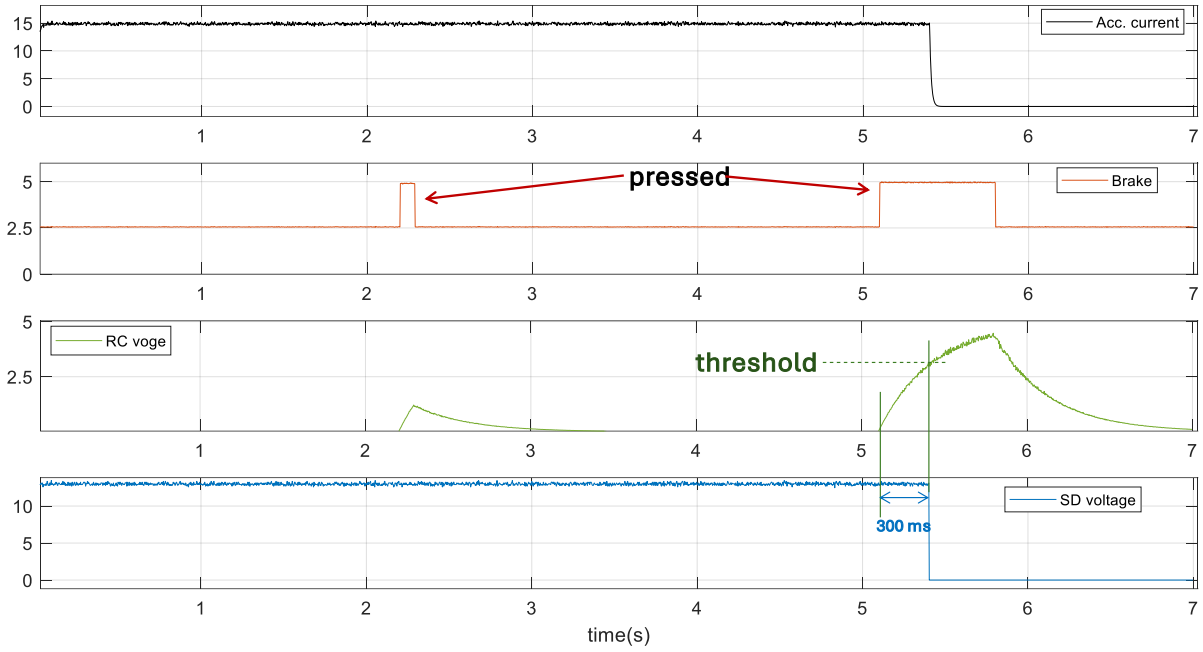


Figure 33. BSPD test.

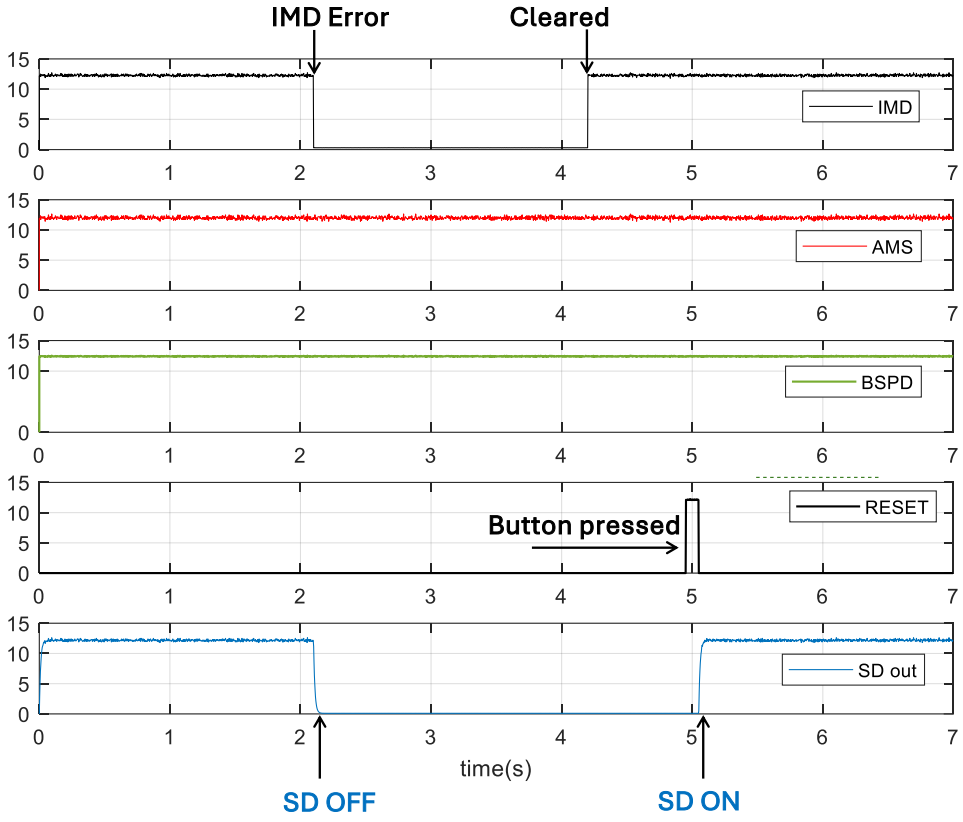


Figure 34. SSD test.

5.3. PDAL

Two tests have been conducted to check the performance of the PDAL and ensure proper turning on and off for the TS. During this test, the FSERC was lifted up and the LV box was opened to check the LEDs in the SSD and PDAL ECs.

5.3.1. Turning the TS on

The dc-link starts from 0V as all AIRs are open and the dc-link capacitor is discharged by the discharge relay. As shown in Figure 35, the SD line is turned on by the SSD circuit at t_o = 0 s. The driver then presses the start button at t_1 = 1.96 s and therefore the parallel capacitors' (C_1 and C_2) voltage starts to increase gradually through R_3 in the PDAL EC. When their voltage (V_{cap}) exceeds the threshold (10 V in this test) at t_2 = 2.41 s, AIR_1 is turned on connecting the negative pole of the accumulator to the dc-link. The pre-charge relay is turned on at the same time, so the dc-link capacitor is charged. At this moment, the RFE signal is sent to the MC to inform it that the TS is about to turn on. Once the pre-charge stage is finished at t_3 = 3.42 s, AIR_2 turns on to connect the positive pole of the accumulator to the dc-link. Thus, the TS is on and the FSERC is ready to enter the ready-to-drive mode. It should be noted that from t_2, the SD line is connected directly to the capacitors C_1 & C_2 as R3 is shorted by K_1.

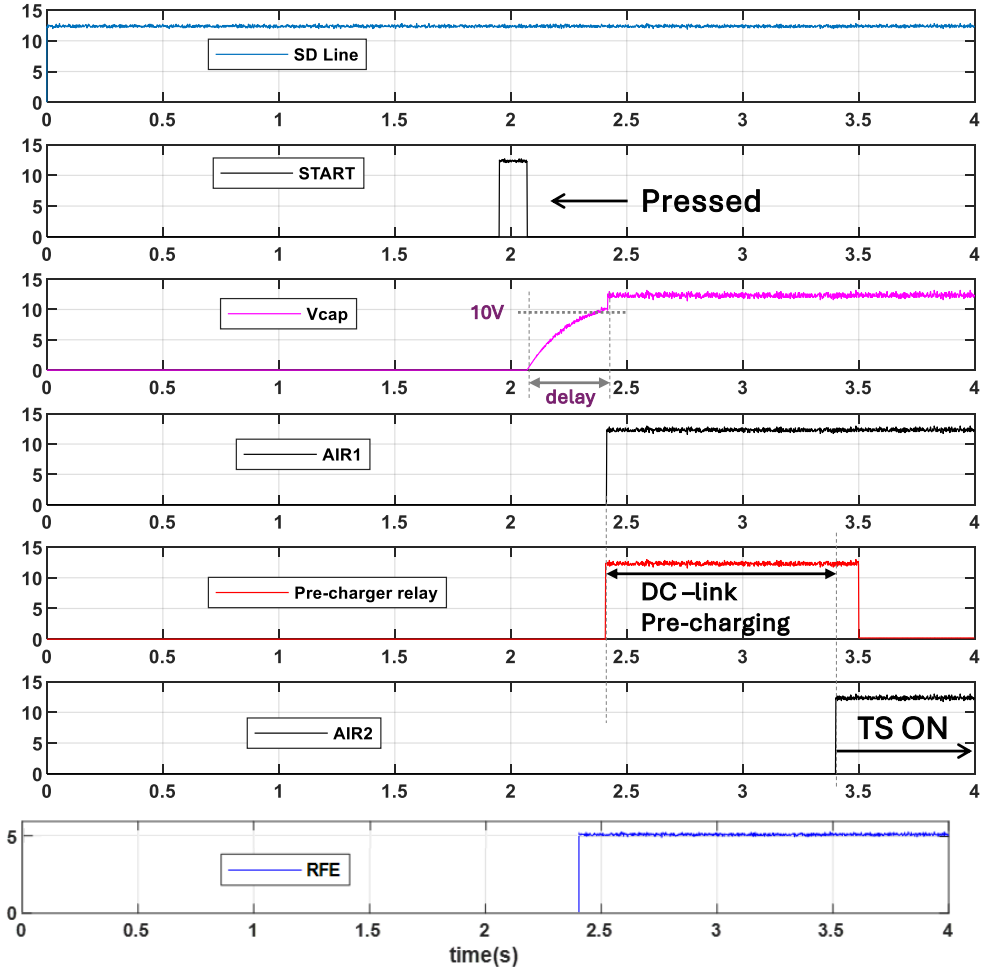


Figure 35. PDAL test during turning on the TS.

5.3.2. Turning the TS off

In Figure 36, the driver pressed the stop button at t_1 = 2.2 s to command the TS to be turned off. Shortly after t_1, the RFE signal becomes low to inform the MC that the TS is turning off soon. The parallel capacitors C_1 & C_2 starts to discharge in the coils of AIR1 and AIR2 which are measured to be ≈12 Ω each. The voltage of the capacitors continues to decrease until it reaches the pre-set threshold (2.7 V in this test) at t_2 = 2.52 s. The threshold can be adjusted by the voltage divider circuit connected to the comparator U2 in Figure 24d. This is important to set the time delay between t_2 and t_1 which is required to protect the MC. The values of the resistors in the voltage divider circuit were chosen to keep the delay

around 280 ms in this test. From t_2, the TS is off, and the discharge resistor will be connected in parallel with the dc-link capacitor to discharge it in less than 5 s. The TS is then ready for a new cycle.

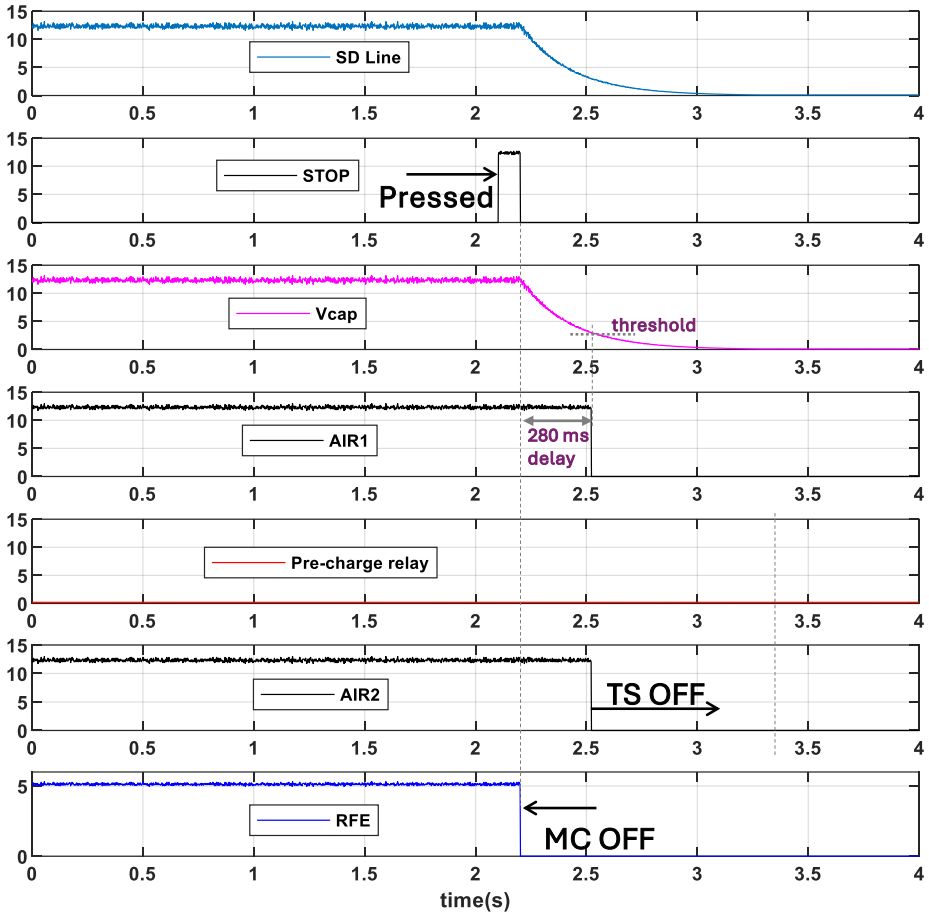


Figure 36. PDAL test during turning off the TS.

5.3.3. TS off Due to an SD Line Error

The action of disconnecting the TS due to an error in the SD line is tested when the AMS error is performed deliberately by disconnecting one of the temperature measurement sensors. As shown in the top graph in Figure 37, the AMS senses the error and therefore its output voltage falls to 0 V at t = 1.2 s causing the SD capacitors to start the discharge process as shown in the second plot. At the same instance, the PDAL EC informs the MC to turn off the enable signal to the PMSM rotating magnetic field as required. After a delay of 280 ms, the two contactors AIR 1 and AIR 2 are turned off so the TS is turned off. The AMS indicator LED in the SSD EC, shown in Figure 27, is turned off to help the team members with troubleshooting the problem caused by losing the temperature sensor.

5.4. TSAL

The performance of the TSAL was tested firstly on the bench with manual switches mimicking the inputs and outputs. Then, the operation has been tested by visual inspection during real operation as shown in Figure 38 to ensure that it fulfils the requirements in Table 1. The TSAL plays an important role in informing the drivers and ESOs about the status of the TS and therefore it a redundant small 12 V battery was added in parallel to the main LVB. It should be noted that the beacon is able to change the frequency of the red flasher internally. However, if a flasher beacon is not available in the market, the output of the TSAL circuit should be modified with a PWM controller to adjust the frequency of the red light. This controller can be added after relay K_1 in the TSAL circuit.

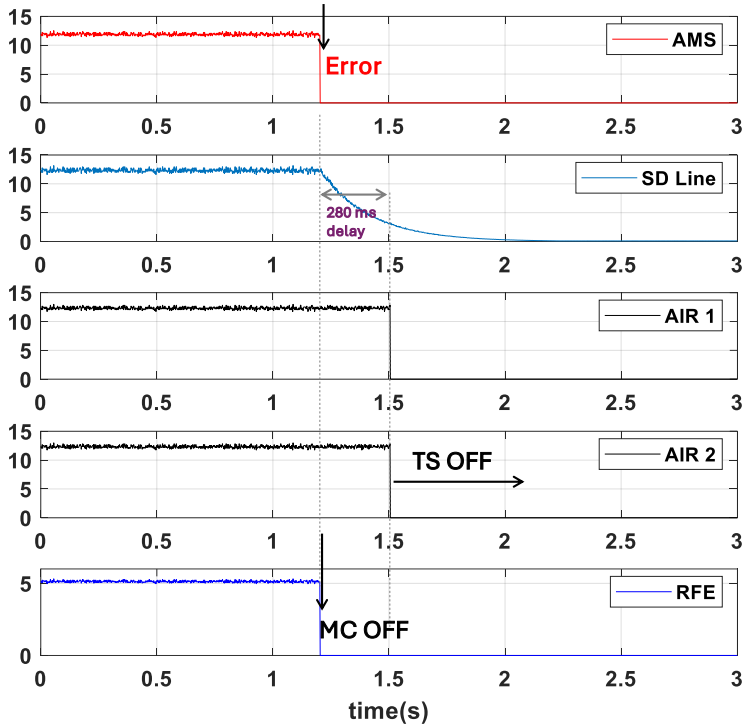


Figure 37. PDAL trips the TS due to an AMS error.

Figure 38. TSAL green and red lights inspection.

5.5. LVB

With the LVCS turned on, Figure 39 shows the voltage, current, and the state of charge (SoC) of the 50 Ah LVB supplying the whole system. The results were recorded when the LVMS is turned on when the SoC of the LVB is 80% and the terminal voltage is 12.8 V. For the first 30 min, the TS is turned off and hence the drawn current supplies the LVCS excluding the AIRs. Then, the TS is turned on via the AIRs and therefore the LVB current increases from 1.13 A to 3.275 A. The LVB is keep operating at this discharge rate for 2 h, so its SoC is reduced to 70% with a drop in the terminal voltage to 12.4 V. The LVB will reach SoC = 20% after 8 h of operation and hence the terminal voltage will decrease to 11.4 V. The tolerance voltages of the LVCS components, including voltage regulators, comparators,

switches, and relays' coils, are selected so they can function at voltages below the minimum expected LVB of 11.4 V.

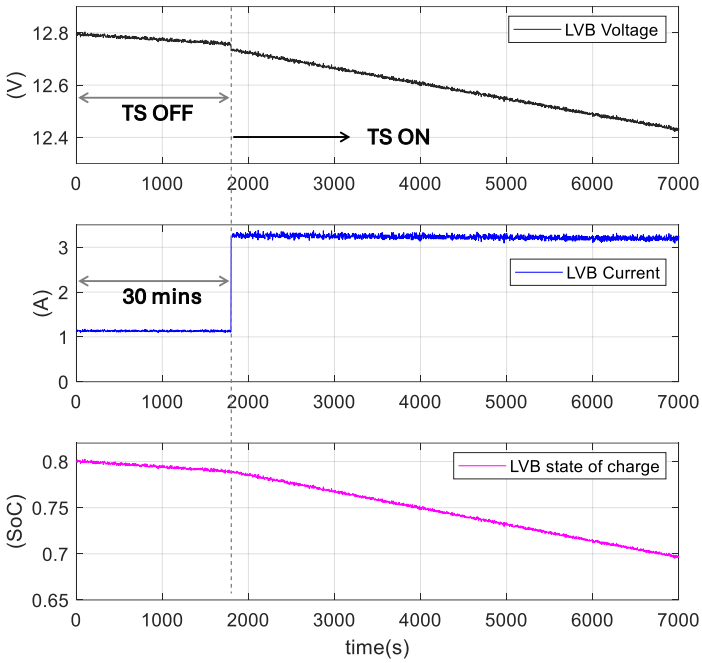


Figure 39. LVB discharge.

5.6. PDB

The PDB EC plays an important role in saving the LVB energy to ensure the operation presented in Section 5.5 and Figure 39. The operation of the PDB is shown in Figure 40 where the PMSM starts from standstill at a temperature of around 27.5 °C. As shown in the bottom graph, the temperature increases until it reaches 45 °C at around 9.6 min of operation at the top speed. When this threshold temperature is reached, the opto-coupler U2 in the PDB EC, shown in Figure 25, is turned on activating the pump and fans system. Thus, rate of temperature rise is reduced until it settles at a value in the range of 50 °C to 60 °C. It is worth noting that the maximum value in the MC program is set to 60 °C before beyond which the MC will stop the process.

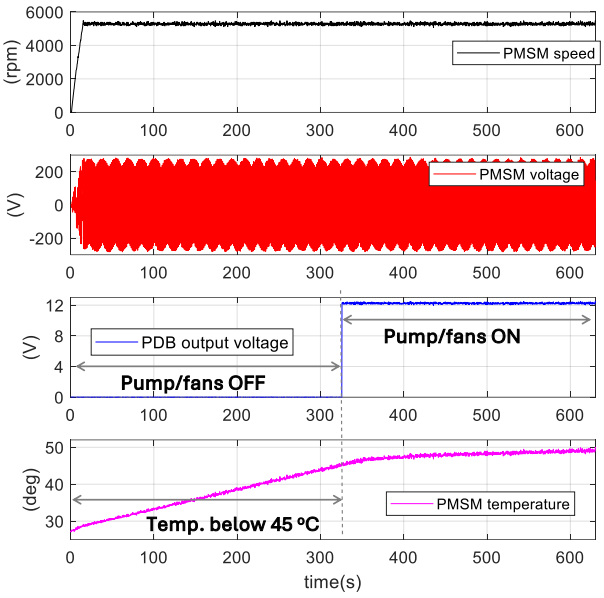


Figure 40. PDB EC activation.

6. Conclusions

The paper presented the design of the LVCS which controls the racing car built by the 2022 LER team. The system is designed to fulfil the IMechE rules, that are put in place to ensure the safety of the operation, and to improve the performance of the FSERC. The LVCS operates mainly at 12 V and supplied from a relatively small LVB which is crucial in satisfying the functionality and the durability conditions. One of the main goals achieved by the LVCS in this work is to minimise the current, and hence the power, absorbed by the LVB so the operational time can be extended. The ECs are designed to be as simple as possible in order to ease their troubleshooting and maintenance processes without compromising the safety regulations. All ECs are equipped with accessible monitoring LEDs to help in identifying the source of faults when they occur. The paper presented a discussion on the effect of the ECs on the performance of the car during acceleration, top-speed operation and during braking using the PMSM model, mathematical analysis, and computer simulations, showing the relation between the hard braking torque and the HV battery power. The ECs are designed so the major functions affecting the safety of the FSERC are fail-safe meaning that the TS will be disconnected and de-energised when any of the components fails, is removed, or damaged. It was taken into consideration that the FS projects usually have limited budgets and hence most of the employed devices in the system are chosen as standard components that are available in the market at reasonable cost. The LVCS have been tested on bench and during operation where experimental results have been provided to show the performance of the circuits.

Supplementary Materials: The following supporting information can be downloaded at: https://www.mdpi.com/article/10.3390/hardware2030010/s1.

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Conflicts of Interest: The authors declare no conflict of interest.

Nomenclature

AMS	Accumulator Management System	**LVB**	Low Voltage Battery
APPS	Accelerator Pedal Position Sensor	**LVCS**	Low Voltage Control System
BMS	Battery Management System	**LVMS**	Low Voltage Master Switch
BOTS	Brake Over-Travel Switch	**PCB**	Printed Circuit Board

BSPD	Brake System Plausibility Device	**PDAL**	Pre-charge Discharge Activation Logic
BPPS	Brake Pedal Position Sensor	**PDB**	Power Distribution Board
EC	Electronic Circuit	**PMSM**	Permanent Magnet Synchronous Motor
ECU	Electronic Control Unit	**SD**	Shutdown
FSERC	Formula Student Electric Racing Car	**TS**	Tractive System
HV	High Voltage	**TSMS**	Tractive System Master Switch
HVD	High Voltage Disconnect	**TSAL**	Tractive System Active Light
IMD	Insulation Monitoring Device		

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