Defect formation in InGaAs/AlSb/InAs memory devices

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(Dated: 8 May 2023)

ABSTRACT
ULTRA**RAM**^{TM} is a novel floating-gate nonvolatile memory in which the oxide barrier of flash is replaced by a triple-barrier resonant tunneling structure comprising of multiple InAs/AlSb heterojunctions. The quality of the triple barrier resonant tunneling heterostructure of a ULTRA**RAM**^{TM} device in terms of interface sharpness and presence of defects was analysed by cross-sectional scanning tunneling microscopy. We observed two different types of defects: stacking faults originating in the layers below the triple barrier resonant tunneling structure and AlSb accumulations at the interface between the lower AlSb layer of the triple barrier resonant tunneling and the InGaAs channel. The InGaAs surface of a second sample was measured by atomic force microscopy in order to investigate whether its unevenness is caused by the deposition of the AlSb layer or already present before the AlSb deposition process.

Keywords: Cross-sectional scanning tunneling microscopy, ULTRA**RAM**^{TM}, III-Sb semiconductors, growth defects

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I. INTRODUCTION

A universal memory, long considered the "holy grail' of computing, should combine the best aspects of dynamic random-access memory (DRAM) and flash[?] . Fundamentally, such a technology must have very robust logic states that can, nevertheless, be easily changed. As the nature of these requirements appears paradoxical, the widely accepted view is that universal memory is unfeasible[?] or almost impossible[?] . ULTRA**RAM**^{TM} is a novel, III-V compound semiconductor memory which has demonstrated many impressive properties which are suggestive of a universal memory candidate. Namely, non-volatility, ultra-low switching energy (per unit area)[? ? ?] and fast switching speed with compact architecture (modelled)[?] . ULTRA**RAM** is a III-V semiconductor floating-gate memory grown by molecular beam epitaxy (MBE) that exploits the InAs/AlSb 2.1 eV conduction band off-set to trap charge.[?] . A triple barrier resonant tunneling (TBRT) structure contained within the epitaxial crystal, between the channel and the floating gate (FG), is formed by multiple InAs/AlSb heterojunctions, specifically by two InAs quantum wells (QWs) sandwiched between three AlSb barriers. In the absence of a bias, electrons are trapped either in the floating gate or in the channel[?] . Electrons are allowed to move across the TBRT by the application of a suitable bias ($\pm 2.5V$) that causes the QWs energy levels to align with the occupied states of the channel (program cycle) or the floating gate (erase cycle)[? ?] . Detailed information on the ULTRA**RAM** device and how it works can be found in Ref. 4 and 8.

ULTRA**RAM** device performance clearly depends on the TBRT, the channel and the FG layers. Ideally, these layers should have extremely sharp interfaces and uniform thicknesses at the atomic level. To investigate whether the quality of the grown layers is close to the ideal one we need a characterization technique able to probe the material with atomic resolution, such as scanning tunneling microscopy (STM).

FIG. 1. Schematic structure of ULTRA**RAM** sample A.

STM is a powerful technique that allows the imaging of a surface at the atomic level. In particular, cross-sectional scanning tunneling microscopy (X-STM) allows us to analyse the grown layers within a semiconductor material[?] . The cross-section of a sample can be probed in order to gain significant information on its electronic and structural properties such as interface quality and presence of defects.

In this work, we present the result of an X-STM analysis on an ULTRA**RAM** sample. The quality of the layers in terms of interfaces sharpness, thickness and composition uniformity was probed, with particular focus on the TBRT structure and the adjacent layers, i.e. a 20 nm thick GaSb layer, the $In_{0.8}Ga_{0.2}As$ channel and the InAs floating gate (Figure 1). We observed that the thin TBRT layers have relatively rough interfaces mostly due to their discrete atomic nature. In addition, the first AlSb barrier (B1) exhibits an unexpectedly irregular thickness due to the presence of top-down triangular shaped AlSb accumulation, which we refer to as nanoridges (NRs), located at the interface with the underlying InGaAs channel. Thus, the channel has an uneven thickness. We also observed the presence of stacking faults originating at the interfaces of the InGaAs channel with the underlying

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FIG. 2. 355 25 nm filled-state LT X-STM image of GaSb/InGaAs/TBRT, taken with a bias voltage V_b of -3 V and a tunneling current I_t of 50 pA. The bottom image is the continuation of the top one. The darker areas that can be seen in the TBRT structure are ripped out part of the layers due to the cleaving. On the right side of the bottom image the schematic structure of the layers is reported: the colours correspond with the different compositions as shown in Figure 1

GaSb layer. To investigate a possible mechanism of formation of the NRs, we analysed by atom force microscopy (AFM) the InGaAs channel top surface of a purposely grown sample. The AFM images also give us further insight on the tri-dimensional shape of the NRs. The relaxation profile of GaSb/InGaAs/TBRT obtained from the STM images was reproduced with finite element (FE) simulations based on continuum elasticity theory in order to investigate whether the InGaAs composition is compatible with the nominal one (group III composition of 80 % In and 20 % Ga).

II. RESULTS AND DISCUSSION

In the X-STM experiment, one of the {110} crystallographic planes of the sample is exposed by cleaving it *in situ*, in ultra high vacuum and analysed either at nitrogen temperature or room temperature (see section IV). A bias is applied between the sample and an atomically sharp tip which is scanned over the cleaved surface. The schematic structure of the analysed ULTRA**RAM** sample A is shown in Figure 1. Note that one bilayer corresponds to one lattice constant of approximately 6.1 Å. Every layer of the sample was analysed by X-STM. However, we will focus on the top part of the structure, namely, the 20 nm thick GaSb layer, the InGaAs channel, the TBRT layers and the InAs FG. The TBRT structure is formed by two InAs quantum wells, QW1 and QW2, respectively 5 bilayers (BL) and 4 BL thick, and three AlSb barriers (B1, B2 and B3). B1 and B3 have an intended thickness of 3 BL while B2 has an intended thickness of 2 BL. The target thickness of the $In_{0.8}Ga_{0.2}As$ channel and the InAs FG is, respectively, 20 BL and 16.5 BL. The InAs FG was never completely accessible to our STM analysis due to its proximity to the edge of the cleaved sample. Similarly, the complete imaging of the underlying GaSb layer was unfeasible due to the presence of several cleavage induced step-edges. A large scale overview of the GaSb/InGaAs/TBRT region is shown in Figure 2. The various layers, such as GaSb, InGaAs channel and TBRT layers, can be clearly distinguished from their difference in brightness. The bottom bright layer is the GaSb layer while the following dark layer is the InGaAs channel. The local variation in the contrast of the InGaAs layer is due to alloy fluctuation, where Ga-rich areas appear darker and In-rich ones appear brighter. Segregated Sb atoms in the InGaAs layer appear as bright dots. Sb segregation is mostly limited to the first few BL of the InGaAs layer. However, Sb atoms can be observed also in the middle of the InGaAs channel, around 10 BL from the GaSb/InGaAs interface.

The subsequent layers form the TBRT structure. The three bright layers are the AlSb barriers (B1-3) while the darker layers in between the barriers are the two InAs quantum wells (QW1 and QW2). In Figure 2, it can be observed that the thickness of B1 is relatively irregular due to the presence of triangular shaped AlSb accumulations at the bottom part of the first AlSb barrier, such as the ones highlighted by the white dashed rectangle in Figure 2. We refer to these features as nanoridges (NRs) due to their shape. NRs will be discussed with further detail in sections II B and II C. The irregularity of the first barrier is reflected in the InGaAs channel that similarly to B1 has an irregular thickness. In contrast, the thickness of the second and third barriers varies only slightly mostly due to the discrete atomic nature of interfaces. Rows of missing atoms can also be observed in Figure 2, in particular in the TBRT layers. Despite InAs and AlSb being closely lattice matched (1.3% lattice mismatch), the TBRT layers are nonetheless strained. Therefore, when the sample is cleaved, part of the layers can be ripped out due to the strain. These ripped out regions appear more frequent in our experiments than usual for an X-STM sample due to the presence of defects (see section II B).

The different layers of the structure can be observed in more detail in Figure 3a, where next to the X-STM image the schematic structure of the sample is reported. Here, the TBRT layers, with the exception of the first AlSb barrier, have the intended thickness. Again, the different layers can be clearly distinguished from the brightness variation. This is not only due to the difference in material but also due the relaxation of the cleaved surface[?]. In particular, the height profile of GaSb/InGaAs/TBRT (Figure 3b) taken in the STM image in Figure 3a shows that the AlSb barriers relax outwards further than the the InAs barriers due to the strain induced by the lattice mismatch. Therefore, the AlSb layers appear brighter because they will be closer to the STM tip. Similarly, the InGaAs layer is darker since it relaxes inwards. The GaSb/InGaAs/TBRT region was imaged over a relatively wide range of biases both at negative or a positive bias but no voltage dependence was observed and no additional information was gained.

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FIG. 3. a. 38 33 nm filled state LT X-STM image of the TBRT, V_b = -3 V, I_t = 50 pA; next to the image the schematic structure of the layers is indicated: the colours correspond with the different compositions as shwon in Figure 1. b. Height profile taken along the black line in Figure 3a and the simulated profile for 80% In relative concentrations. The coloured rectangles at the bottom of the graph indicate the different materials (see Figure 1).

A. Relaxation profile and X-ray diffraction characterization

In the height profile, the different layers, i.e, GaSb, InGaAs, the AlSb barriers, the QWs and the FG, can be distinguished (Figure 3b). From the profile, it can be seen that the Sb containing layers relax outwards while the In(Ga)As layers relax inwards, especially the channel. GaSb is taken as reference since the 500 nm GaSb layer (Figure 1) was grown to be fully relaxed by introducing an interfacial misfit (IMF) array between it and the GaAs substrate[?,?] as also as evidenced by the XRD data of Figure 4 In this way, the strain should be reduced within the first few monolayers from the interface[?]. Assuming perfect pseudomorphic growth, the in-plane lattice constant of all layers above the GaAs will be fixed at the GaSb lattice constant. Therefore, the AlSb barriers are compressively strained since AlSb has a bigger lattice constant than GaSb (0.61355 nm and 0.609593 nm, respectively). Contrarily, InAs and $In_{0.8}Ga_{0.2}As$ have smaller lattice constants (0.60583 nm and 0.5977 nm) than GaSb, therefore the In(Ga)As layers are tensile strained.
In order to fit the relaxation profile of GaSb/InGaAs/TBRT, FE simulations based on continuum elasticity theory are performed. One of the aims of the simulation is to establish whether the relative In and Ga concentrations in the channel of the analysed sample correspond to the nominal ones, i.e. 80 % In and 20 % Ga. In Figure 3b the X-STM profile is compared with the curve simulated for a relative In concentration of 80%. It can be seen that the simulated profile deviates slightly from the experimental. However, as we mentioned in II, the InGaAs layer exhibits alloy fluctuation. Therefore, the In concentration can be either lower or higher than the nominal one in different areas of the sample. Moreover, we observed that the experimental profile varies in different STM images. This is partly due to the electronic contribution to the STM images and to the presence of distinct defects in the various STM images. X-ray diffraction (XRD) measurements of the (004) reflection are shown in Figure 4, along with the results of a simulation to fit the experimental data. An optimal fit is achieved when assuming complete relaxation of the GaSb buffer layer relative to the underlying GaAs, indicating that an IMF array was successfully formed at the GaSb/GaAs interface. The only other layer to show a small $20 \pm 5\%$ relaxation in the XRD fitting was the 50 nm InAs layer, which is unsurprising as it is above the theoretical critical thickness[?] for InAs on GaSb. But for the purposes of the following analysis it is sufficient to assume that all In(Ga)As and AlSb layers are pseudomorphically strained relative to the GaSb lattice constant.

FIG. 4. XRD spectrum of the ULTRA**RAM**^{TM} sample A and corresponding simulation.

B. Growth defects

As previously mentioned, NRs form mostly in the first AlSb barrier at the interface with the InGaAs channel causing both B1 and the InGaAs channel to have an uneven thickness (Figure 2). Overall, a 2.3 ± 0.2 μm long stretch of the TBRT layers was measured and 96 NRs were visible with an average separation of 25 ± 4 nm. NRs have either an inverted triangular shape or a inverted trapezoidal shape. The average length of the top side of the NRs is 12 ± 4 nm. The height varies between 3 and 9 BL below the first AlSb barrier including its thickness. The average depth of the NRs is 3.8 ± 0.9 nm (6 ± 1 BL). When the NRs are higher than 6 BL, the formation of NRs was observed also in the AlSb layers B2 and B3. For instance, in Figure 2, the formation of a smaller NR in B2 stacked above the NP in B1 can be observed (red dashed rectangle). We suggest that the formation of NRs in B2 and B3 is caused by strain induced nucleation, similarly to the stacking of quantum dots (QDs) first observed by Xie *et al.*[?]. Differently, in the case of the smaller NRs, B2 and B3 generally show sharp interfaces and a greater constant thickness. This is due to the fact that the formation of a flat surface is energetically favoured during deposition.
The NRs result in a locally thicker AlSb barrier. Electrons will have greater difficulty to tunnel through "thick" NRs than through a "thin" AlSb barrier with the expected thickness (3 BL). However, at the side the NRs, the AlSb barriers are typically of the designed thickness or slightly thinner, i.e. 2 BL or

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1 BL instead of 3 BL. Electrons with the appropriate energy prefer to tunnel through the thinner parts of the barrier at the sides of the NRs. Due to the local variation of the first AlSb barrier and occasionally the first InAs QWs, we expect that local electronic properties of the material will be influenced. However, we anticipate that the device characteristics will not be affected to a significant extent as current will mainly flow through the parts of the TBRT next to the NRs. Ref. 8 shows that TBRT function is quite robust to BL fluctuations in thickness, where B1 is thicker due to a NR.
Moreover, the NRs size (i.e. 12 ± 4 nm) is virtually negligible compared to the device dimensions (i.e 10-20 $\mu m^?$). Despite the relatively high concentration of NRs, the parts of TBRT with intended layer thickness will be dominant. Thus, we expect the presence of the NRs to have little effect on the device characteristics.
A second type of feature that was observed in the ULTRA**RAM** heterostructure are stacking faults. A stacking fault is a planar defects that can form during the growth of a crystal. Stacking faults are caused by an local interruption in the stacking sequence of the atoms[?]. For example in a face-centred cubic (FCC) crystal, the stacking sequence ABCABC... becomes ABCBCAB... when a (-111) plane is removed from the structure. In this case, an intrinsic stacking fault is formed. Alternatively, an extrinsic stacking fault with ABCBABC... stacking sequence forms if an additional (-111) plane is introduced in the crystal structure[?]. Examples of stacking faults observed in sample A are shown in Figure 5a, highlighted by red dashed rectangles. In Figure 5b an example of thin twins is displayed. A thin twin forms when an intrinsic stacking fault occurs on every (-111) plane of the crystal[?]. The formation of a thin twin in the ULTRA**RAM** sample was observed in three different images. The twins we observed in the sample have similar characteristics to the stacking faults, therefore the stacking faults description in the next paragraph applies as well to the twins.
The stacking faults originate at the interface between the InGaAs channel and the underlying GaSb layer despite this interface being particularly sharp. The formation of the stacking faults is due to the lattice mismatch between the two materials (-2.0%). The stacking faults always appear as diagonal features across the layers with an angle of about $\pm 45^o$ with respect to the growth direction. Since we are measuring one of the $\{110\}$ crystallographic planes, we can establish that the stacking faults run along one of the $\{111\}$ crystallographic planes. Indeed, as previously mentioned, stacking faults typically form on $\{111\}$ planes in crystals with a FCC structure and this is due to the fact that $\{111\}$ planes have the lowest stacking fault energy[?].

In total, 38 stacking faults with an average distance of 62 $\pm$ 14 nm were found. 21 of the stacking faults run along one of the $\{111\}$ crystallographic planes with a $+45^o$ angle while the other 17 have a -45° angle. 9 of the stacking faults ends at the bottom of a NR, similarly to the stacking fault in Figure 5a (red dashed rectangle) while the remaining 29 run also through the TBRT layers and terminate at the top surface of the sample. Also in this case, the stacking faults typically

FIG. 5. a. Filled-state LT X-STM image, macro from the white dashed rectangle in Figure 2 V_b = -3 V, I_t = 50 pA. The two dashed rectangles highlight two stacking faults. One of the stacking faults terminates at the bottom of a NR (red). The other one ends with a ripped out line of atoms (orange). In the inset the structural model of the (110) surface is shown, with the stacking fault extending along the [-1 1 1] direction as in the STM image. The smaller atoms represent the subsurface atoms that are not visible in the STM image b. Filled-state LT X-STM image showing a case of twinning and the corresponding structural model in the inset.

correspond to the presence of an NRs. However, NRs also form in the absence of a stacking fault. Indeed, the number of NRs (96) is more than twice the number of stacking faults. However, we believe that there is a relation between the stacking faults and the presence of NRs.
Occasionally, a stacking fault favoured the ripping off of atoms when the sample was cleaved, as it increases the strain in the structure. In Figure 5a it can be seen that the ripped off part of the layers correspond to the stacking fault highlighted by the orange dashed rectangle. However, regions of ripped off material can be seen throughout the TBRT layers independently from the presence of a stacking fault since the TBRT structure is intrinsically strained.

C. AFM measurements of InGaAs surface

In order to determine whether the NRs form before or after the deposition of the first AlSb barrier, a new sample B was grown. The growth of sample B was terminated after the deposition of the InGaAs channel. The InGaAs surface was analysed by atomic force microscopy (AFM) as shown in Figure 6. Trenches in two different directions perpendicular to each other can be observed. One of the directions, however, appears to be favoured. We believe that these trenches on the InGaAs surface correspond to the termination of stacking faults inside the InGaAs layer. By counting the number of trenches (16) along the black dashed line in Figure 6b (1.1 $\pm$ 0.2 μm), we obtained a an average distance of 69 $\pm$ 18 nm, comparable with the one found from the STM images (62 $\pm$ 14 nm). However, the lateral extent of the ridges seen in the AFM measurements does not correspond with the average base length the NRs observed in the X-STM images. This is due to the oxidation of the InGaAs surface imaged by AFM and to the lower resolution of the AFM tip compared a STM tip.
In our opinion the trenches function as nucleation points for the formation of the NRs. When the first AlSb barrier is grown, Al and Sb fill up the ridges, flattening the surface and resulting in the features we observe in the X-STM images. In-

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deed, we observed that typically the upper interface of the first AlSb barrier is sharper, despite the presence of the NRs.
The AFM measurements gave us also deeper insight into the length and the 3-dimensional shape of the NRs. In the STM images, we observed a pyramidal or truncated pyramidal cross-section shape. However, the STM images do not allow the determination of the actual 3-dimensional shape of the NRs since STM is a surface technique, showing only perpendicular cross-sections of the NRs running in one of the two directions. The presence of trenches in the AFM images indicate the NRs have a elongated shape. Hence the denomination "nanoridges" of the structures we see in the X-STM images.

FIG. 6. a. 5 5 μm AFM image of the InGaAs surface of sample B. The dashed white rectangle correspond to Figure 6b. b.1 1 μm AFM image of the InGaAs surface.

III. CONCLUSIONS

We analysed an ULTRA**RAM** sample by X-STM and we observed the presence of growth defects in the upper layers of the sample, i.e. channel, TBRT structure and FG. We observed stacking faults originating at the lower interface of the InGaAs channel and triangular-shaped AlSb accumulations, or nanoridges, at the upper InGaAs interface. Almost all the stacking faults correspond to the formation of NR. Therefore we assumed there is a correlation between the stacking faults and the formation of NRs. From AFM measurement of the InGaAs surface of sample B, we observed the presence of trenches at the surface of this layer causing it to be uneven. We believe that the NRs form when the following AlSb layer is deposited. The deposition of the first AlSb flattens the surface and, as a result, the following TBRT layers have sharper interfaces and more uniform thickness. Despite the presence of growth defects, we do not expect the memory device performances to be significantly effected. Indeed, the formation of the NRs and consequent flattening of the subsequent TBRT layers can be seen as an advantageous self-correcting mechanism in the growth.
The ULTRA**RAM** sample A was characterized by XRD and the corresponding simulation was performed. The In(Ga)As and AlSb layers were assumed to be strained with respect to the GaSb buffer layer, which was considered to be completely relaxed. Similarly, the GaSb buffer layer was taken as reference in the FE simulation of the GaSb/InGaAs/TBRT relaxation profile. Therefore, the In(Ga)As layers are tensile strained while the AlSb barrier are compressively strained. The simulated profile deviate slightly form the experimental one partly due to electronic contribution to the X-STM image.

IV. METHODS AND MATERIALS

The sample's epilayers were deposited on a 2" GaAs n-type wafer by molecular beam epitaxy using a Veeco GENxplor system. Following thermal desorption of the native oxide a 500-nm GaAs buffer layer was deposited at 560^oC. The As cell was then closed for 10 s to remove As background from the chamber and the substrate was cooled to 505^oC under Sb flux in preparation for a 500-nm GaSb layer. Through careful control of the substrate temperature, III/V flux ratio and growth rate, an IMF array is formed at the GaAs/GaSb interface[?] that completely relaxes the lattice misfit strain in the GaSb. Next, the substrate was cooled to 440^oC for deposition of a 50-nm n-type Si-doped InAs backgate and a 8-nm AlSb charge blocking layer. A further 20 nm of GaSb was deposited at 505^oC before the substrate was cooled to 445^oC for deposition of a 12-nm $In_{0.8}Ga_{0.2}As$ channel layer. Finally, the substrate was cooled to 440^oC in preparation for deposition of the triple-barrier resonant tunnelling structure and floating gate, which consisted of; 1.8 nm AlSb, 3.0 nm InAs, 1.2 nm AlSb, 2.4 nm InAs, 1.8 nm AlSb and 10 nm InAs. High-resolution X-ray diffraction measurements were carried out on a Bruker D8 Discover system. The copper K-α X-ray beam was conditioned by a two-bounce Ge crystal and collimating optics. The diffracted signal was collected using an one-bounce Ge crystal and scintillation counter. Fitting of $\omega - 2\theta$ data was carried out using RADS Mercury software. To reduce the number of free parameters in the fitting model the InAs layer thicknesses were linked using a fitting parameter, a, such that $T_n^{InAs} = a \times T_{n,target}^{InAs}$. Where T_n^{InAs} are the individual InAs layer thicknesses calculated by the simulation and $T_{n,target}^{InAs}$ are the InAs layer thicknesses that were expected to have been deposited. A similar method was used for the AlSb layers using a fitting parameter, b, such that $T_n^{AlSb} = b \times T_{n,target}^{AlSb}$. It was also assumed that only the 50 nm InAs back gate and GaSb buffer layer contained any relaxation of the crystal lattice. The X-STM experiments have been performed in a commercial Scienta Omicron low-temperature STM (LT-STM) at liquid nitrogen temperature (LNT) and in a Scienta Omicron room-temperature STM. Both systems work at ultra high vacuum (UHV) with a pressure of 4-6 $\times 10^{-11}$ mbar. Rectangular shaped samples of $4\times8\ mm^2$ cut from the wafer were clamped in an upright position in a custom sample holder. The samples are loaded in the system and baked at at $(\sim 180^oC)$ to remove impurities form the surface. The samples are then cleaved and moved inside to the STM for the experiment. When the experiment is performed in the LT-STM, the sample is first cooled down at liquid nitrogen temperature and afterwards it is cleaved. In the LT-STM, the cleaved surface remains clean for a relatively extended amount of time (weeks) thanks to the low temperature and the UHV environment. Differently, in the RT system, despite the UHV, a new sample must be cleaved after two days due to the deposition of contaminants on the cleaved surface. The STM tips were prepared by electrochemical etching of polycrystalline tungsten wire in KOH 2 M. The tips are then loaded in the system, backed at $(\sim 230^oC)$ and sputtered with Ar to remove the W oxides that form on the

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surface.
The AFM experiment was performed at room temperature on a commercial Veeco Dimension III AFM, using a Pt coated Si cantilever with tetrahedral tip (OMCL-AC240TM-B2).
The X-STM and the AFM images were processed by Gwyddion. On the images an initial levelling of data by mean subtraction was applied. No further processing was necessary for the AFM images. A sharpening filter was applied on the STM images to better highlight the different feature presents, such as the stacking faults. No artifacts are added to the images through this processing method.

ACKNOWLEDGMENTS

This work was supported by European Union's Horizon 2020 research and innovation programme under the Marie Skłodowska-Curie grant agreement n 956548, project QUANTIMONY and the EPSRC Future Compound Semiconductor Manufacturing Hub grant EP/P006973/1.
The authors wish to acknowledge Michael Verhage and Niels de Vries for the AFM measurements and Raja Gajjela for the FE simulations.

AUTHOR DECLARATIONS

The authors have no conflicts to disclose.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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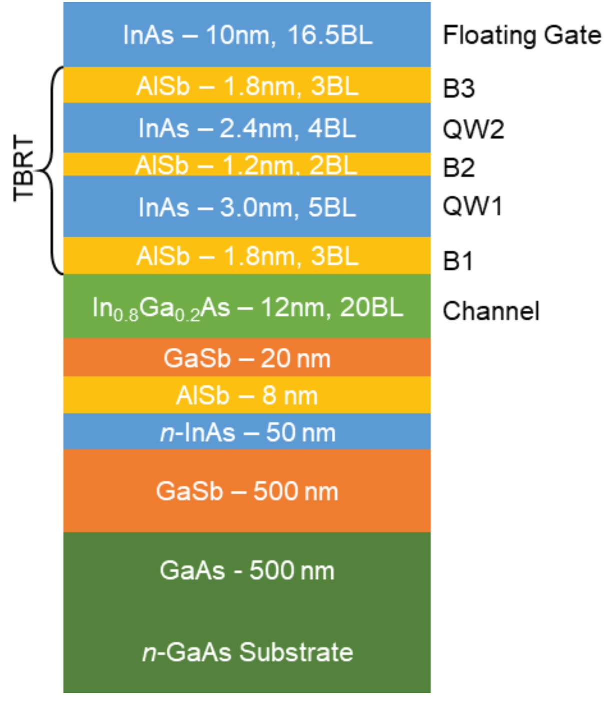

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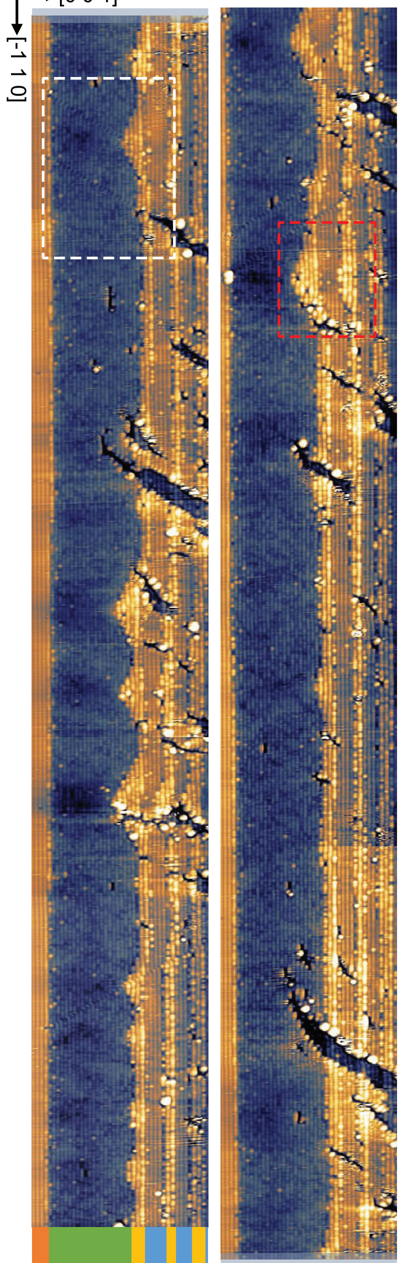

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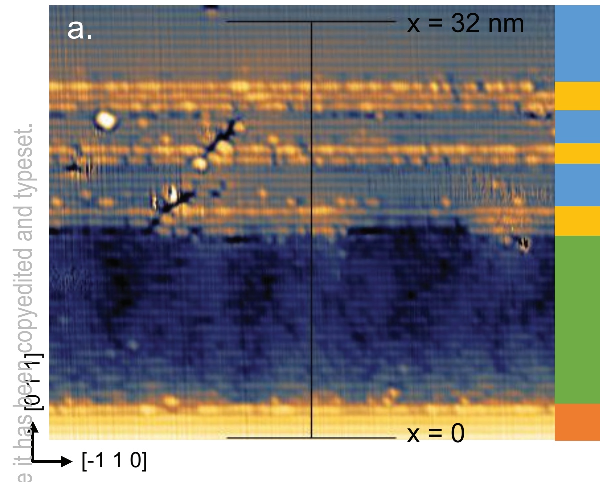

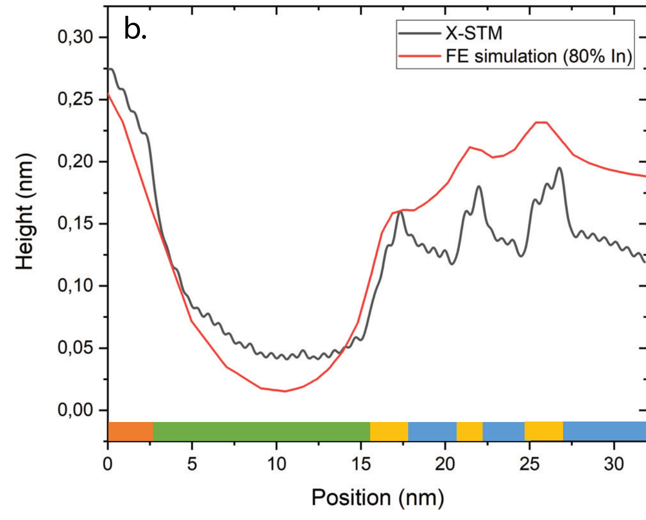

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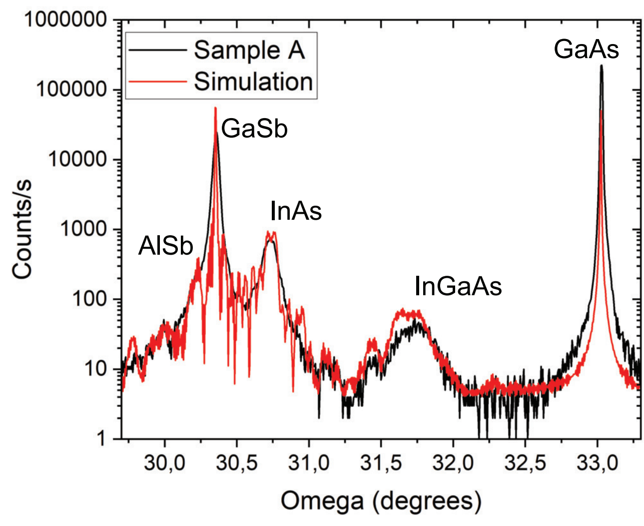

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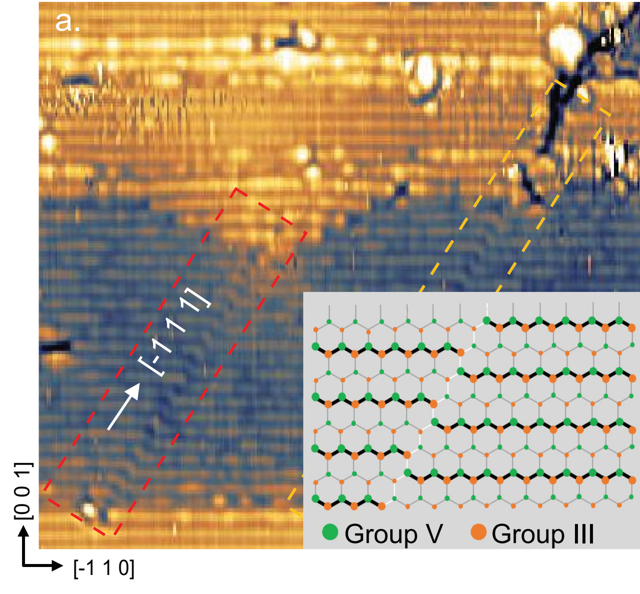

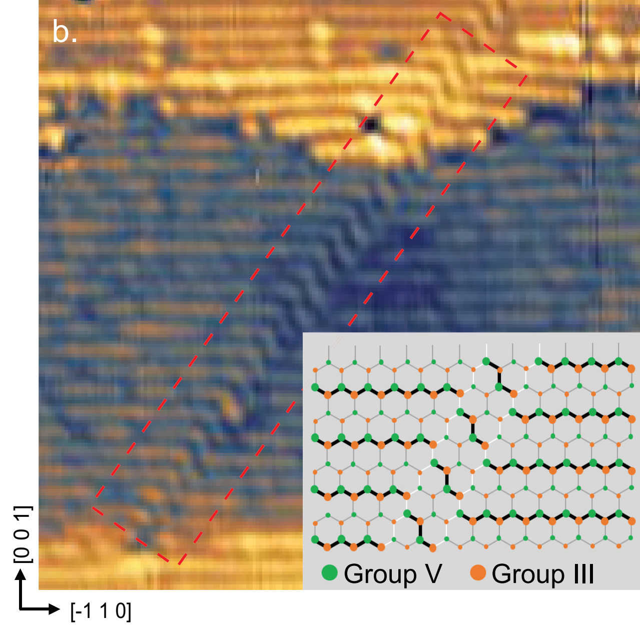

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