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Dual Isolated Multilevel Modular Inverter with Novel Switching and Voltage Stress Suppression

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Abstract: This paper presents an improved structure for the submodules (SMs) in the three-phase modular inverter (TPMI) based on a dual isolated SEPIC/CUK (DISC) converter for large-scale photovoltaic (LSPV) plants. The DISC SMs can offer several advantages, including increased efficiency, reduced passive elements, and galvanic isolation via compact-size high-frequency transformers. The SMs can also provide a wide range for the output voltage and draw continuous currents with low ripples from the input source. However, the high dv/dt value across the switches during hard switching can cause current oscillations and voltage spikes, which will impair the operation of complementary switches and affect the safety of the power devices. For this challenge, the DISC SM is improved by replacing the output switches with diodes and adding a bypassing switch. In comparison to the conventional DISC SM, the improved DISC SM reduces the switch's voltage spikes; hence, it can increase the overall efficiency. Thus, the DISC SM's will be able to suppress voltage spikes in the TPMI inverter and therefore the total reliability will be improved. The work will detail the analysis of the proposed system along with design guidelines. Additionally, the simulation and experimental results to validate the operation of proposed DISC SM are presented using MATLAB/SIMULINK as well as a scaled-down experimental prototype.

Keywords: photovoltaic systems; modular inverters; reduced number of switches; power electronic converters

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1. Introduction

A solid commitment of policymakers in different countries to repair the ongoing damage to our planet's ecosystem caused by fossil fuel consumption has increased the interest in the use of renewable energy sources (RESs) in both the energy and transportation sectors. Among the various RESs, photovoltaic (PV) systems became more promising due to their long-term viability in distributed generation systems, which can give humanity free available energy. In recent years, PV systems have progressively risen to the top of the RESs list for electricity generation [1]. By 2030, the capacity of new solar PV installations is expected to reach about 270 GW per year and will be increased to 372 GW by 2050. This progress is driven by the decrease in the cost of PV modules, which has paved the way for large-scale PV (LSPV) plants. In response to the recent rapid development of LSPV plants, several companies have started looking for a wide variety of PV inverter systems with various topologies and features [2].

Traditionally, LSPV power plants have been connected to the grid via conventional two-level inverters, filters, and low-frequency transformers (LFTs). This configuration adds to the size and the cost of the system dramatically and decreases the controllability and the reliability in case of partial failure [3]. Therefore, an inverter topology with a small footprint and better performance is necessary for handling the power and boosting the voltage of the PV modules to the medium-voltage (MV) level [4]. Modular multilevel inverters (MMIs) have become an essential power conversion unit in grid-integration applications [5].

They introduce several advantages, such as high-quality voltage generation, modularity, scalability, reduced switching power loss, lower dv/dt stress, and better total harmonics distortion (THD) [6]. MMIs are promising candidates for integrating PV systems into the MV grid since they can boost the low voltage of PV modules to the MV level and be compliant with grid regulations and codes [7]. Early multilevel converters relied on a single DC source and a single dc-link capacitor or series of capacitors. They used a high number of passive components to generate more voltage levels [8]. In this category, the neutral point clamped (NPC) and flying capacitor (FC) converters are the common topologies. Both topologies suffer from imbalance issues with the capacitors and hence they are unsuitable for the PV/MV applications [9].

MMI topologies with the cascaded H-bridge converter (CHB) have gained increased popularity in recent years due to numerous advantages, including the possibility to be supplied from different sources, scalability to increase the power level, and modularity [10]. Accordingly, CHB converters have distributed maximum power point tracking (MPPT) controllers, which will increase the total harvested power [11]. Due to their modular structure, they can generate large voltages, by increasing the number of modules, ranging from many hundreds of kV to the MV level if needed. They have a high fault tolerance and require low capacitances for balancing [12]. However, their main problem is the lack of galvanic isolation and the circulation of leakage currents which poses risks to the PV arrays and raises safety concerns [13].

In this context, the development of MMI topologies is necessary to ensure their compatibility for PV systems at the MV or HV levels. Research efforts have been conducted to explore modular topologies which can provide galvanic isolation and improve the performance of LSPV systems when connected to the MV grid [14,15]. These topologies employ internal high-frequency transformers (HFTs) into their submodules (SMs) to increasing the reliability and security of the PV system [16]. These topologies aim for achieving a full MPPT control, ensuring galvanic isolation, generating low THD, and reducing the total size and weight [17]. Several three-phase modular inverters (TPMIs) have been proposed in the literature as candidates for LSPV systems [18]. These TPMIs employ several SMs in series/parallel combination to boost the voltage from the PV modules level to the MV grids, control the power flow and harvest the maximum energy from the PV modules [19].

The fly-back converter is a well-known topology due to its simplicity and low cost as well as its ability to connect with a PV-tied grid to offer both isolation and unidirectional power flow [20]. In [21], a three-phase modular fly-back topology inverter is presented. The proposed inverter structure is comprised of parallel SMs based on isolated fly back converters with a suitable power level. These SMs are connected in parallel on the DC input side and differentially on the grid side. The performance of fly back with MMIs benefits from the HFTs to provide voltage-boosting and galvanic isolation. Multiple fly-back SMs are connected in parallel to allow the current distribution of them, hence enabling an increase in the apparent switching frequency and a corresponding reduction in the HFTs. Although the proposed structure is modular, the power capability does not rise proportionally with the number of SMs. To add more power to this structure, more SMs and PV modules must be connected in parallel with the ones that are already there. Thus, it can be suited for low-power applications, as shown in the results. Moreover, fly back suffers from high leakage inductance and discontinuous current nature at the input and output sides, which will limit the conversion efficiency [22].

Four possible SM topologies for C5 (Cuk), F5, G5 (SEPIC), and P5 converters are investigated in [23]. These SM converters are employed in MMI structure that offers galvanic isolation with the use of HFTs and can operate at a high switching frequency; hence, the footprint of the system can be considerably decreased [24]. Moreover, HFTs are proposed to provide the necessary level of safety and eliminate leakage currents. With their modularity aspect, more SMs and new PV modules can easily be added to increase power capability. Even in partial shade, MPPT operation will be improved because of the low

number of PV modules connected to each SM [25]. However, the unbalanced currents in the output sides make the associated control technique more complicated.

Among several converter topologies, a new SM based on a dual isolated SEPIC/Cuk (DISC) converter is introduced for MMIs, see Figure 1 [26]. The proposed SM inverter delivers balanced dual output voltages without additional voltage balance regulation. As the DISC SM has inductors on both the input and output sides, the ripple current will be reduced significantly, which is well suited for MPPT operation [27]. Furthermore, each side of the HFT has one capacitor connected in series with it to cancel the dc component of the transformer magnetising current, which in turn will reduce the size of the HFT [28]. DISC SM makes use of fewer passive components and power switches, performing single-stage DC–AC conversion, voltage boosting, compact size, and galvanic isolation.

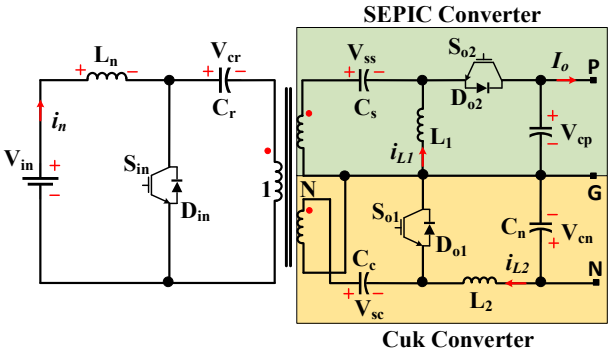

Figure 1. Classic DISC-SM of the TPMI inverter.

Despite the several benefits of DISC submodules in the literature, the high inrush current generated by the hard switching instants and the physical design of circuit at turned off moment results in significant current spikes through the switches, which can degrade the overall efficiency of the TPMI grid-connected inverter. To cope with an inrush current of the conventional DISC SM, this paper proposes a modified structure for the DISC in order to alleviate the current spikes without compromising the DISC SM benefits. By adding an active switch and diode to the output side of DISC-SMs and replacing other two active switches with passive diodes, the modified SM eliminates the problem completely. Replacing the two active switches with diodes will reduce the complexity of the operation as well as the switching losses. The additional output switch is operating at the grid 50/60 Hz frequency and therefore the switch losses will be reduced.

This paper presents the mathematical analyses and the steady-state space model of the modified eighth-order converter proposed DISC, which permits the design of robust controllers. The issue of the current spikes is discussed and solved. Then, the paper explains the operation of the proposed TPMI using the modified SM in the context of LSPV systems and provide the guide to select the parameters. A simple controller is used to show the performance of the final TPMI with MATLAB/SIMULINK computer simulations when powered from 500 W PV modules. The operation of the system is tested using a scaled-down experimental prototype when controlled with a TMS320F28335 DSP. The rest of the paper is organised into the following sections: Section 2 presents the proposed TPMI system. The inverter's modulation technique is explained in Section 3. The generic operation of the inverter and the circuit diagrams are shown in Section 4. The details of steady-state analysis and the inverter's dynamic average model are described in Section 5. In Section 6, the parameter selection design is discussed. Both simulations and experiments are presented to validate the inverter's performance in Section 7.

2. General TPMI Description

The TPMI shown in Figure 2 can harvest the energy from the PV modules and transfer this energy to the MV grid. The converter SMs are arranged in series/parallel combination to make it possible for a grid-tied PV system without the need for a step-up transformer.

The SMs in this work consist of a combined SEPIC/Cuk (DISC) converter with dual-winding isolation.

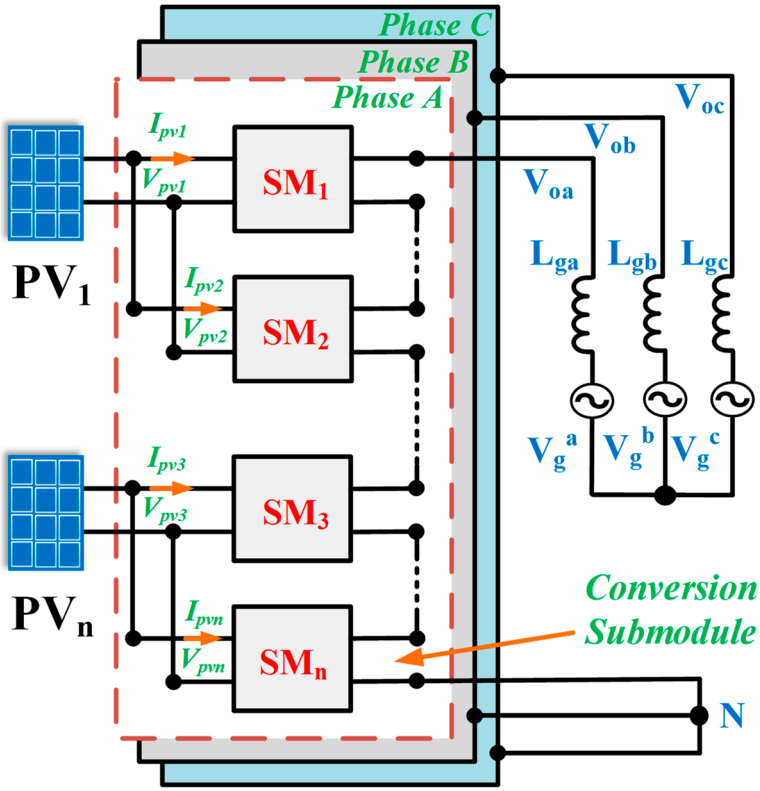

Figure 2. Proposed TPMI PV conversion system.

As long as the SEPIC and Cuk converters have the same instantaneous duty cycle, they can share a common front end and two output ends, which allows for dual output voltage generation. In the steady state, the SM's gain voltage is equal to the sum of the output voltages of the Cuk and SEPIC converters. Therefore, the DISC SM has the following voltage gain ratio due to both of these converters being buck-boost converters:

$$\frac{V_O}{V_{in}} = \frac{2\,N\,D}{1-D} \tag{1}$$

where D represents the duty-cycle ratio in steady state and N denotes the turn's ratio of the HTF. The SM's output voltage is twice that of conventional buck-boost converters. Additionally, the HFT can contribute to the voltage gain increase by adjusting N as appropriate.

2.1. Current Spikes Limitation

Figure 1 shows the classic SM of dual isolated DISC converter for the proposed TPMI inverter. As a disadvantage, current spikes over switches occur because both outputs switch S_{o1} and S_{o2} began conducting simultaneously with the input switch S_{in} being turned off, see Figure 3. In this case, the input current is distributed across the two output switches according to the SEPIC (C_S), Cuk (C_C), and positive output (C_p) capacitor impedances, as well as their connection and polarity. The SEPIC capacitor and the positive output have the same polarity, which is the opposite to the Cuk capacitor. They can be expressed as:

$$V_{sum} = V_{SS} + V_{Cp} - V_{SC} \tag{2}$$

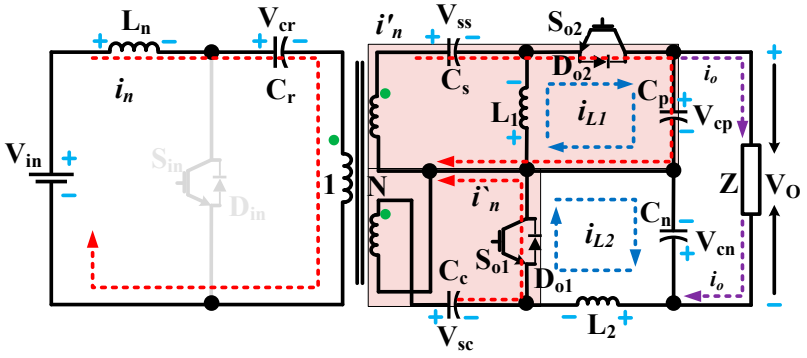

Figure 3. Output switches turned ON.

While both output switches are in the ON state, the sum voltages are abruptly reduced to zero, resulting in a short circuit and a huge current spike through the output switches. The rapid rate of current variations through the capacitors during the off state causes a current spike which may damage any semiconductor in its path. Practically, the current spike may be reduced by the loop's parasitic resistance, which includes the on-resistance of switches R_{sw} and equivalent series resistance (ESR) of capacitors.

2.2. Proposed DISC SM

The DISC SM converter is modified to fix the problem explained in the previous subsection. In the modified DISC SM topology, the output switches of the converters are replaced by diodes while an active switch and diode are introduced to the AC output side to alleviate the TPMI inverter's current spike issue, see Figure 4.

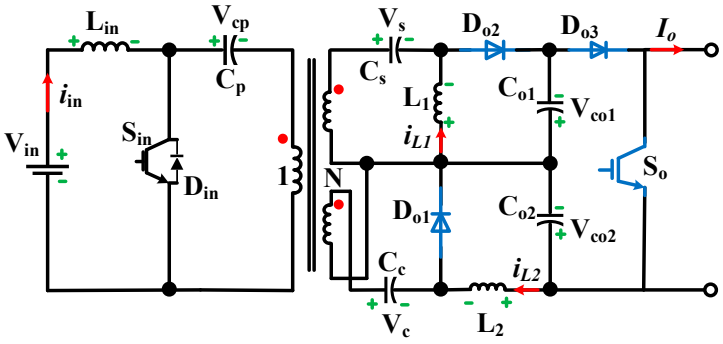

Figure 4. Proposed DISC SM OF TPMI inverter.

The modified structure of the DISC SM uses diodes D_{o1} and D_{o2} to minimise the number of switches and to provide a proper path for the interrupted current. In this case, the inductors size can be selected large enough to provide a smoother current at the output side. Moreover, the freewheeling diodes can also participate to protect the capacitors from overcharging. An external diode is attached to the output terminal of DISC to prevent short-circuiting. The outer switch S_o is responsible for bypassing the load's reverse current. The proposed DISC SM will remove the current spikes problem without the need for any advanced control on the output side, and therefore it provides lower switching and conduction losses, increased efficiency, and improved system reliability.

3. Modulation Scheme

The modulation principle is based on comparing a carrier signal to a reference signal in order to generate switching pulses. To explain this principle, two successive SMs have been chosen. Both SMs are supplied from the same PV array but each SM only operates for half a cycle without adding the DC offset component to the output voltage terminal. Figure 5 illustrates the SMs' AC voltage components appearing at the grid terminal. The following equations describe the output voltage for each SM.

$$V_{Jn-1} = \begin{cases} V_{n-1}\sin\omega t & 0 \geq \omega t \geq \pi \\ 0 & \pi > \omega t \geq 2\pi \end{cases} \quad (3)$$

$$V_{Jn} = \begin{cases} 0 & 0 \geq \omega t \geq \pi \\ V_n \sin(\omega t + \pi) & \pi > \omega t \geq 2\pi \end{cases} \quad (4)$$

where J indicates the phase (a, b, or c) and n the number of PV SMs. As both V_{n-1} and V_n are equal, the output voltage that emerges from both SMs is:

$$V_{JnO} = V_n \sin\omega t \quad (5)$$

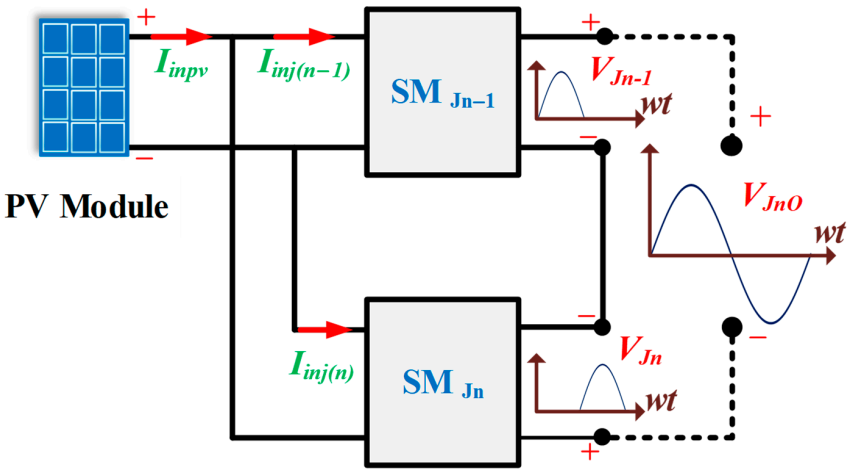

Figure 5. Modulation principle.

It is possible to determine the D of the SM number 'n' in phase 'J' by using the following formula:

$$\frac{V_{JnO}}{NV_{in}} = \frac{2D}{(1-D)} \quad D = \frac{V_{JnO}}{2N(V_{in} + V_{JnO})} \quad (6)$$

4. SM Operation

The SM operates in the continuous conduction mode (CCM). Three different operational states are possible in the SM topology within a single switching cycle t_s as follows:

- State 1 (ON cycle)

In this mode, S_{in} is turned ON while the output switch S_o is OFF, causing the input current i_{in} to increase, which discharges the primary capacitors C_p as seen in Figure 6. At the same time, the energy stored in C_s and C_c is released into the inductors L_1 and L_2. In this mode, diodes D_{o1} and D_{o2} do not conduct; the output capacitors C_{po} and C_{no} provide the necessary load current through D_{o3} to keep everything running smoothly.

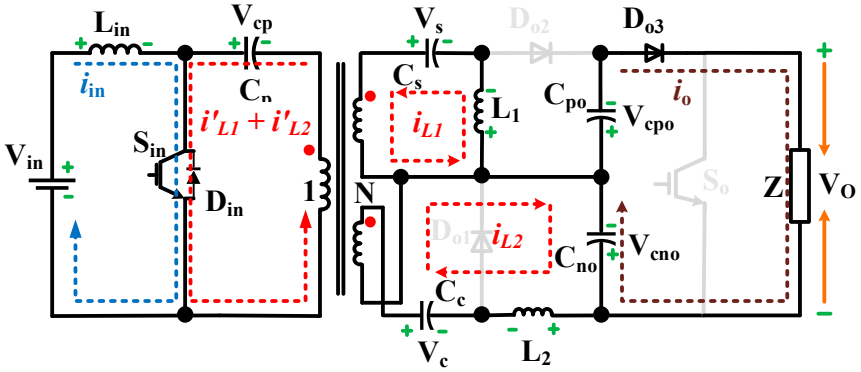

Figure 6. SM in state 1.

- State 2 (OFF cycle)

Switches S_{in} and S_O are turned OFF as seen in Figure 7. In this case, i_n flows through the primary capacitor C_p, the C_S, and the C_C capacitors. Consequently, these capacitors charge, and their voltages immediately increase. The diodes D_{o1} and D_{o2} are forward biased and hence the upper output inductor L_1 releases energy to charge C_{po} and drive it to the load in its path through output diode D_{o3}, while the lower output inductor L_2 discharges and transfers energy to C_{no} and the output load.

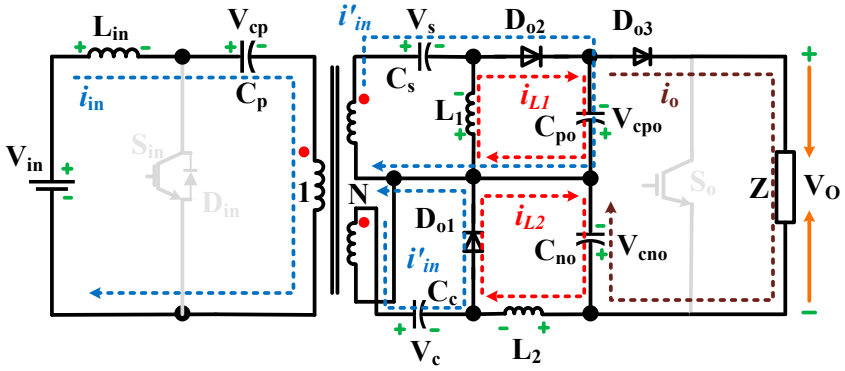

Figure 7. SM in State 2.

- State 3 (Shutdown)

As illustrated in Figure 8, only S_o is turned ON while input switch S_{in} and all diodes are off. Therefore, the switch S_o provides the path for constant current of output current i_o. This mode of operation remains until the next switching period begins.

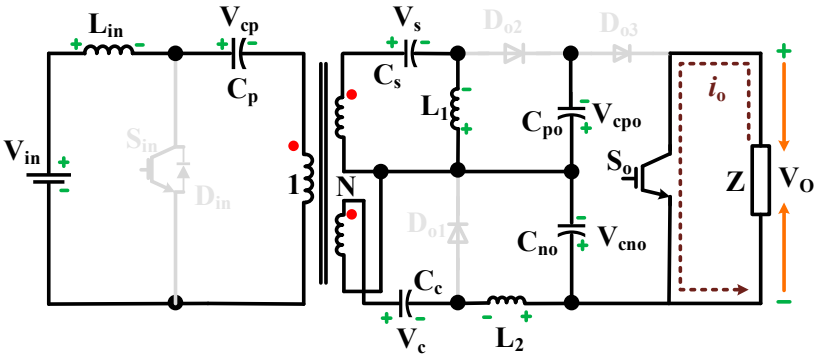

Figure 8. SM in State 3.

5. System's SM Average Model

5.1. Analysis of SM Steady States

It is challenging to present a state-space average model for the DISC because it is an 8th order converter and hence has not yet been published in the literature. The state-space model is important to understand the SM's behaviour, generate the transfer function for control design, and use it in the selection of parameters. Using the following equations, the state-space model can be described:

$$\dot{x} = Ax + Bu \tag{7}$$

$$y = Cx + Bu \tag{8}$$

where x is a vector representing the state variables, and u and y are the input and output vectors, respectively. The state vector can be defined as follows: $x(t) = [i_n(t)\ v_{cp}(t)\ v_s(t)\ v_c(t)\ i_{L1}(t)\ i_{L2}(t)\ v_{cpo}(t)\ v_{cno}(t)]$. Figure 9 shows theoretical waveforms for the proposed

DISC SM. Thus, the state-space model can be averaged over the ON and OFF states in the following way:

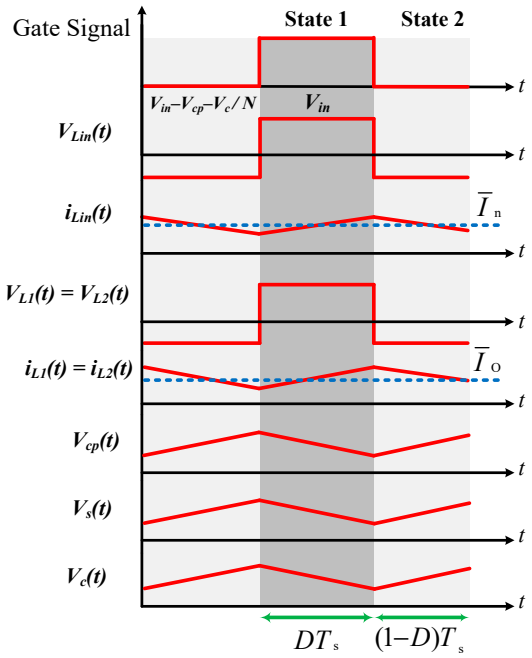

Figure 9. Theoretical waveforms of SM.

I. Mode-1.

The equivalent circuit of DISC SM during state 1 is shown in Figure 6. Consequently, the differential equations for the state variables of the SM can be derived as follows:

$$\frac{di_{in}}{dt} = \frac{1}{L_{in}} V_{in} \tag{9}$$

$$\frac{dv_{cp}}{dt} = -\frac{N}{C_p} (i_{L1} + i_{L2}) \tag{10}$$

$$\frac{dv_s}{dt} = -\frac{1}{C_s} i_{L1} \tag{11}$$

$$\frac{dv_c}{dt} = -\frac{1}{C_c} i_{L2} \tag{12}$$

$$\frac{di_{L1}}{dt} = \frac{N}{L_1} V_{cp} + \frac{1}{L_1} V_s \tag{13}$$

$$\frac{di_{L2}}{dt} = \frac{N}{L_2} V_{cp} + \frac{1}{L_2} V_c - \frac{1}{L_2} V_{cno} \tag{14}$$

$$\frac{dv_{cpo}}{dt} = -\frac{1}{C_{po}Z} V_{cpo} - \frac{1}{C_{po}Z} V_{cno} \tag{15}$$

$$\frac{dv_{cno}}{dt} = \frac{1}{C_{no}} i_{L2} - \frac{1}{C_{no}Z} V_{cpo} - \frac{1}{C_{no}Z} V_{cno} \tag{16}$$

II. Mode-2.

It is not possible to solve the differential equations directly without making certain estimations due to the complexity of the SM combination of the Cuk and SEPIC out-put sides. These estimations were based on the following observations.

A. The average currents of the capacitors are zero in the sub-circuit depicted in Figure 10a, which results in the average values of L_1 and L_2 being almost equal to the average load current i_o.

B. Since the inductors' currents are equal, the currents going into C_s and C_{po} in a separate loop are equal, see Figure 10b. Hence, the total series capacitance of C_s and C_{po} can be determined as follows:

$$C_T = \frac{C_s * C_{po}}{C_s + C_{po}} \tag{17}$$

C. Figure 10c shows that the input current is divided by the impedance values of the capacitors on the converter's output sides in accordance with the ratio ($\mathcal{R}$).

$$\mathcal{R} = \frac{C_c}{C_T} \tag{18}$$

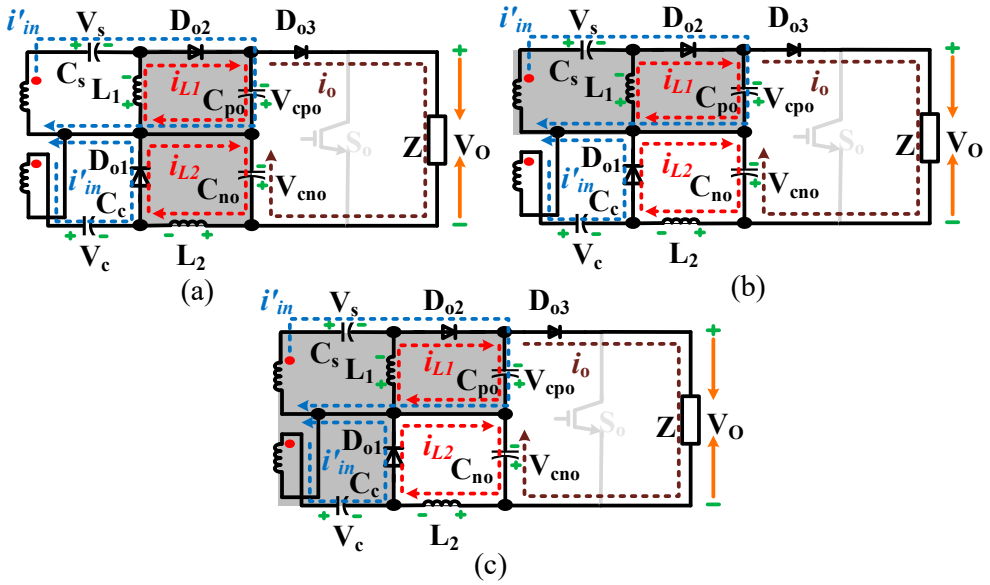

Figure 10. Observation in state 2: (**a**) sub-circuit current flow, (**b**) series capacitors loop, and (**c**) input current splitting.

During state 2, these observations and assumptions are important in order to simplify the differential equations. Thus, the following differential equations can then be deduced:

$$\frac{di_{in}}{dt} = \frac{1}{L_{in}} V_{in} - \frac{1}{L_{in}} V_{cp} - \frac{1}{NL_{in}} V_c \tag{19}$$

$$\frac{dv_p}{dt} = \frac{1}{C_p} i_{in} \tag{20}$$

$$\frac{dv_s}{dt} = \frac{1}{C_s} * \frac{1}{N(1+\mathcal{R})} i_{in} \tag{21}$$

$$\frac{dv_c}{dt} = \frac{1}{C_c} * \frac{\mathcal{R}}{N(1+\mathcal{R})} i_{in} \tag{22}$$

$$\frac{di_{L1}}{dt} = -\frac{1}{L_1} V_{cpo} \tag{23}$$

$$\frac{di_{L2}}{dt} = -\frac{1}{L_2} V_{cno} \tag{24}$$

$$\frac{dv_{cpo}}{dt} = \frac{1}{C_{po}} * \frac{1}{N(1+\mathcal{R})}\, i_{in} \tag{25}$$

$$\frac{dv_{cno}}{dt} = \frac{1}{C_{no}}\, i_{L2} - \frac{1}{C_{no}Z}\, V_{cpo} - \frac{1}{C_{no}Z}\, V_{cno} \tag{26}$$

5.2. Modelling of DISC SM

The following matrices are associated with the state-space model of DISC topology:

$$[A_{on}] = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{-N}{C_p} & \frac{-N}{C_p} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{-1}{C_S} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{C_C} & 0 & 0 \\ 0 & \frac{N}{L_1} & \frac{1}{L_1} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{N}{L_2} & 0 & \frac{1}{L_2} & 0 & 0 & 0 & \frac{-1}{L_2} \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{-1}{ZC_{po}} & \frac{-1}{ZC_{po}} \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{C_{no}} & \frac{-1}{ZC_{no}} & \frac{-1}{ZC_{no}} \end{bmatrix} \tag{27}$$

$$B_{on} = \begin{bmatrix} \frac{1}{L_{in}} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}^T \tag{28}$$

$$C_{on} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & -1 & 1 \end{bmatrix}^T \tag{29}$$

$$\begin{bmatrix} A_{off} \end{bmatrix} = \begin{bmatrix} 0 & \frac{-1}{L_{in}} & 0 & \frac{-1}{NL_{in}} & 0 & 0 & 0 & 0 \\ \frac{1}{C_p} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \frac{C_{po}}{K} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \frac{C_{po}+C_S}{K} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_1} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_2} \\ \frac{C_s}{K} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{C_{no}} & \frac{-1}{ZC_{no}} & \frac{-1}{ZC_{no}} \end{bmatrix} \tag{30}$$

where K denotes the variables in the aforementioned state-space matrices, and the following is the corresponding expression:

$$K = N * \left(C_c C_{po} + C_c C_S + C_S C_{po}\right) \tag{31}$$

$$B_{off} = \begin{bmatrix} \frac{1}{L_{in}} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}^T \tag{32}$$

$$C_{off} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & -1 & 1 \end{bmatrix}^T \tag{33}$$

The following averaged state-space matrices are obtained by averaging the two state-space representations over the ON cycle modes.

$$\begin{bmatrix} A_{Avg} \end{bmatrix} = \begin{bmatrix} 0 & \frac{D-1}{L_{in}} & 0 & \frac{D-1}{NL_{in}} & 0 & 0 & 0 & 0 \\ \frac{-(D-1)}{C_p} & 0 & 0 & 0 & \frac{-DN}{C_p} & \frac{-DN}{C_p} & 0 & 0 \\ \frac{-C_{po}(D-1)}{K} & 0 & 0 & 0 & \frac{-D}{C_S} & 0 & 0 & 0 \\ \frac{-(D-1)C_{po}+C_S}{K} & 0 & 0 & 0 & 0 & \frac{-D}{C_C} & 0 & 0 \\ 0 & \frac{DN}{L_1} & \frac{D}{L_1} & 0 & 0 & 0 & \frac{D-1}{L_1} & 0 \\ 0 & \frac{DN}{L_2} & 0 & \frac{D}{L_2} & 0 & 0 & 0 & \frac{-1}{L_2} \\ \frac{-C_s(D-1)}{K} & 0 & 0 & 0 & 0 & 0 & \frac{-D}{ZC_{po}} & \frac{-D}{ZC_{po}} \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{C_{no}} & \frac{-1}{ZC_{no}} & \frac{-1}{ZC_{no}} \end{bmatrix} \tag{34}$$

$$B_{Avg} = \begin{bmatrix} \frac{1}{L_{in}} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}^T \quad (35)$$

$$C_{off} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & -1 & 1 \end{bmatrix}^T \quad (36)$$

The DISC SM has the following s-domain transfer function:

$$G(s) = C_{avg}(sI - A_{avg})^{-1} B_{avg} \quad (37)$$

$$G(s) = \frac{a_5 s^5 + a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0}{b_7 s^7 + b_6 s^6 + b_5 s^5 + b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b} \quad (38)$$

where $a_5, \ldots a_0$ and $b_7, \ldots b_0$ are the coefficients of the numerator and denominator whose values depend on the DISC SM parameters. As expected, the steady-state voltage gain ratio of the SM is given by:

$$\lim_{s \to 0} G(s) = \frac{V_O}{V_{in}} = \frac{2DN}{1 - D} \quad (39)$$

6. Passive Components Design

The design procedure entailed averaging the DISC SM in state 1 or state 2 to derive equations describing the voltages across and currents through the individual passive components. Therefore, it is possible to derive inductance and capacitance formulas that are dependent on other known parameters by combining equations from any of these modes with the inductor and capacitor equations. These equations can be of extremely high order (up to eight) due to there being eight passive components and hence the derivations are simplified using small ripple approximations. The following equations are formed because of this approach:

$$L_{in} = \frac{V_O \, {V_{in}}^2 \, t_s}{2N(V_{in} + V_O) P_{out} \, \Delta I_{in}\%} \quad (40)$$

$$L_1 = L_2 = \frac{V_{in} \, {V_o}^2 \, t_s}{2(V_{in} + V_O) P_{out} \, \Delta I_{L_{1,2}}\%} \quad (41)$$

$$C_p = \frac{V_O \, P_{out} \, t_s}{2(V_{in} + V_O) V_{in} \Delta V_{cr}\%} \quad (42)$$

$$C_s = C_c = \frac{P_{out} \, t_s}{2N(V_{in} + V_O) \Delta V_{s,c}\%} \quad (43)$$

$$C_{po} = \frac{P_{out} \, t_s}{2N(V_{in} + V_O) \Delta V_{cpo}\%} \quad (44)$$

$$C_{no} = \frac{V_o \, t_s}{2N(V_{in} + V_O) \Delta V_{con}\%} \quad (45)$$

These factors $\Delta I\%$ *and* $\Delta V\%$ are the maximum allowable current and voltages ripples (represented as a proportion of their average values), where t_s refers to the switching time.

7. System's Validation

To show the operation of the TPMI with the modified SM, SIMULINK/MATLAB models have been built and controlled using the parameters shown in Table 1 and will be explained in this section. Moreover, the experimental results conducted to test the performance of the TPMI will be shown and discussed.

7.1. Simulation Results

This section presents the MATLAB/Simulink simulation results for the proposed topology when used in a large-scale PV plant generating 1 MW and connected to the MVAC grid. The system's parameters used in this case study are listed in Table 1.

Table 1. Parameters of the SIMULINK/MATLAB model.

Parameters	Value
Number of modules	n = 80
SM rated power	P_{SM} = 4.2 kW
SM inductors	L_{in} = 1.5 mH and $L_1 = L_2$ = 1 mH
SM capacitors	$C_p = C_s = C_c$ = 10 µF C_{no} = 10 µF and C_{po} = 50 µF
SM Switching frequency	f_s = 50 kHz
Transformer turns' ratio	N = 1
PV module	Grape Solar GS-S-420-KR3 (P_m = 420 W, V_{mp} = 48.73 V, I_{mp} = 8.62)
PV array	10 parallel × 3 series
Grid voltage	13.47 kV
Grid impedance	L_g = 1 mH, r_g = 0.5Ω
Grid frequency	f = 50 Hz

Figure 11 shows a simple control system to operate the TPMI power flows from the PV arrays to the MV grid. The output current is controlled by a proportional-resonant (PR) controller tuned at the grid frequency $\omega_o = 2\pi f$. It should be noted that this control system assumes that all the PV modules operate at the same irradiance and other weather conditions. However, another system-level control will be necessary in case of partial shading to distribute the power on the SMs according to their different maximum power points. The partial shading cases are not covered in this paper and may be considered in future publications.

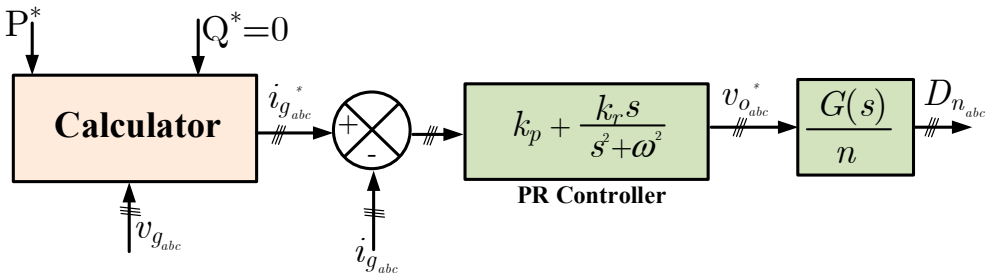

Figure 11. Control system during DC/AC inversion.

Figure 12 shows the simulation results for the proposed system using MATLAB/SIMULINK software. The power is increasing from zero to the maximum of around 1 MW in 100 ms. To simulate the dynamic response, the irradiance, and hence the power, falls to 60% of the maximum for all PV modules simultaneously at t = 300 ms. Figure 12a shows the total power transferred from the PV modules and injected into the MV grid when it increases from zero to the maximum after 100 ms and then drops to 60% at 300 ms. Figure 12b shows the total output three-phase voltage and grid current. As the output voltage is constant in this case, the output current has dropped to 60% of its rated value. Figure 12c shows the output voltage of the top two SMs in phase a, where each SM is operating for one half-cycle. The magnitude of this voltage has not been changed but the phase angle has been changed slightly to cater for the change in the power. The top graph of Figure 12d shows the input currents for the 1st two SMs in phase a while the bottom graph shows the total input current from the PV array. Although the individual currents of the SMs in the phases are pulsating at 100 Hz, the total current drawn from the PV modules is constant and so the PV modules can operate at the maximum possible power point.

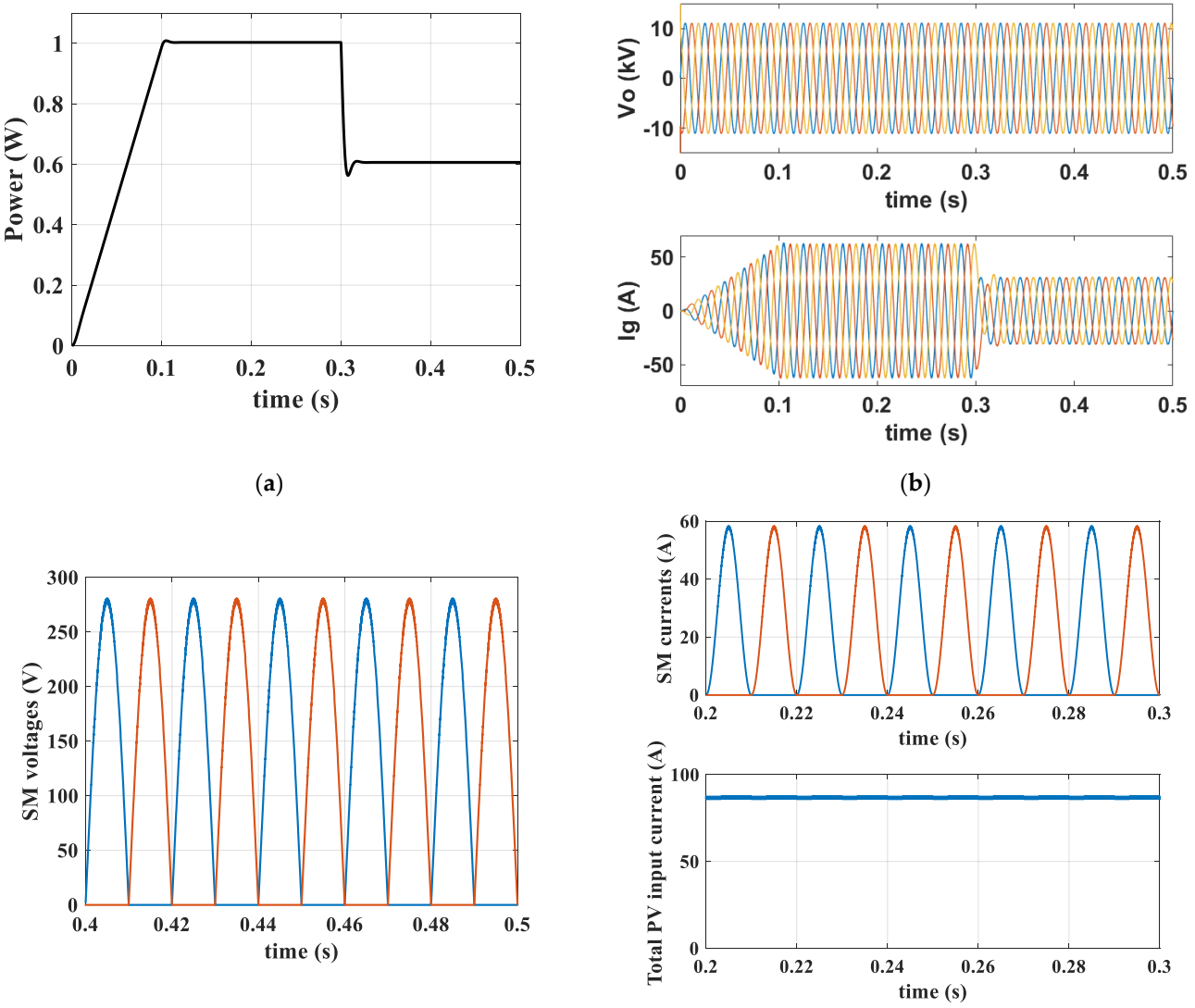

Figure 12. SIMULINK/MATLAB simulations of the MCI during DC/AC inversion from PV modules to grid. (**a**) Total ouput power; (**b**) Three-phase voltage and current; (**c**) Output voltage of the first two SMs in phase *a*; (**d**) Input currents: (**top**) the input currents to the first two SMs in phase *a*, and (**bottom**) the total PV module current for the first SMs in phases *a*, *b*, and *c*.

7.2. Experimental Results

Figure 13 shows the experimental setup for the three-phase TPMI with 12 SMs (4 SMs per phase) each rated at 250 W and hence the full system is rated at 3 kW. The inverter is controlled by a TMS32028335 DSP with the same passive element mentioned parameters used in the computer simulation.

The DC voltage sources at 48 V have been used to mimic the PV modules in the associated modes of operation. To test the operation of the inverter, the system is connected to the local grid and the rated power of 3 kW is converted from the power supplies to the LV AC load. Figure 14a shows the measured total power of the inverter when it is set to 3 kW. Figure 14b shows the total output voltage and the current of phase *a*. Figure 14c shows the output voltages of the first two SMs in phase a where the output switches S_o are controlled to operate each SM in a complete half-cycle. The bottom two SMs are not shown in the Figure because they are identical in this case. The voltage at the point of common coupling (PCC) is shared by the four SMs in each phase. Finally, Figure 14d shows

the input current of these first SMs in phase *a* with the total input (PV) current supplied to the three-phase SMs. This current is absorbed from the first DC supply. Although the individual currents of the SMs in the phases are pulsating at 100 Hz, the total current drawn from the PV modules are constant so the PV modules can operate at the maximum possible power point.

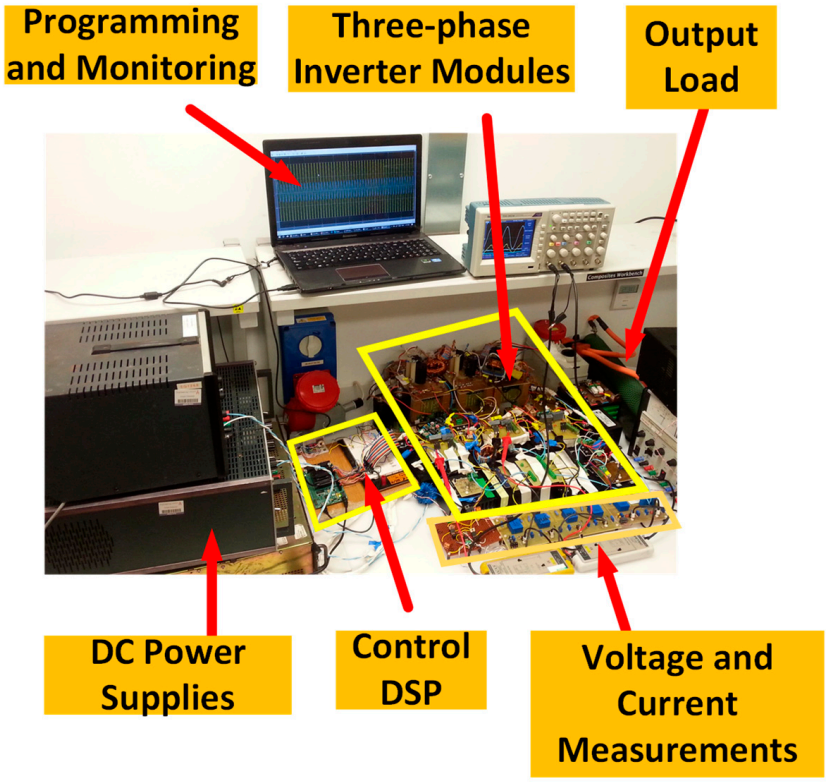

Figure 13. Experimental prototype.

Figure 15 shows the electrical connection of the SMs to the two power supplies. To show the operation of the proposed system during the partial shading of some PV modules, it will be assumed in the following experiment that the bottom source is shaded by generating 50% of its rated power while the top supply will keep generating 100% of its rated power. Thus, the total maximum available power of the system is 75% of the normal condition's value while this is controlled by setting the reference value of the output grid current to 75% of the rated value. It is assumed that the MPPT controller will be able to perform this action, which is not in the scope of this paper.

At t = 100 ms, the power will drop to 75% of the normal condition's value as shown in Figure 16a due to the shading of the lower supply. Figure 16b shows phase *a* grid voltage with the current when it drops to 75% at the moment of partial shading. Figure 16c shows the output voltages of the SMs in phase *a*. Before the partial shading moment, the output voltages of the SMs were equal. Then, the unshaded SMs' voltages have been increased to compensate for the drop in the current while the shaded SMs' voltages have been decreased by the same ratio. Figure 16d shows the supply voltages for the unshaded (Vpv1) and shaded (Vpv2) modules with their currents.

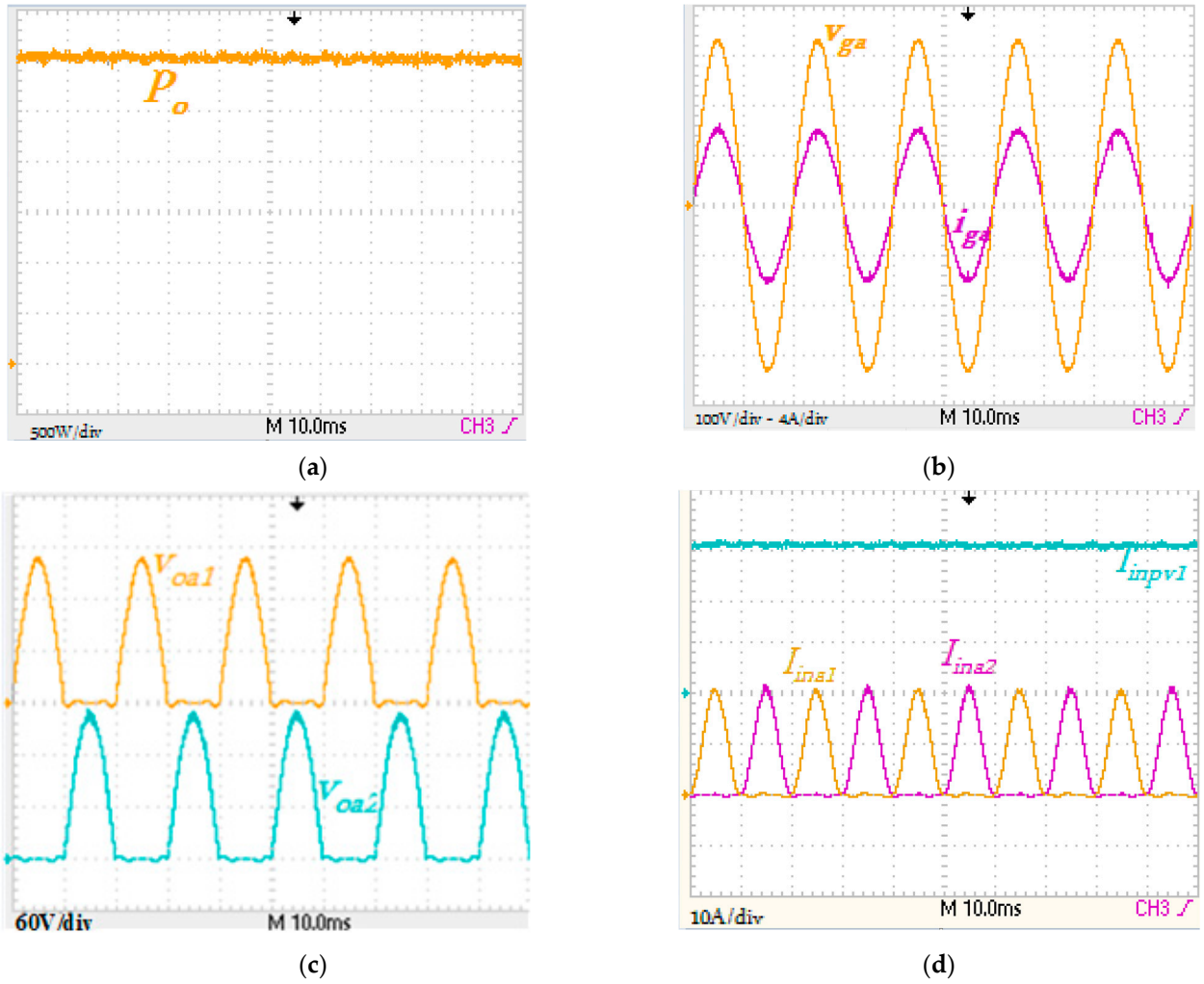

Figure 14. Experimental results during DC/AC inversion from DC sources to grid. (**a**) Total output power; (**b**) Phase *a* output voltage and current; (**c**) Output voltage of the first SMs in phases *a* (60 V/div); (**d**) PV modules currents of the first SMs in phases *a*, *b*, and *c*.

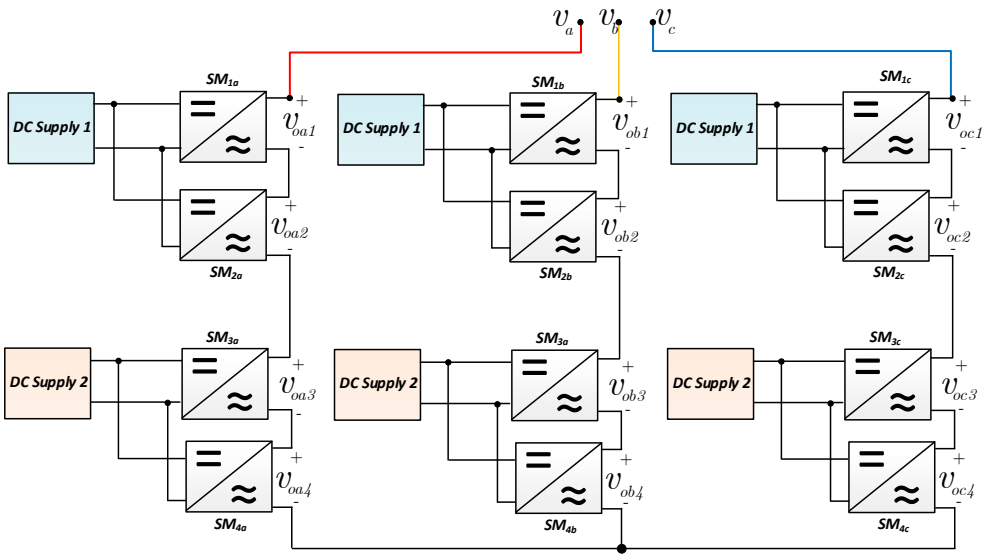

Figure 15. Experimental results during DC/AC inversion from DC sources to grid.

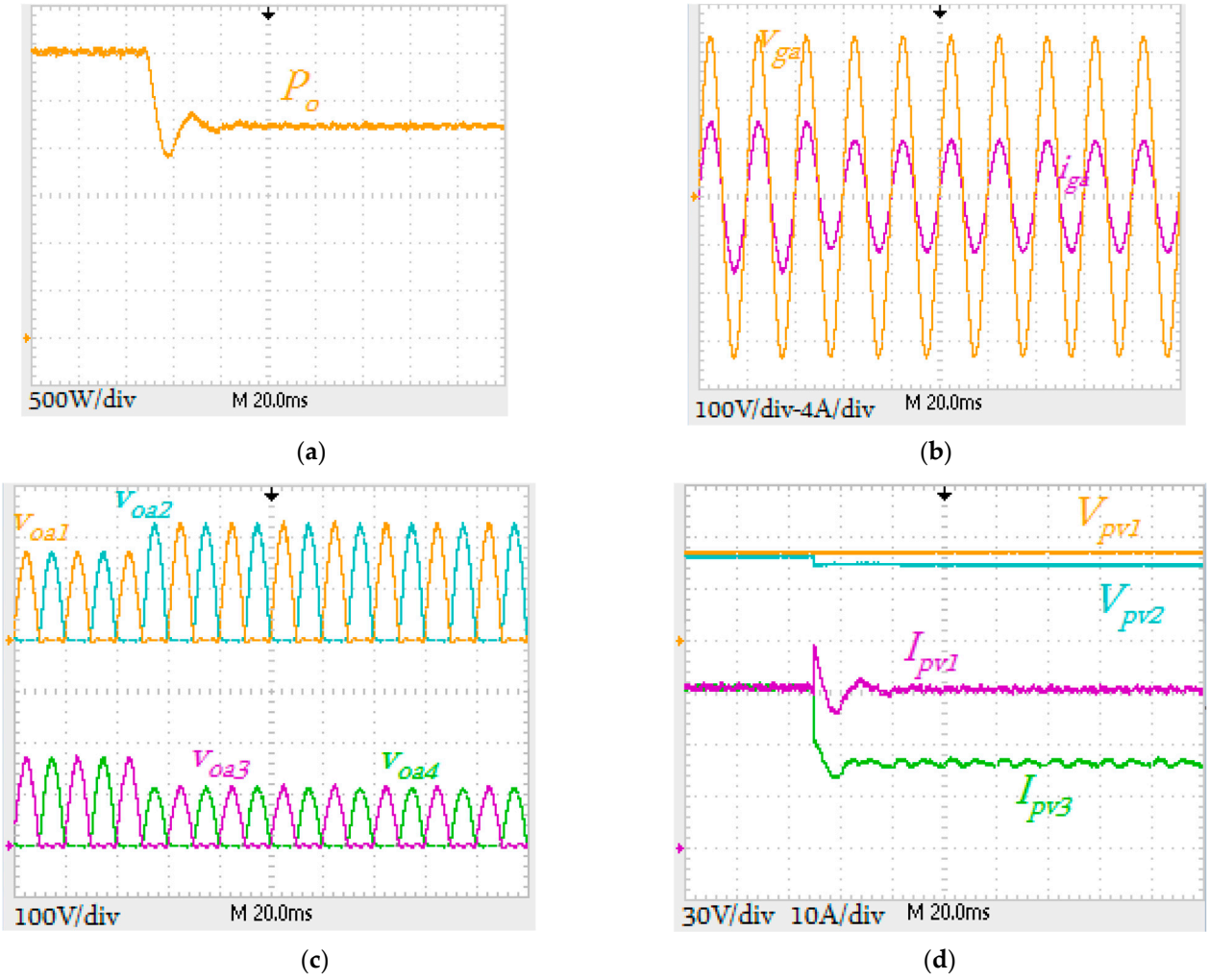

Figure 16. Experimental results during partial shading. (**a**) Total ouput power; (**b**) Phase *a* output voltage and current; (**c**) Output voltage of the first SMs in phases *a*; (**d**) PV modules voltage and currents.

8. Conclusions

In this paper, an improved MMI structure is introduced to reduce the switch count, control complexity, and eliminate the current spike. The TPMI inverter for LSPV systems is composed of a series of connection SMs that combine two fundamental converter configurations, namely, SEPIC and Cuk. The Dual-Isolated SEPIC/CUK (DISC) SM needs very small input capacitance to keep the input current constant, which will improve the reliability of the system. In addition, the DISC SM allows for employing small-sized high-frequency transformers to provide galvanic isolation between the PV arrays and the ac output side. A comparison of the proposed new structure of DISC SM and classic DISC SMs reveals that the former improves safety and avoids the formation of current spike issues. The improved structure is accomplished by employing an active switch and two diodes to the output side. Replacing the two active switches in the classic structure of DISC SMs with diodes minimises the complexity of the operation as well as the switching losses. Furthermore, as the new output switch operates at the grid's 50/60 Hz frequency, the switching losses will be significantly decreased. The proposed SM in this work uses fewer switches and drivers without compromising the capability of generating the desired output voltage without short-circuit problems. Thus, the SM's conduction losses can be reduced, leading to improved overall efficiency and higher power density. The SMs used in TPMI are promising for PV applications and appropriate connection in a DC–AC grid because they reduce

losses and increase inverter reliability. The proposed inverter transient and steady-state dynamics are studied to obtain voltage/current equations, voltage conversion ratios, and passive component de-sign formulae. Simulations and experiments were conducted on the inverter topology to show the operation and validate the theoretical analyses.

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