

# Progress in cooling nanoelectronic devices to ultra-low temperatures

A. T. Jones,<sup>1</sup> C. P. Scheller,<sup>2</sup> J. R. Prance,<sup>1,\*</sup> Y. B. Kalyoncu,<sup>2</sup> D. M. Zumbühl,<sup>2</sup> and R. P. Haley<sup>1</sup>

<sup>1</sup>*Department of Physics, Lancaster University, Lancaster, LA1 4YB, UK*

<sup>2</sup>*Department of Physics, University of Basel, CH-4056 Basel, Switzerland*

Here we review recent progress in cooling micro/nanoelectronic devices significantly below 10 mK. A number of groups worldwide are working to produce sub-millikelvin on-chip electron temperatures, motivated by the possibility of observing new physical effects and improving the performance of quantum technologies, sensors and metrological standards. The challenge is a longstanding one, with the lowest reported on-chip electron temperature having remained around 4 mK for more than 15 years. This is despite the fact that microkelvin temperatures have been accessible in bulk materials since the mid 20th century. In this review we describe progress made in the last five years using new cooling techniques. Developments have been driven by improvements in the understanding of nanoscale physics, material properties and heat flow in electronic devices at ultralow temperatures, and have involved collaboration between universities and institutes, physicists and engineers. We hope that this review will serve as a summary of the current state-of-the-art, and provide a roadmap for future developments. We focus on techniques that have shown, in experiment, the potential to reach sub-millikelvin electron temperatures. In particular, we focus on on-chip demagnetisation refrigeration. Multiple groups have used this technique to reach temperatures around 1 mK, with a current lowest temperature below 0.5 mK.

Keywords: Nanoelectronics; Ultra-low temperatures; Dilution refrigeration; Adiabatic nuclear demagnetization

## 1. Introduction

Millikelvin electronic measurements of micro/nanoscale devices and materials are used in a wide range of fields; from quantum technology, materials science and metrology to observational astrophysics and dark matter searches. In some cases, physical effects emerge at low temperature that provide a new and useful electronic behaviour, such as superconductivity or conductance quantisation. In other cases, low temperatures provide a “quiet” environment that can, for example, improve the signal-to-noise ratio of sensitive detectors or increase the coherence time of qubits. Regardless of the goal, or the refrigeration technology used, it remains challenging to cool the conduction electrons in a nanoscale device or material significantly below 10 mK. As the temperature drops, the thermal coupling between conduction electrons and the host lattice weakens and the heat capacity of the electronic system falls. This makes the electron temperature more sensitive to parasitic heating. In a nanoscale structure, where the physical size already limits the electronic heat capacity, it is very challenging to maintain low electron temperatures against the incoming heat from electromagnetic radiation, eddy-current heating, nearby hot insulators, and the electronic connections needed for measurement. This review outlines the current progress in cooling nanoelectronic systems below 10 mK, and the potential for new techniques to reach electron temperatures deep in the microkelvin regime.

The ability to access low-millikelvin or microkelvin

temperatures in nanoelectronic structures brings the exciting possibility of unexpected discoveries in a new regime. But there are also immediate goals that motivate much of the work we discuss here. Low electron temperatures are needed to observe new predicted electronic phases, including exotic quantum Hall states [1–5], topological insulators [6], collective electron-nuclear spin states [7–10], insulating ground states in 2D systems [11, 12] and superconductivity in some materials [13]. In established applications, lower electron temperatures may improve coherence times of semiconductor and superconducting qubits [14–16] and hybrid Majorana devices [17–19], as well as reducing error mechanisms in metrological standards such as charge pumps [20, 21] and quantum Hall resistance standards [22].

This review focuses on cooling techniques that we know to have successfully produced on-chip electron temperatures significantly below 10 mK in experiment. We will not discuss emerging refrigeration techniques, such as micro/nanoscale electronic coolers, that may be able to reach ultralow temperatures but have not yet done so in experiment. More information on micrometer-scale refrigeration can be found in recent reviews such as [23, 24]. We will also not discuss ultralow temperature thermometry in detail, although this is obviously an important and relevant topic. Information about the current state of metrology in ultralow temperature thermometry can be found in [25]. More information about techniques that are particularly relevant to micro/nanoelectronic devices at ultralow temperatures can be found, for example, in [26–28] for noise thermometry, [29–32] for Coulomb blockade thermometry and [33–35] for quantum dot-based thermometry. Almost all of the work discussed below makes use of one or more of these thermometry techniques.

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\* [j.prance@lancaster.ac.uk](mailto:j.prance@lancaster.ac.uk)

## 2. Cooling techniques and heat flow in nanoelectronic devices

When trying to cool micro/nanoelectronic devices to ultralow temperatures, experimentalists are faced with several unfavourable physical scaling laws: the heat capacity of the conduction electrons falls with temperature, as does their thermal coupling to other electronic systems and to phonons in the host lattice. To achieve an electron temperature  $T_e$  that is close to the base temperature of the surrounding environment, parasitic heat leaks into the conduction electrons need to be carefully managed. What this means quantitatively depends on the details of each sample and how it is coupled to its local environment; however, the scaling laws, discussed in more detail below, demonstrate the extent of the challenge of moving to lower temperatures. As a trivial example, consider a device that has been well-thermalised to a refrigerator operating at 10 mK by cooling through bond wires and keeping the total parasitic heat leak below 1 fW. The same device could require a total heat leak below 10 aW to stay similarly well-thermalised to a refrigerator operating at 1 mK. In this section, we outline a general thermal model for an on-chip conductor at low temperatures and use this model to illustrate the various cooling techniques that can be employed to reach on-chip electron temperatures below 10 mK.

### 2.1. Thermal model

The thermal model is outlined in Fig. 1. It shows several channels that are available to remove heat from the conduction electrons in an on-chip material. The thermal resistances of the channels are temperature dependent and so the optimal way to cool the electrons will also change with temperature. The details of the thermal resistance for each cooling channel may be different in different samples, but the illustration in Fig. 1 is often a useful approximation and could apply to, for example, conduction electrons in a semiconductor nanostructure or in a thin-film metal circuit. In the following discussion we use the simple example of a metal conductor on the surface of an insulating substrate.

In the first instance, conduction electrons in an on-chip material are coupled to phonons and spins in the same material. In many commonly-used metals and semiconductors, the low-temperature thermal coupling between conduction electrons at temperature  $T_e$  and phonons at temperature  $T_p$  is given by the heat flow

$$\dot{Q}_{ep} = \Sigma V (T_e^5 - T_p^5), \quad (1)$$

where  $\Sigma$  is a material-dependent coupling constant and  $V$  is the volume of the material. Note that the exponent of the temperatures in this equation is commonly accepted to be 5 in many materials [36–38], however in some systems, particularly those confined to fewer

dimensions, it has been observed to take other values  $2 < n \leq 5$  [29, 31]. Typical values of  $\Sigma$  measured below 1 K range from  $\sim 0.01 \times 10^9 \text{ W m}^{-3} \text{ K}^{-5}$  in doped semiconductors to  $\sim 1 \times 10^9 \text{ W m}^{-3} \text{ K}^{-5}$  in metals [23].

If the on-chip material contains spinful nuclei, heat will flow between the nuclear spin bath and conduction electrons through spin-lattice relaxation. In the limit of small nuclear Zeeman splitting ( $g_n \mu_n B \ll k_B T$ , where  $g_n$  is the g-factor,  $\mu_n$  is the nuclear magneton and  $B$  the magnetic field), the spin-lattice relaxation rate  $\tau_1^{-1}$  is proportional to  $T_e$  and characterised by the Korringa constant  $\kappa = \tau_1 T_e$  [39]. Also in this limit, the heat capacity of the nuclei is above the Schottky anomaly and follows  $C_n \propto B^2/T_n^2$ . The thermal coupling between conduction electrons and the nuclear spin bath at temperature  $T_n$  is then given by the heat flow [40, 41]

$$\dot{Q}_{en} = \frac{\lambda_n n B^2}{\mu_0 \kappa T_n} (T_e - T_n), \quad (2)$$

where  $\lambda_n$  is the molar nuclear Curie constant of the material,  $n$  is the number of moles and  $\mu_0$  is the permeability of free space. Equation 2 has been experimentally verified in a broad range of metals and semiconductors [36] and we will assume that it is valid in the following discussion. However, it should be noted that deviations from the Korringa law, which invalidate Equ. 2, have been observed in some metallicly-doped semiconductors below 10 K in the disordered, interacting regime [42], semiconductors doped close to the metal-insulator transition [43] and Kondo metals [44].

The thermal model in Fig. 1 shows an on-chip material that contains a thermal bath of nuclear spins. The same basic model could also apply to a material that contains paramagnetic impurities. In this case, the nuclear spin bath is replaced by a bath of electron spins bound to impurities or dopants. The thermal resistance between these spins and the conduction electrons will be determined by the spin relaxation time. The heat capacity of the spin bath is likely to include a Schottky anomaly in the millikelvin temperature range [45].

While the heat flows described by Equ. 1 and 2 redistribute energy between the thermal subsystems of an on-chip material, the thermal resistances  $R_{WF}$  and  $R_K$  determine how well the material is coupled to the outside environment. The thermal resistance  $R_{WF}$  represents electronic heat conduction through the electrical connections to a device. It is related to the electrical resistance  $R$  of the connection via the Wiedemann–Franz law

$$R_{WF} = \frac{3}{\pi^2} \left( \frac{e}{k_B} \right)^2 \frac{R}{(T_e + T)/2}, \quad (3)$$

where  $T$  is the temperature of the outside environment. In practice, the value of  $R$  can be chosen across a wide range. The resistance of a single gold bond wire, including contact resistance, can be less than 10 m $\Omega$  at low temperatures [46]. On the other hand, the electrical re-

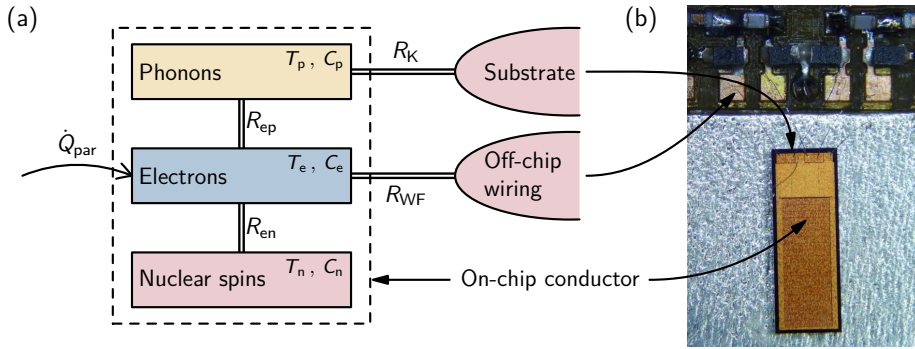


Fig. 1. Thermal model of an on-chip conducting material at low temperature. The on-chip conductor [dashed box in (a)] contains three thermal subsystems: phonons, conduction electrons and nuclear spins, with heat capacities  $C_p$ ,  $C_e$ ,  $C_n$  and temperatures  $T_p$ ,  $T_e$ ,  $T_n$  respectively. Heat flow between the subsystems is determined by temperature differences and the thermal resistances  $R_{ep}$  and  $R_{en}$ . The conductor sits on an insulating substrate, which is assumed to be macroscopic and in thermal equilibrium with the base temperature of an external refrigerator. The thermal resistance between the conductor and the substrate is the phonon boundary (Kapitza) resistance  $R_K$ . The conductor is electrically connected to off-chip wiring, which is also assumed to be well-thermalised with the external refrigerator. The thermal resistance  $R_{WF}$  between on-chip electrons and electrons in the wiring is determined by the electrical resistance of the connection. (b) illustrates the location of each component in an optical image of a typical device on a low-temperature sample mount.

sistance can easily be increased above  $10\text{ k}\Omega$  by including on-chip thin-film resistors or tunnel junctions [47–50].

The final component of the thermal model is the phonon boundary (Kapitza) resistance  $R_K$ , which is typically between the on-chip conductor and the substrate. The value of  $R_K$  depends on the substrate material and the on-chip material, as well as the microscopic properties of the interface [51]. The boundary resistance roughly scales as  $R_K \propto T^{-3}$  with a prefactor that depends on the acoustic mismatch between the two materials, the strength of scattering at the interface and the area  $A$  of the interface. For common metals (including Al, Cu, Au, In) on insulating substrates (Sapphire, Quartz, Si) expected values are  $AR_K T^3 \sim 10^{-2}\text{ K}^4\text{ m}^2\text{ W}^{-1}$  [51]. Because it is difficult to control the quality of interfaces in experiment, a precise prediction of  $R_K$  is rarely possible. However, at ultralow temperatures it is common to find  $R_{ep} \gg R_K$  and therefore cooling of the conduction electrons through phonon channels is not limited by  $R_K$ . In some samples, for example a semiconductor 2D electron gas, the conduction electrons are inside the substrate material and couple directly to the substrate phonons. In this case,  $R_K$  may be omitted from the thermal model or it may be used to represent the boundary resistance between the substrate and its support.

All of the thermal channels shown in Fig. 1 have temperature-dependent thermal resistances. Figure 2 shows predicted values of the corresponding thermal conductances for two example situations. In the first example, shown in Fig. 2(a), a thick ( $\sim \mu\text{m}$ ) on-chip copper film has a low-resistance electrical connection to some off-chip wiring. Both the external wiring and substrate chip are assumed to be macroscopic and well-thermalised with the refrigerator. Above  $\sim 1\text{ K}$ , the on-chip conduction electrons are primarily coupled to the refrigerator through phonons. At lower temperatures, the phonon

channel closes rapidly and the bond wire provides the strongest thermal connection to the refrigerator. At temperatures  $\ll 1\text{ K}$ , cooling of the on-chip electrons will mostly happen through the bond wire, with a base electron temperature determined by the parasitic heating  $\dot{Q}_{par}$  and the thermal resistance  $R_{WF}$ . The second example, shown in Fig. 2(b), is a similar system but with a  $0.1\text{ T}$  magnetic field present and  $10\text{ k}\Omega$  electrical resistance added between the external conductor and the on-chip copper. In this case, the magnetic field increases the thermal coupling between the conduction electrons and the spin-3/2 nuclei in the copper, and the electrical resistance is large enough to thermally isolate the conduction electrons from the off-chip wiring across the whole temperature range. This example shows that, for some devices, the conduction electrons can be most strongly coupled to other on-chip thermal subsystems at ultralow temperatures. It also demonstrates the challenge of cooling high-impedance devices such as single-electron transistors (SETs) or semiconductors with resistive ohmic contacts. Comparing the two examples in Fig. 2, the parasitic heating would need to be  $10^6$  times smaller for the high-impedance case to reach the same electron temperature as the low impedance case.

The steady-state electron temperature in the thermal model is only determined by thermal resistances, the amount of parasitic heating and the temperature of the cold reservoir (refrigerator). However, the heat capacities of the various subsystems are needed to understand any dynamic behaviour. Figure 3 shows how the heat capacities of two example materials vary with temperature between  $3\text{ K}$  and  $100\ \mu\text{K}$ . The heat capacity of the conduction electrons falls linearly with temperature, making the instantaneous on-chip electron temperature more sensitive to intermittent sources of heat. In the case of undoped silicon, shown in Fig. 3(b), its total heat capac-

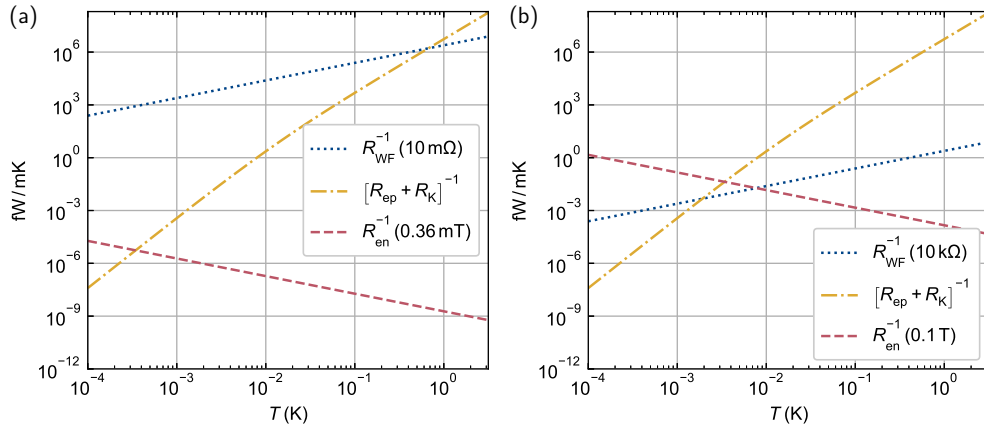


Fig. 2. Predicted thermal conductances for the model shown in Fig. 1 in two example situations. In both, the on-chip conductor is a copper film of size  $205 \mu\text{m} \times 38.5 \mu\text{m} \times 5 \mu\text{m}$  (similar to the device in [52]). Its substrate is a silicon chip, which is assumed to be well-thermalised to the external refrigerator at temperature  $T$ . In (a), the on-chip electrons are electrically connected to well-thermalised external wiring through a low-resistance ( $10 \text{ m}\Omega$ ) bond wire. This path provides the strongest thermal connection to the electrons for  $T \ll 1 \text{ K}$ . No external magnetic field is applied and the internal magnetic field is assumed to be  $0.36 \text{ mT}$ , the effective dipolar field in copper. In (b), the resistance of the electrical connection is  $10 \text{ k}\Omega$  and a magnetic field of  $0.1 \text{ T}$  is applied. As a result, coupling between the on-chip electrons and the external refrigerator is much weaker for  $T \ll 1 \text{ K}$  and, below a few millikelvin, the nuclear spin bath in copper becomes strongly coupled to the electrons.

ity drops all the way down to  $100 \mu\text{K}$ , where it reaches a value  $\sim 10^{10}$  times smaller than the room temperature phonon heat capacity. The situation is different in copper, as shown in Fig. 3(a), because its total heat capacity is boosted below  $\sim 1 \text{ mK}$  by the presence of a nuclear spin bath. The nuclear heat capacity grows with applied magnetic field, moving the crossover to higher temperatures. At ultralow temperatures, the heat capacity of copper will be dominated by this contribution, even with zero applied magnetic field due to the internal magnetic field  $b = 0.36 \text{ mT}$  [36]. The heat capacity of the nuclear spin bath can be used to stabilise the electron temperature [since  $R_{\text{en}} \ll R_{\text{ep}}$ , as shown in Fig. 2(b)] and even to cool the electrons through demagnetisation refrigeration, as discussed in later sections.

## 2.2. Parasitic heat leaks and electrical filtering

Eliminating parasitic heat leaks is one of the major challenges in cooling nano-electronic devices down to ultra low temperatures. Material heat release, microwave radiation from higher temperature stages of the dilution refrigerator as well as RF and low frequency noise coupling to the sample through its electrical leads are well known sources of parasitic heating. The main countermeasures include installation of radiation shields, thermal anchoring of the sample leads at multiple temperature stages of the dilution refrigerator, elimination of ground loops and, in particular, intensive microwave filtering. Various different filtering approaches have been proposed in the literature, a summary of which can be found in [53]. These designs include metal powder filters [33, 54–56], micro-fabricated filters [57–60], thermo-

coax cables [61, 62], copper ‘tape worm’ filters [63, 64], thin film filters [65] and lossy transmission lines [66].

Depending on the application, specific filtering designs may have advantages over others, for example the use of  $50 \Omega$  characteristic filters [55] when impedance matching is crucial, or dissipative cryogenic filters with zero dc resistance [63] for low impedance devices. Thermocoax cables [61, 62] provide very strong attenuation in the microwave and THz regime, and can be used as signal wires from room temperature down to the mixing chamber. However, thermalisation of the inner conductor carrying the measurement signal is rather challenging, and filtering in the MHz regime is not as effective. Therefore a combination of thermocoax cables for the high frequency range and, for example, low cut-off frequency silver-epoxy microwave filters with improved thermalisation [33], as used for microkelvin experiments at the University of Basel (see Fig. 4), ensures good filtering throughout the relevant frequency range and optimal thermal anchoring.

## 2.3. Cooling techniques

The combination of higher thermal resistances and lower electronic heat capacity makes it difficult to reach on-chip electron temperatures below  $10 \text{ mK}$  using standard experimental techniques in a dilution refrigerator. The most common approach, which works well at higher temperatures, is to ensure that the substrate and external wiring are well thermalised through solid contact with the coldest stage of the refrigerator, and to reduce parasitic heating and dissipation in the device as much as possible. Often, the latter requires careful filtering of electrical noise in the incoming wiring. For successful examples

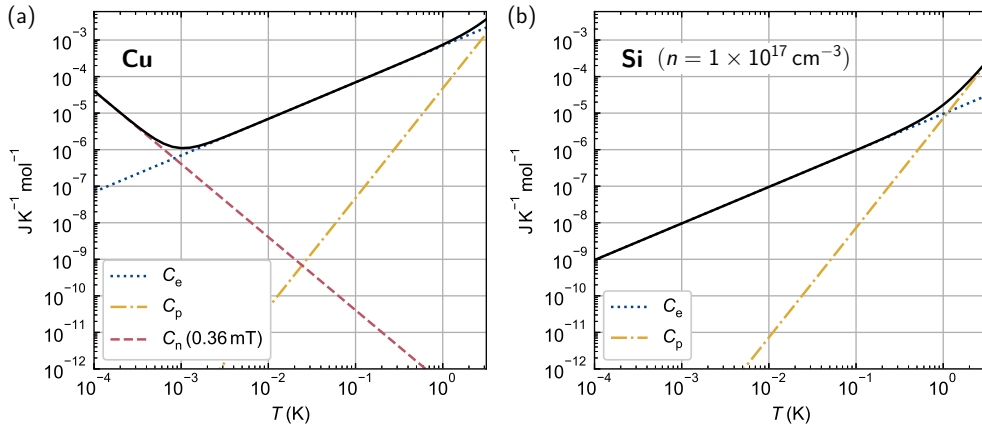


Fig. 3. Molar heat capacities of copper and silicon at low temperatures. (a) Total heat capacity (solid line) of copper, which is the sum of contributions from conduction electrons  $C_e$ , phonons  $C_p$  and nuclear spins  $C_n$ . (b) Total heat capacity (solid line) of undoped silicon in zero applied magnetic field with a free electron concentration of  $1 \times 10^{17} \text{ cm}^{-3}$ . This could be, for example, silicon in the channel of an accumulation-mode FET. In both materials,  $C_p$  is insignificant for  $T \ll 1 \text{ K}$ . Even in zero applied magnetic field, the total heat capacity of copper is dominated by  $C_n$  for  $T \ll 1 \text{ mK}$ . The contribution from  $C_n$  grows as the square of applied magnetic field.

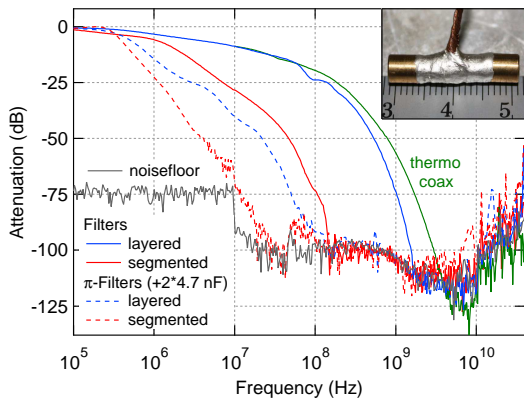


Fig. 4. Room temperature attenuation characteristics of a 1.5 m long thermocoax cable (green) and different silver epoxy microwave filters. Blue and red represent layered and segmented filters, respectively, where the segmented filters have reduced parasitic capacitance. For the dashed characteristics, a 4.7 nF discoidal capacitor from Pacific Aerospace [67] was added to both filter ends. A picture of a silver epoxy microwave filter and centimetre scale bar is shown in the inset. This figure was taken from [33].

demonstrating  $6 \text{ mK} \lesssim T_e \lesssim 10 \text{ mK}$ , see [33, 34, 68–72]. Reaching significantly lower on-chip electron temperatures requires a different approach to thermalising the sample and different refrigeration technology, since even the best dilution refrigerators are limited to temperatures above 1 mK [73].

Demagnetisation cooling is, at present, the most widely used technique for cooling bulk materials below the base temperature of a dilution refrigerator. It is used in low temperature laboratories [74] and has been applied, although much less widely, to cool micro/nanoelectronic devices. It is an application of the magnetocaloric effect,

first discovered in iron in 1883 [75], whereby the temperature of a suitable material can be changed upon the application of a magnetic field. This occurs in materials that are paramagnetic by virtue of an electronic magnetic moment or as a result of the nuclear spin. Nuclear paramagnets are most relevant for the temperature range discussed in this review, and the corresponding cooling technique is known as adiabatic nuclear demagnetisation.

The principle of demagnetisation cooling is well established. For overviews, see for example [36, 41, 74]. Here we provide a brief outline for those unfamiliar with the topic to aid understanding of later sections. Nuclear demagnetisation refrigeration operates by controlling the Zeeman splitting of the nuclear spin energy levels in an applied magnetic field. For small magnetic fields, the Zeeman splitting is much less than the thermal energy  $k_B T$ , leading to a random spin-orientation distribution throughout the refrigerant. This gives an entropy contribution of  $S = R \ln(2I + 1)$ , for  $R$  the ideal gas constant and  $I$  the nuclear spin. In suitable materials [76], where this is the dominant entropy contribution, a significant entropy reduction can be obtained by ordering the spin orientations in a large magnetic field. This can be used as part of a cooling technique by first applying a magnetic field of  $\sim 10 \text{ T}$  and then waiting for the nuclear spins to thermalise to the base temperature of a dilution refrigerator (a process termed precooling). The refrigerant is then thermally isolated from the mixing chamber of the dilution refrigerator, allowing it to remain at approximately constant entropy, and the magnetic field is swept down, producing cooling.

The molar nuclear spin entropy is approximately [77]

$$S \approx R \ln(2I + 1) - \frac{\lambda_n}{2\mu_0} \left( \frac{B}{T_n} \right)^2. \quad (4)$$

This shows that the entropy is entirely a function of

$B/T_n$ , meaning that the minimum attainable final temperature is given by  $T_f = T_i B_f / B_i$ , where  $T_i$  is the initial nuclear temperature, and  $B_i$  &  $B_f$  are the initial and final magnetic fields, respectively. Note that the total magnetic field consists of the externally applied field  $B_{\text{ext}}$  and the effective nuclear internal field  $b$ , which arises from the magnetic dipole interactions in the nuclei. These fields combine to give the total field  $B = \sqrt{B_{\text{ext}}^2 + b^2}$ .

Cooling by demagnetisation often uses elaborate refrigeration stages [74] on state of the art, custom-built dilution refrigerators [73], or vibration isolated systems on commercial, cryogen-free dilution refrigerators [78, 79]. While these systems can readily reach bulk electron temperatures  $\sim 100 \mu\text{K}$ , it is not straightforward to use them to cool a nanoelectronic sample to similar temperatures. In the remainder of this review, we will discuss recently developed techniques that can be used to overcome some of the challenges and effectively apply demagnetisation refrigeration to micro/nanoelectronic devices and samples.

### 3. Immersion cooling

In the context of low temperature micro/nanoelectronic devices, immersion cooling means immersing parts of the experiment, including the device, in liquid helium to improve thermal contact with the coldest stage of a refrigerator. This coldest stage may be the liquid helium refrigerant inside the mixing chamber of a dilution refrigerator or the solid refrigerant of a demagnetisation refrigerator. The helium in the immersion cell may be either  $^3\text{He}$ ,  $^4\text{He}$ , or a mixture of the two and, depending on the working temperature, may be in either the normal state or the superfluid state. Thermal contact to liquid in the immersion cell is often improved by the use of sintered metal-powder heat exchangers, which provide an extremely large solid/liquid contact area to counteract the boundary resistance at the solid/liquid interface [36, 80]. For example, a sintered silver heat exchanger with a volume of a few cubic centimetres may have a contact surface area  $\sim 10 \text{m}^2$  [81]. In the context of the thermal model discussed above, immersion cooling can be used to ensure that the substrate, off-chip wiring and the sample environment (which contributes to  $\dot{Q}_{\text{par}}$ ) are all well thermalised at the base temperature of a refrigerator.

Immersion cooling has been used to thermalise micro/nanoelectronic devices to the base temperature of dilution refrigerators [5, 12, 31, 35, 82, 83] and demagnetisation refrigerators [11, 46, 84, 85]. In all cases where a separate immersion cell is used, sintered metal powder heat exchangers are used to make thermal contact between the helium in the cell and the cold metal parts of the refrigerator. In many cases, sintered silver heat exchangers in the immersion cell are also used to make good thermal contact with the off-chip wiring [5, 11, 12, 31, 46, 82, 84, 85]. The aim is to cool on-chip electrons through

electronic heat conduction, exploiting the  $T^{-1}$  scaling of the electronic thermal resistance (Equ. 3) in preference to the  $T^{-4}$  scaling of the electron-phonon thermal resistance (Equ. 1). This approach is particularly effective for samples with a low electrical contact resistance, and optimising sample fabrication for lower resistances can produce lower base electron temperatures [46].

Despite significant efforts, electron temperatures reached with immersion cooling are rarely below  $\approx 4 \text{mK}$ . Pan, Xia, Tusi and co-workers [84, 85] found an electron temperature of 4 mK in a GaAs/AlGaAs 2D electron gas using a  $^3\text{He}$  immersion cell cooled by a PrNi<sub>5</sub> nuclear demagnetisation stage. Some of the same authors have also reported temperature-dependent behaviour down to 0.5 mK in a similar experiment [11]. At Lancaster University, Bradley et al. [31] reached an electron temperature of 3.7 mK in an experiment where a Coulomb blockade thermometer (CBT) was placed in the mixing chamber of a dilution refrigerator, rather than in a separate immersion cell. A  $^3\text{He}$  immersion cell cooled by a copper nuclear demagnetisation stage has been used to reach an electron temperature below 2 mK in a 2D electron gas, as measured using current-noise-sensing thermometry [46]. While successful, experiments of the type described above require custom-made or significantly customised refrigerators. Nicolí et al. [35] developed an immersion cell to reach an electron temperature of 6.7 mK in a gated, GaAs/AlGaAs quantum dot in a commercial, cryogen-free dilution refrigerator. While still technically challenging, this experiment did not require significant modification of the dilution refrigerator (for example, opening the mixing chamber) and no additional magnetic cooling stage was added.

In principle, immersion cooling can be used to reach low-millikelvin electron temperatures in a commercially-available dilution refrigerator. However, if significantly lower temperatures are needed, it is also necessary to employ nuclear demagnetisation refrigeration. In the following section, we describe how demagnetisation cooling can be used to directly refrigerate off-chip wiring, potentially bypassing the need for an immersion cell.

### 4. Demagnetisation refrigeration of electrical contacts

In traditional microkelvin experiments, the measurement wiring is typically thermalised at the lowest temperatures on a single nuclear demagnetization stage by wrapping a long section of wiring but making thermal contact only through a thin layer of electrical (and thus thermal) insulation, preventing undesired electrical shorting. At temperatures below 10 mK, or certainly below 1 mK, this becomes prohibitively inefficient. In this section we summarize the results obtained using networks of demagnetisation stages, where each measurement lead passes through its own nuclear refrigerator (NR). This eliminates the weak cooling link through an electrical insulator

and replaces it with electronic Wiedemann–Franz cooling. The approach has been implemented in three successive versions at the University of Basel. We describe these experimental setups and review measurements of micro/nanoelectronic devices cooled through nuclear refrigeration of their measurement leads. The first two generations of nuclear stages were developed for a Leiden cryogenics MNK wet dilution refrigerator. The third generation was installed on a Bluefors LD dry dilution refrigerator.

A full schematic of the latest (3rd generation) demagnetisation setup, installed on a Bluefors LD refrigerator, is shown in Fig. 5. With increasing generation of demagnetization stage, the lowest electron temperature after demagnetization in the NRs was reduced from 1 mK in [86] to 0.2 mK in [87] and finally to 0.15 mK in [88]. The improvements result mainly from increasing the amount of copper per plate (0.57 mol / 1 mol / 2 mol) while optimizing the geometry for reduced eddy-current heating and increasing the diameter of the silver wires (1.27 mm / 1.27 mm / 2.54 mm) connecting the NRs to silver sintered heat exchanges residing inside the mixing chamber. Finally, the surface area of the silver sintered heat exchangers, as determined from BET surface area analysis [89], was increased from 3 m<sup>2</sup> in the first two generations to 9 m<sup>2</sup> in the third generation. An overview of relevant system parameters for the different generations of demagnetization stage is given in table 1.

Measurement setups on both dilution fridges (wet and dry) use  $\approx 1.5$  m long thermocoax cables from room temperature down to the mixing chamber, which are excellent microwave filters in the few GHz to the high THz regime [33, 61, 62]. The wires are thermally anchored at all relevant temperature stages of the dilution refrigerator. In order to also obtain strong microwave attenuation in the MHz regime, additional home-built Ag-epoxy microwave filters with  $> 100$  dB attenuation for frequencies above  $\approx 200$  MHz are installed at the MC level in both experimental setups. Transmission spectra for the microwave filters and a thermocoax cable for comparison are shown in Fig. 4. The filters consist of  $\approx 2.5$  m of Cu wire with thin insulation, embedded into a conductive Ag-epoxy matrix, thus leading to excellent thermalisation properties in addition to the filtering [33], as demonstrated on a wet dilution refrigerator without a demagnetization stage where electron temperatures of 7.5 mK were obtained in two metallic Coulomb Blockade Thermometers (CBTs).

Three different types of nanoelectronic devices have been investigated on the second generation nuclear stage: quantum dots fabricated on GaAs/AlGaAs heterostructures [91], normal metal-insulator-superconductor tunnel junctions (NIS) [87], and metallic CBTs [29]. All devices were installed at the sample stage located some distance below the NRs and were held at constant magnetic field (zero field in case of the quantum dot and NIS samples and a small finite field in case of the CBTs). The nuclear demagnetization experiments discussed in the following

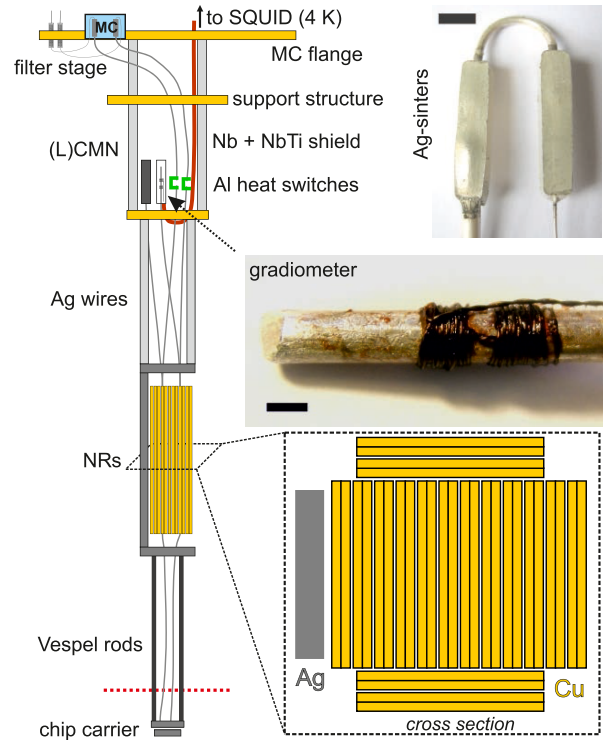


Fig. 5. Schematic of a nuclear demagnetization stage mounted on a Bluefors LD dry dilution refrigerator. The measurement leads are thermalised with Ag powder sinters (*top right picture*, scale bar: 5 mm) in the mixing chamber (MC, blue) and pass through C-shaped Al heat switches (green) to the Cu plates. The gradiometer of a noise thermometer as well as the (L)CMN thermometers are positioned in a region of cancelled magnetic field between the MC and the NR stage. The gradiometer is double-shielded by a Nb tube and an outer NbTi tube (red). *Middle right inset*: photograph of the gradiometer pick-up coil made from insulated Nb wire with 100  $\mu$ m diameter. The  $2 \times 20$  turns are wound non-inductively on a high-purity silver wire which is spot-welded to a NR. Scale bar: 2 mm. *Lower inset*: schematic cross section through the network of 16 parallel NRs. Each NR is 2 mol of Cu (99.99% Cu, low-H<sub>2</sub> content [90], RRR  $\sim 500$ ) and consists of two half-plates, spot-welded together at the top and bottom. Each half-plate is of dimension 3.4 cm  $\times$  0.17 cm  $\times$  12 cm. This figure was taken from [88].

therefore reveal information solely about cooling devices through their electrical contacts.

The GaAs quantum dots were investigated in two modes of operation, direct transport and charge sensing. In the first method, a small source drain bias of  $V_{SD} = 70 \mu$ V was applied to a single quantum dot and the resulting DC current, shown in Fig. 6, was measured as a function of plunger gate voltage  $V_p$  used to shift the quantum dot level with respect to the source and drain chemical potential. In the limit of small tunnelling rates, the temperature broadening of the resulting DC current steps can be fit with a Fermi-Dirac distribution to obtain separately the electronic temperature of the adjacent source and drain leads. Strictly speaking, this

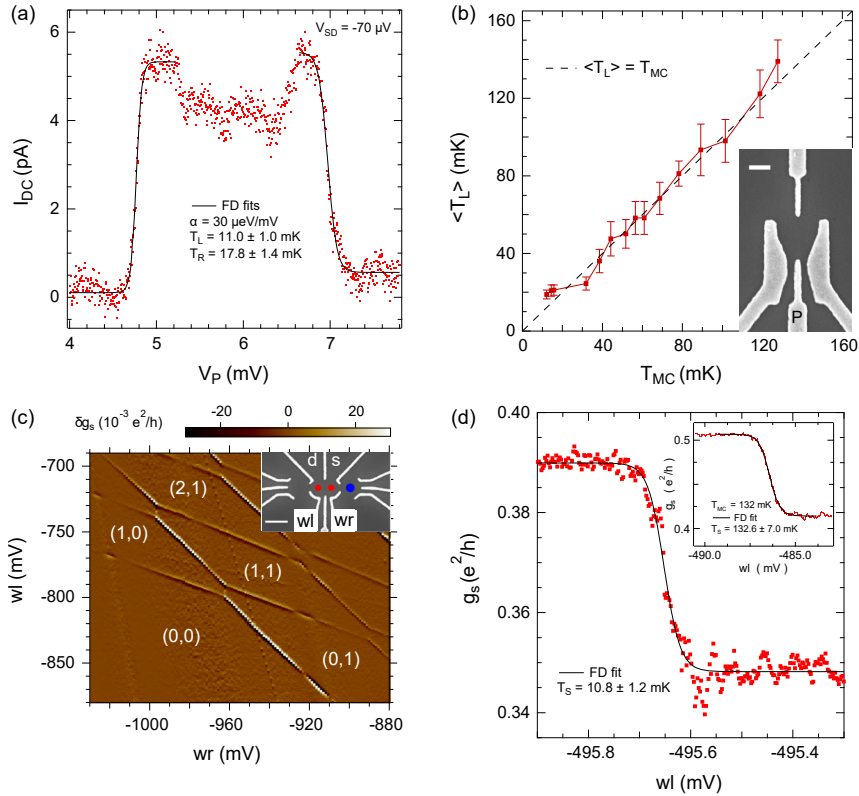


Fig. 6. Electron temperature extracted from direct DC transport (a,b) and charge sensing (c,d) of quantum dots formed at the heterointerface of GaAs/AlGaAs structures. (a) Measured DC current (red dots) along with Fermi-Dirac curve fits (solid black curves). (b) Extracted electron temperature  $T_L$  from measurements as shown in (a) as a function of mixing chamber temperature  $T_{MC}$ . The inset shows a SEM image of a similar device. (c) Charge stability diagram of a double quantum dot similar to the one shown in the inset. (d) Electron temperatures extracted by fitting a Fermi-Dirac distribution to the charge sensing signal at base temperature and  $T_{MC} = 132 \text{ mK}$  are shown in the main panel and inset, respectively. This figure was adapted from [91].

method holds only in two-dimensional systems where the density of states is constant and thus the shape of the current profile (given by the integral over energy of the density of states multiplied by their occupation probability) is determined only by the Fermi-Dirac distribution. In practice, changes in the density of states for 1D and 3D systems are small on the energy scale of a few  $\mu\text{eV}$  such that this analysis is also valid for current leads with any dimensionality (complications may arise from local mesoscopic fluctuations that can induce significant changes in the density of states). The resulting electron temperature obtained from direct DC transport was  $11 \pm 1 \text{ mK}$  at a refrigerator temperature of  $9 \text{ mK}$ .

The second method of quantum dot thermometry relies on charge sensing using the double quantum dot device shown in the inset of Fig. 6(b) (SEM image of a similar device). The charge stability diagram obtained from the sensor quantum dot located on the right-hand-side of the device is shown in Fig. 6(c) and exhibits the typical honeycomb structure for double quantum dots with charge occupation as indicated in the figure. Charge sensing works with arbitrarily low tunneling rates in the dots, allowing them to remain in the temperature broad-

ened regime to arbitrarily low temperatures. Thermometry was carried out by scanning across the (0,0)–(0,1) charge transition line as a function of the right wall [ $wr$  in Fig. 6(c)] gate voltage and fitting the current profile obtained from the sensor quantum dot with a Fermi-Dirac distribution. The lowest electron temperature obtained from 6 consecutive charge sensing traces in this case was  $10.3 \pm 4.4 \text{ mK}$ . These measurements were mainly limited by  $1/f$  noise from the semiconductor wafer.

We note that in contrast to direct transport measurements, where the lever-arm (the conversion between gate voltage and quantum dot energy) can be extracted directly from a single DC bias trace and is given by the width of the current step and applied DC bias, the present method requires high temperature calibration. Here the sample is heated up to a regime where the mixing chamber temperature and electronic device temperature are assumed to agree, which then allows for extraction of the lever-arm from the broadening of the charge transition line. Alternatively, the charge transition line may be also explored as a function of applied DC bias, see [91], resulting in a lever-arm of unity for the given set of parameters, thus eliminating the need for high temper-



ature calibration. Consistent results have been obtained with both approaches. We note two difficulties in measuring ultra-low temperatures using quantum dots. First, due to the small dimensionality of the device, those systems are very susceptible to charge fluctuations in the host waver material, typically on the order of  $1 \mu\text{eV}$  [92], and second, voltage noise in the electrical contacts can translate directly into an elevated electron temperature reading.

Metallic CBTs are simple to use two-terminal devices that allow for precise thermometry down to the few millikelvin regime and below. The devices consist of parallel chains of metallic islands separated by tunnel junctions (usually aluminium oxide). In contrast to quantum dots, which are operated in deep Coulomb blockade, the CBT islands are in the high temperature limit where their charging energy  $E_C$  is comparable to the thermal energy  $k_B T_e$ . The conductance of the CBT exhibits a dip around zero bias, and both the width and the depth of the dip are temperature dependent and can be used for thermometry. The applied AC and DC bias, and any voltage noise, is equally divided between the junctions in each chain of islands on the CBT. This reduces the demands on the environmental noise level compared to quantum dot thermometry. Fig. 7(a) shows the bias dependence of three CBTs with differing total resistance. A full fit to the bias dependence (dashed black curves) delivers the charging energy of the device and the corresponding electron temperature [93].

Higher electron temperatures (14.9 mK / 12.2 mK / 11.4 mK) were obtained for the lower resistance devices (67 k $\Omega$  / 175 k $\Omega$  / 4.8 M $\Omega$ ) during regular operation of the dilution refrigerator, consistent with the notion of better isolation from the environment due to larger resistances. Only little cooling is observed during the off-chip adiabatic nuclear demagnetization (the device resides on a sample holder at compensated magnetic field), lowering the electron temperature of the 4.8 M $\Omega$  device from 11.4 mK to 9.5 mK upon reduction of the Cu-plate temperature from  $\approx 10$  mK to 2 mK. This is not so surprising since Wiedemann–Franz cooling through the sample leads is expected to be effective only for low impedance devices, as illustrated in Fig. 2. Presumably the small temperature reduction upon demagnetization results mainly from the sample holder being cooled by a nuclear refrigerator through a massive, 99.999% pure (5N), silver wire which results in slightly improved cooling of the CBT through its insulating substrate.

Next we review thermometry results from normal metal-insulator-superconductor (NIS) devices. The sharp quasiparticle peak in the density of states of the superconductor provides an ideal probe to measure the thermal broadening of the distribution of occupied states in the adjacent normal metal. In order to do so, an insulator is sandwiched between the normal metal and the superconductor. This is such that the creation of Cooper pairs is highly suppressed, and therefore the resulting DC

current through the device, as a function of bias voltage  $V$ , reflects the superconducting gap. The electron temperature  $T_N^A$  can then be directly extracted by performing a linear fit [solid black lines in Fig. 8(a)] to the onset of the quasiparticle current  $I$  in logarithmic scale, i.e.  $T_N^A = e/k_B \cdot dV/d(\ln I)$  where  $e$  and  $k_B$  are the elementary charge and the Boltzmann constant, respectively. Alternatively, a fit to the full bias profile can be applied [dashed red curves in Fig. 8(a)] to extract the electron temperature of the normal metal as described in detail in [87].

Due to the huge, mm-size macroscopic leads on the NIS device, one could hope for improved off-chip nuclear demagnetization performance compared to the high impedance arrays present in the metallic Coulomb blockade thermometers. Indeed, the electron temperature drops by  $\approx 30\%$  from  $\approx 10$  mK to  $\approx 7$  mK in Fig. 8(b) upon reducing the Cu-plate temperature down to 3 mK, compared to only a  $\approx 15\%$  reduction in temperature in the case of the CBTs in Fig. 7(b). The limiting factor in this case is most likely the RMS voltage noise  $\langle V_N^2 \rangle$  in the measurement leads which couples directly to the chemical potential in the normal metal and translates into an elevated temperature reading if  $\langle V_N^2 \rangle \gg k_B T_e / e$ . In addition, residual perpendicular magnetic fields also lead to a drastic overestimation of the electronic temperature [87].

Table 1 summarizes all the relevant system parameters such as sample mount, nuclear stage dimensions and mass, filtering, sinters and so forth for the three generations of nuclear stage installed on a wet MNK system from Leiden cryogenics (1st and 2nd generation) and on a dry LD system from Bluefors (3rd generation). In addition, an overview is given of the electron temperature measurements performed using quantum dots, NIS devices, and metallic CBTs. Details of the lowest temperature results, which were reached using CBTs on the 3rd generation stage, can be found in section 5.2.

The experiments discussed above show that low-millikelvin on-chip electron temperatures can be successfully reached by magnetic refrigeration of external electrical connections. These experiments also demonstrate that the the base electron temperature is often limited by the device being measured, not the external refrigerator. In the case of quantum dots and NIS thermometers, intrinsic noise (charge fluctuations), extrinsic noise (voltage fluctuations) and residual perpendicular magnetic field (for the NIS thermometer) likely limited the lowest  $T_e$  that could be resolved. In the case of CBTs, their high impedance meant that cooling through electrical connections was less effective. In the following section, we discuss how on-chip magnetic refrigeration can be used to overcome the latter challenge.

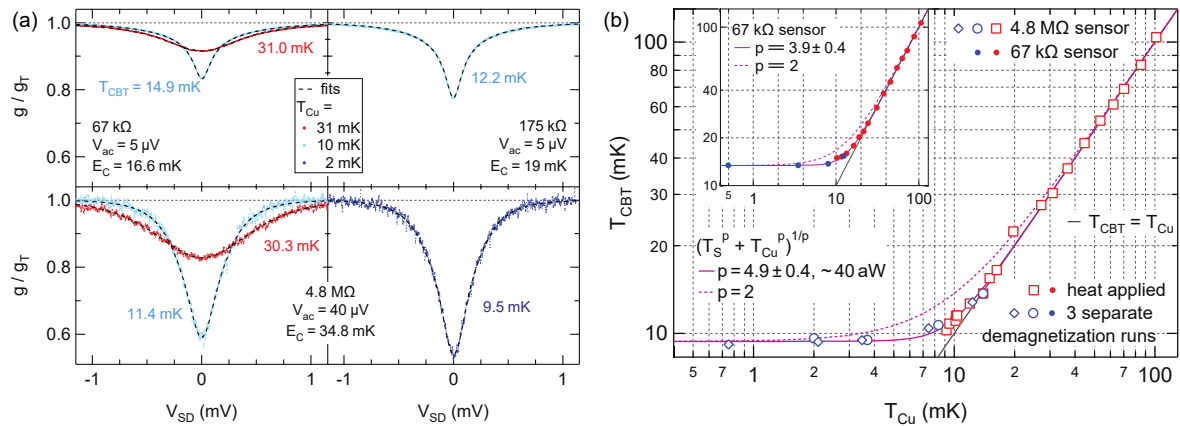


Fig. 7. Thermometry using various metallic Coulomb blockade thermometers with differing resistance. Normalised differential conductance  $g/g_T$  as a function of applied DC bias is shown in panel (a) for various copper plate temperatures  $T_{Cu}$ . Off-chip demagnetization down to  $T_{Cu} = 2$  mK slightly reduces the electronic temperature for the 4.8 M $\Omega$  device from 11.4 mK (light blue) to 9.5 mK (dark blue). (b) Extracted electron temperatures as a function of  $T_{Cu}$ . Open (closed) markers represent the 67 k $\Omega$  (4.8 M $\Omega$ ) device. Data for the red and blue markers were collected during regular dilution refrigerator operation and adiabatic nuclear demagnetization, respectively. This figure was adapted from [29].

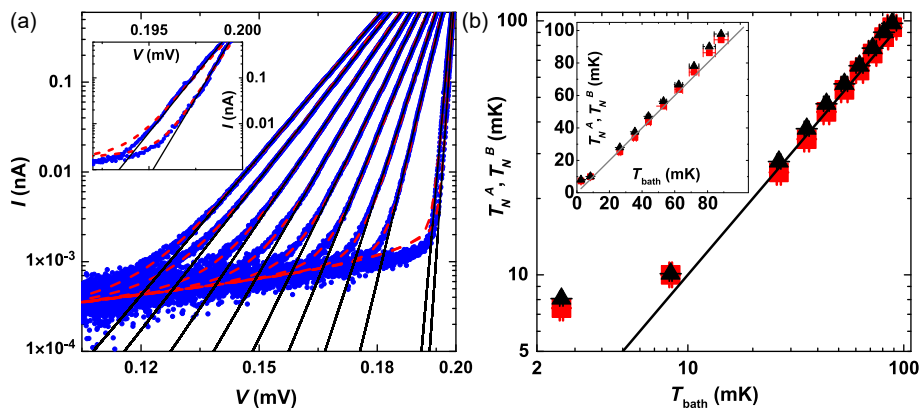


Fig. 8. Normal metal-insulator-superconductor (NIS) tunnel junction thermometry. (a) Linear fits (solid black) to the onset of the measured quasiparticle current (blue dots) in an NIS device. Fits to the full current profile are shown in dashed red. The inset shows a close-up for mixing chamber (bath) temperatures of 10 mK and 7 mK on the left and right, respectively. (b) Extracted electronic temperatures from (a) for the full curve fit and the linear fit are shown as red squares and black triangles, respectively. This figure was adapted from [87].

## 5. On-chip demagnetisation refrigeration

On-chip demagnetisation refrigeration uses a small quantity of refrigerant integrated onto a micro/nanoelectronic device. The refrigerant is electrically connected to the device's conduction electrons, providing a thermal link to the nuclear spins via hyperfine interactions between the nuclei and electrons [36, 95]. This bypasses the electron-phonon coupling bottleneck associated with cooling a sample through its electrically insulating substrate. It also bypasses the weak thermal link to off-chip wiring in high impedance devices.

The earliest observations of on-chip magnetic cooling were made where, instead of using a conventional nuclear demagnetisation refrigerant such as copper, the spin entropy was provided by electronic paramagnetism within

the material of the device structure. In [96], which is an investigation into the anomalous Hall effect in a topological insulator, an unexpected variation in the Hall bar's resistivity was found and ultimately identified as the result of unexpected temperature changes. These temperature changes arose from a magnetocaloric effect in some unknown part of the device. During experiments, the device temperature was reduced to 25 mK from a mixing chamber temperature of 40 mK. This resulted in a very low longitudinal resistance and excellent Hall conductance quantisation. Unexpected cooling has also been observed in measurements of aluminium SETs [97]. In this work, the aluminium was doped with manganese in order to suppress superconductivity, which was undesirable for good device operation. The doping was found to have the side effect of allowing demagnetisation refriger-

Generation stage	1st generation [86]	2nd generation [29, 87]	3rd generation [88]
Refrigerator model	Leiden cryogenics (MNK)	Leiden cryogenics (MNK)	Bluefors (LD)
Wet / dry system	Wet	Wet	Dry
Sample mount	Sample stage	Sample stage	Nuclear stage
Demagnetization	Off-chip	Off-chip	On- & off-chip
# NRs	13	21	16
NR dimensions	$10 \cdot 2 \cdot 0.2 \text{ cm}^3$	$9 \cdot 3.2 \cdot 0.25 \text{ cm}^3$	$2 \cdot (12 \cdot 3.4 \cdot 0.17 \text{ cm}^3)$
Cu NR mass	0.57 mol	1 mol	2 mol
Sinter surface area	$3 \text{ m}^2$	$3 \text{ m}^2$	$2 \cdot 4.5 \text{ m}^2$
Ag wire diameter	1.27 mm	1.27 mm	2.54 mm
Discrete filter @ MC	None	[29] RC 2-pole, 10 kHz BW 820 $\Omega$ /22 nF, 1.2 k $\Omega$ /4.7 nF [87] RC 2-pole, 30 kHz BW 1.6 k $\Omega$ /2.2 nF, 2.4 k $\Omega$ /470 pF	RC 2-pole, 45 kHz BW $2 \cdot [2 \text{ k}\Omega/680 \text{ pF}]$
Lowest NR $T_e$	1 mK Power curves	[29] 0.3 mK / [87] 0.2 mK Power curves	0.15 mK Noise thermometry
Lowest sample $T_e$	Not measured	QD [91]: 10.4 mK CBT [29]: 9.5 mK NIS [87]: 7 mK	CBT [94]: 2.8 mK (1.8 mK in Fig. 13)

Table 1. Comparison of the three different Basel nuclear stages, the first two on the same wet system and the third on a dry system. For all systems  $\approx 1.5 \text{ m}$  of uninterrupted thermocoax cable was used for the measurement wires down to the mixing chamber, at which different cold filters were mounted. For the 3rd generation, two half plates were spot welded together for the purpose of reducing eddy-current heating and two Ag sinters with  $4.5 \text{ m}^2$  surface area were installed for each measurement lead. The lowest electron temperatures for the nuclear stage and sample are indicated in the last two rows.

ation of the SET to 140 mK, down from the 300 mK base temperature of the  $^3\text{He}$  cryostat in which the sample was mounted.

For on-chip cooling to a few millikelvin, the most effective approach to date uses relatively small blocks of metallic refrigerant in direct electrical connection with the circuit elements of a device. Provided the connection has a low enough electrical resistance, the conduction electrons in the device and the refrigerant are essentially a single thermal bath, cooled by demagnetisation of the refrigerant's nuclear spins. A number of demonstrations have been made using CBTs to measure electron temperature during the cooling process, at Lancaster University [52], the University of Basel [94] and Delft University of Technology [98, 99]. The CBT is particularly well suited to the demonstration of magnetic cooling since the operation of the device itself is insensitive to the applied magnetic field [100–102], and it can also be fabricated with conveniently sized metallic islands for the addition of refrigerant, which can be electroplated up to a thickness of  $\sim 10 \mu\text{m}$  [see Fig. 9(a) and (b)]. Electroplating is used to avoid stress build-up in the thick metal film, which often occurs with more conventional deposition techniques (e.g. sputtering or evaporation).

### 5.1. Demagnetisation cooling with only on-chip refrigerant

On-chip nuclear refrigeration was first demonstrated using  $6 \mu\text{m}$  thick copper refrigerant electroplated onto the  $32 \times 20$  metal island array of a CBT device [52]. This sample was pre-cooled to  $T_e \approx 9 \text{ mK}$  using a cryogen-free dilution refrigerator, with a base temperature of 7 mK, in a 5 T magnetic field. When demagnetising from 5 T at a rate of 2.5 mT/s, the CBT conductance was seen to drop as would be expected for a falling on-chip electron temperature. Repeated experiments made with different DC biasing of the CBT confirmed that the conductance change was indeed due to a change in temperature, and not the result of electromagnetic induction. The lowest temperatures reached with such single-rate demagnetisations were  $T_e \approx 5 \text{ mK}$ , significantly below the base temperature of the dilution refrigerator.

Electron temperature data from single-rate demagnetisation experiments were compared to predictions of the thermal model described in section 2. The temperature of the nuclear spins was assumed to reduce adiabatically as the magnetic field was stepped down, with the electrons being cooled by heat flow to these spins in competition with the incoming heat via electron-phonon coupling and parasitic heating. The model was found to be consistent with the electron temperature data in Fig. 9(c) and a dynamic (during the sweep) heat leak of 6.3 fW per island,

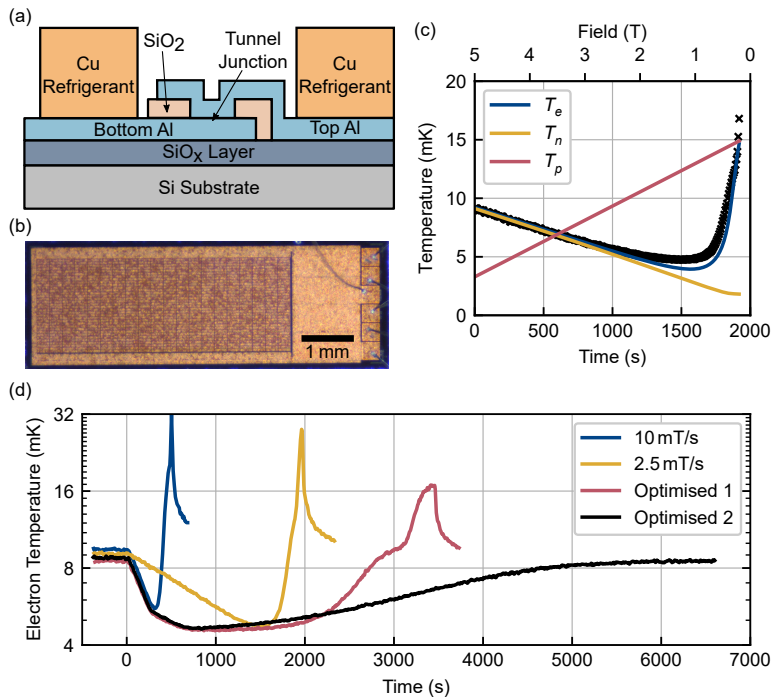


Fig. 9. Demonstration of on-chip demagnetisation refrigeration with copper refrigerant. The CBT device shown schematically in (a) features large ( $6\ \mu\text{m}$  thick) Cu refrigerant blocks applied to an array of metallic islands. A photograph of the  $6.5\ \text{mm} \times 2.3\ \text{mm}$  chip is shown in (b), with the  $32 \times 20$  array of metal islands taking up the left 3/4 of the device. The black crosses in panel (c) show the measured electron temperature during a  $2.5\ \text{mT/s}$  demagnetisation, to which the three subsystem model was fitted, allowing extraction of the phonon and nuclear spin temperatures. Panel (d) shows how the base temperature and hold time were extended by using three different demagnetisation rates instead of one. Details of the demagnetisation profiles ‘Optimised 1’ and ‘Optimised 2’ can be found in [52].

also confirming that the heat flow to the nuclear spins goes as  $B^2$ , as expected from Equ. 2. With the heat leak due to eddy-current heating going as  $(dB/dt)^2$  [36], it was expected that reducing the ramp rate as the demagnetisation proceeded to lower fields would lead to lower base temperatures (see also [103, 104]). The result of this optimisation is shown by the third (red) and fourth (black) traces in Fig. 9(d), in which the latter line shows the benefit of having a larger nuclear heat capacity if the demagnetisation is completely stopped at a higher magnetic field. Optimisation of the demagnetisation profile resulted in a slightly lower base electron temperature of  $4.5\ \text{mK}$  and a significantly longer hold time: around  $1200\ \text{s}$  below  $5\ \text{mK}$ .

As discussed in section 2, the minimum possible temperature that can be reached during adiabatic demagnetisation is set by the initial entropy reduction achieved during magnetisation and precooling. As the entropy is given by Equ. 4, we see that it is favourable to maximise the value of  $B/T_n$  by using larger magnetic fields and lower precooling temperatures. A similar CBT was therefore cooled in a different, Lancaster-built dilution refrigerator with an  $8\ \text{T}$  superconducting solenoid and a base temperature of  $2.3\ \text{mK}$  [105], offering a potential five-fold improvement in  $B/T_n$  over the dry cryostat.

The Lancaster-built cryostat features an openable plastic mixing chamber [106] and sintered silver heat exchangers were added to the mixing chamber to help precool the CBT, as shown in Fig. 10(a) and (b). This cryostat also has the inherent benefit of lower mechanical vibrations because there is no pulse-tube cooler, from which [107] there can be a significant additional heat leak through eddy-current heating [79, 88] and additional electrical noise [108]. The particular dilution refrigerator used for the results shown in Fig. 11 also features extensive vibration isolation and is located within a shielded room which further removes vibrations and electrical noise.

In Fig. 11(a), we see that the transition to a colder dilution refrigerator significantly improved the base electron temperature from  $4.7\ \text{mK}$  to  $2.0\ \text{mK}$  for the unoptimised single-rate demagnetisations, and from  $4.5\ \text{mK}$  to  $1.9\ \text{mK}$  for the optimised multi-rate demagnetisations. The latter case, where a significant magnetic field was held following the demagnetisation in order to maintain significant nuclear heat capacity, also shows a much increased hold time of some  $6000\ \text{s}$  around  $2\ \text{mK}$ . These improvements are further reflected in Fig. 11(b) which shows the quantity  $B/T_e$ , scaled such that its initial value is equal to unity at the start of the wet demagnetisations. As described in section 2, the entropy of the system is entirely a

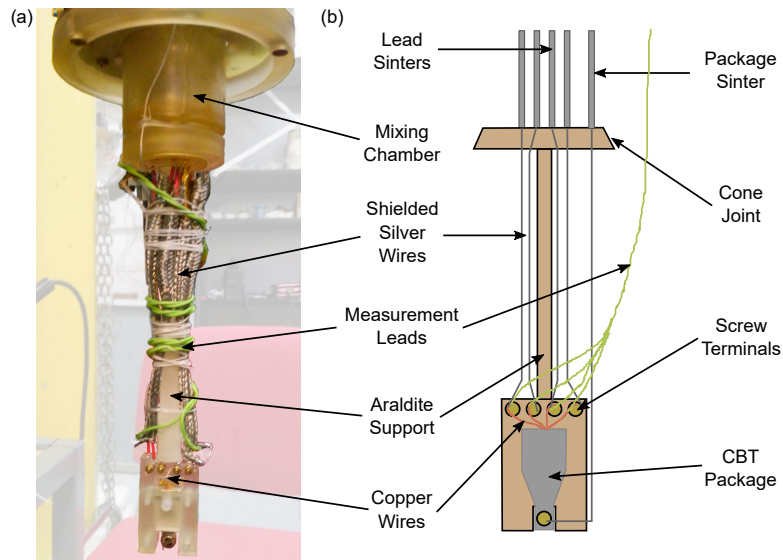


Fig. 10. The ‘coldfinger’ used for precooling a CBT sensor in its package on a dilution refrigerator in Lancaster. Panel (a) shows the coldfinger mated with the mixing chamber hence, when cooled, the sinters shown at the top of the diagram in panel (b) are immersed in the liquid  $^3\text{He}$ - $^4\text{He}$  refrigerant of the dilution refrigerator. Cooling is provided through the silver wire connected to the package and also the shielded silver wires attached to each measurement lead.

function of  $B/T_n$ , and since the electron-phonon coupling here is extremely weak compared to the electron-nuclear spin coupling, we can assume  $T_e = T_n$ . Figure 11(b) therefore shows deviation from the ideal case of constant entropy, which would be represented by a straight horizontal line. There is a clear initial benefit to the use of a cryostat with a lower base temperature and higher field magnet, since this leads to a larger initial  $B/T_e$  value and hence a larger entropy reduction during precooling. We also see that the optimised sweeps are able to avoid the sudden entropy change as the nuclear heat capacity is exhausted at the end of the single-rate sweeps.

Traditionally, the naturally abundant copper isotopes  $^{63}\text{Cu}$  and  $^{65}\text{Cu}$ , both with spin  $I = 3/2$ , have been used for large bulk demagnetisation stages capable of themselves reaching electron temperatures of  $12\ \mu\text{K}$  [109] and cooling liquid helium to  $100\ \mu\text{K}$  [110]. Copper has been widely used both due to its thermodynamic benefits, such as a relatively large nuclear magnetic moment for all isotopes and low temperature of spontaneous magnetic ordering, but also more practical considerations such as the ease at which it can be machined into a desired shape and its good availability in high purity form [36, 74]. However, there are other materials which have some benefits over copper, particularly in terms of the magnitude of the Korringa constant which determines the thermal coupling between the nuclear spins and conduction electrons.

An alternative nuclear refrigerant is indium, which has spin  $I = 9/2$ , nuclear Curie constant  $\lambda_n/\mu_0 = 13.8\ \mu\text{JKT}^{-2}\text{mol}^{-1}$  and Korringa constant  $\kappa = 0.09\ \text{Ks}$ . Indium therefore seems promising when compared to copper, which has smaller  $\lambda_n/\mu_0 = 3.22\ \mu\text{JKT}^{-2}\text{mol}^{-1}$ , and

hence a smaller nuclear heat capacity, and longer Korringa constant  $\kappa = 1.2\ \text{Ks}$  [36], meaning weaker electron-nuclear spin coupling. Yet indium is mechanically soft, features an electric quadrupole interaction, which causes nuclear orientation below  $300\ \mu\text{K}$  [111], and has a superconducting transition at  $28\ \text{mT}$  [112], limiting the lowest temperatures that can be reached during demagnetisations. This means indium has seldom been used for the construction of bulk demagnetisation stages. However, for on-chip cooling, where the refrigerant is applied by electroplating, and the minimum temperatures obtained are currently above  $300\ \mu\text{K}$ , these limitations are not necessarily important.

Yurttagül et al. at Delft University of Technology have demonstrated on-chip magnetic cooling using  $25\ \mu\text{m}$  thick, on-chip indium refrigerant blocks [98]. These blocks were electroplated onto a CBT consisting of a  $35 \times 15$  array of metallic islands. Precooling was performed using a ‘wet’ dilution refrigerator equipped with a  $12.8\ \text{T}$  magnet and reached an initial electron temperature of  $16\ \text{mK}$ . Following a demagnetisation at a rate of  $0.4\ \text{mT/s}$ , a minimum electron temperature of  $3.2\ \text{mK}$  was obtained at a field of  $2\ \text{T}$ , followed by rapid warming to above the initial electron temperature when the magnetic field ramp was stopped at  $40\ \text{mT}$ , similar to what was observed for the unoptimised field sweeps in the copper experiments.

For both the indium and copper on-chip demagnetisations, the minimum electron temperature was found to be heavily influenced by the heat leak into the electrons on each of the CBT islands. This is particularly important since the CBT islands were permanently linked to the mixing chamber of the dilution refrigerator via the

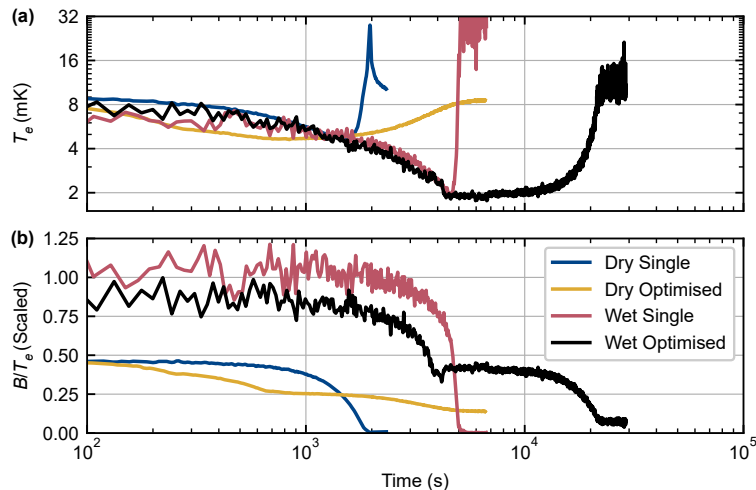


Fig. 11. Comparison of demagnetisation cooling using the same cooling platform on wet and dry dilution refrigerators. Panel (a) shows a comparison of the electron temperatures achieved during single rate and optimised multi-rate demagnetisations on the wet and dry dilution refrigerators. Panel (b) shows a quantity related to the entropy change during the demagnetisations, and therefore shows the amount of deviation from the ideal case of constant entropy.

electron-phonon coupling and conduction through the measurement leads, with no controllable heat switch to break this link during the demagnetisation. While this makes for easy construction of the cooling platform, a penalty is paid in terms of the continuous heat input, particularly from phonons, when the CBT electrons are cooled significantly below the temperature of the fridge. Therefore, one approach for improving the minimum electron temperatures is to thermally isolate the device using a heat switch [113] and to cool the environment surrounding the CBT chip. This has been performed by combining the on-chip demagnetisations with demagnetisation of both the incoming measurement lines and the box the sample is mounted in, as described below.

## 5.2. Magnetic cooling with on-chip and off-chip refrigerant

Coulomb blockade thermometers with on-chip copper refrigerant have been studied in Basel using the 3rd generation magnetic refrigeration stage on a Bluefors LD dilution refrigerator (see section 4 and table 1 for details). In this case, the heat-leak into the cold on-chip islands is reduced by ensuring that substrate phonons and the off-chip wiring are also cooled below the base temperature of the dilution refrigerator.

While dry dilution refrigerators, such as the Bluefors LD, seem to be the future path of low temperature physics, with obvious advantages compared to wet systems such as lower operating costs and independence of the worlds helium production, there are also disadvantages. Stronger magnets are available for wet systems due to the more efficient cooling when immersing the mag-

net directly into liquid helium. Furthermore, the pulse tube coolers used in dry systems introduce higher levels of vibrations, which is detrimental for adiabatic nuclear demagnetization experiments due to vibration induced eddy current heating. It is these vibrations that result in relatively high CBT precooling temperatures in these experiments, as shown in Figs. 12,13. This is the current bottleneck for this setup.

In contrast to previous experiments using the Basel refrigeration stages, here the sample is placed inside a small copper box which is mounted directly onto a nuclear refrigerator while using two other NRs as sample leads. This allows for direct on-chip demagnetization of the copper electroplated CBT islands in addition to off-chip demagnetization. The CBTs are operated in secondary mode, i.e. recording only the zero bias conductance during demagnetization. While this method requires high temperature calibration it comes with the advantage that no DC current passes through the device which otherwise would lead to Joule heating effects. In fact, a single bias trace after demagnetization is sufficient to destroy the nuclear polarization in the Cu-plated CBT islands that was built up during precooling at large magnetic field. The Joule heating effect is already visible at the lowest temperatures obtained in continuous mode operation of the dilution refrigerator without demagnetization, as demonstrated in [33, 94].

The inset in Fig. 12(a) shows the relative conductance dip size  $\delta g = 1 - g(V_{SD})/g_T$  as a function of Cu-plate temperature, where  $g(V_{SD})$  is the differential conductance as a function of applied source-drain bias  $V_{SD}$  and  $g_T$  the temperature-independent high-bias differential conductance. The relative conductance dip size can be approximated by  $\delta g = u/6 - u^2/60 + u^3/630$  where

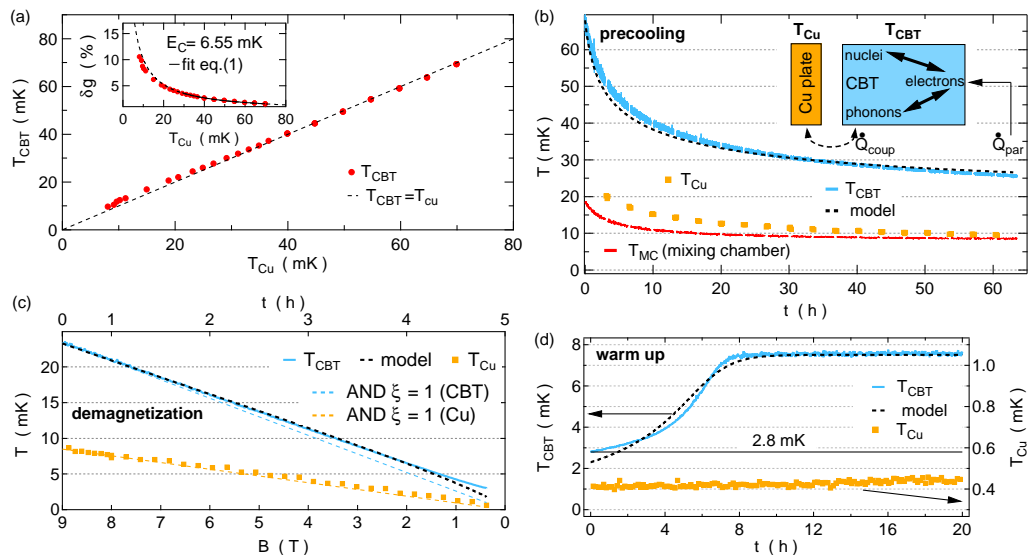


Fig. 12. Nuclear adiabatic demagnetization of a metallic Coulomb blockade thermometer. (a) CBT temperature  $T_{\text{CBT}}$  versus copper plate temperature  $T_{\text{Cu}}$ . The diagonal dashed line indicates ideal thermalisation  $T_{\text{CBT}} = T_{\text{Cu}}$ . The inset shows the normalized zero bias conductance dip  $\delta g$  as a function of  $T_{\text{Cu}}$ . A fit [30] (solid black curve) in the high temperature regime  $T_{\text{Cu}} > 30$  mK is used to extract the charging energy  $E_C = 6.55$  mK. The three steps of nuclear demagnetization, precooling, demagnetization, and warmup, are shown in panels (b), (c), and (d) respectively. Light blue, yellow, and red data indicate  $T_{\text{CBT}}$ ,  $T_{\text{Cu}}$ , and  $T_{\text{MC}}$ , respectively. Black dashed curves in (b-d) are predictions from a thermal model schematically indicated in (b). A light blue line in (c) indicates ideal adiabatic demagnetization. This figure was adapted from [94].

$u = E_C / (k_B T_{\text{CBT}})$  [30]. Therefore a fit to  $\delta g$  in the high temperature regime where  $T_{\text{CBT}} = T_{\text{Cu}}$  allows one to extract the charging energy  $E_C$  as the only free fit parameter. Subsequently, any measured conductance dip can be converted back to an electronic temperature  $T_{\text{CBT}}$  using the previously determined charging energy. The CBT agrees very well with the Cu-plate temperature and only starts to deviate slightly at low temperatures, reaching  $T_{\text{CBT}} = 9.7$  mK at  $T_{\text{Cu}} = 8.1$  mK. Here, for the third generation nuclear stage the Cu-plate temperature is determined directly by noise thermometry. In order to do so a gradiometer (non-inductive coil with 20 clockwise turns following 20 counter clockwise turns) is used to measure the magnetic noise created by the Brownian motion of electrons within a massive 5N silver wire spot-welded to a NR, see Fig. 5. The superconducting wires from the gradiometer are then fed through concentric Nb and NbTi shields up to the 4K stage where a superconducting quantum interference device (SQUID) is used to amplify the small voltage fluctuations. See [88] for more details on this noise thermometry setup.

When precooling the device at a large magnetic field in Fig. 12(b), the CBT reaches a temperature of 24 mK after more than 60 h precooling time, significantly higher than the mixing chamber temperature  $T_{\text{MC}}$  and Cu-plate temperature  $T_{\text{Cu}}$ , which both saturate just below 10 mK. The high precooling temperature is limited by pulse tube vibrations leading to either eddy current induced heating in the CBT islands and/or voltage fluctuations in the measurement wires that are then dissipated through

Joule heating in the sample. The pulse tube vibrations are clearly visible in voltage noise measurements across the device (see supplemental information in [94]) showing up as frequency combs with a 1.4 Hz spacing in-between peaks. In the subsequent demagnetization step in Fig. 12(c) the CBT temperature drops by a factor of 8.6, reaching 2.8 mK at the end of the adiabatic demagnetization. After completing the demagnetization, the CBT immediately starts to warm up in Fig. 12(d), reaching equilibrium at  $T_{\text{CBT}} = 7.5$  mK after roughly 8 h while the external NRs remain at microkelvin temperatures. This highlights the importance of on-chip demagnetization for metallic Coulomb blockade thermometers, and the thermal isolation of the on-chip islands from the off-chip wiring.

In an initial attempt to reduce parasitic heating caused by the pulse tube vibrations, additional fixing mechanisms were introduced, shown in Fig. 13(a). Insulating screws made from PEEK (polyether ether ketone) were used to attach the support structure of the parallel network of nuclear stages with respect to the mixing chamber radiation shield, and a second set of PEEK screws fixed the still radiation shield with respect to the mixing chamber shield.

The CBT device investigated here is nominally the same as in Fig. 12, but mounted perpendicular to the demagnetisation field in contrast to the measurements shown in Fig. 12. The high temperature calibration required for operating the device as a secondary thermometer is shown in the inset of Fig. 13(b), giving a charging

energy of  $E_C = 6.72 \pm 0.04$  mK. Fixing the NRs with respect to MC and still shields, together with an increased precooling time of 140 h results in a CBT temperature of 20.3 mK at the beginning of the adiabatic nuclear demagnetization. In addition, compared to the results in Fig. 12, the ratio of initial and final electron temperature increased from 8.6 to 11.3, giving a final CBT temperature of  $T_{\text{CBT}} = 1.8$  mK in the Bluefors LD system [114].

On- and off-chip demagnetisation refrigeration have also been combined by Sarsby et al. at Delft University of Technology, but with indium as the refrigerant [99]. They employed indium refrigerant blocks electroplated on the islands of a CBT, similar to that used for the on-chip indium investigation [98], but with each of the four electrical measurement lines also passing through a macroscopic indium block in the fridge. Both the CBT and the lead NRs were precooled in a ‘wet’ dilution refrigerator in a magnetic field of 12 T over a period of approximately 7 days, giving a starting temperature of 13 mK. After this, the authors employed a continuously variable demagnetisation rate, proportional to magnetic field, in order to balance the available nuclear cooling power against the eddy current heating. When the demagnetisation ended, at a final field of 100 mT, the CBT electron temperature was 420  $\mu$ K. The electron temperature then remained below 700  $\mu$ K for some 85 hours, owing to a small heat leak of 27 aW per island.

## 6. Conclusions and open questions

Techniques for cooling micro/nanoelectronic devices to ultralow temperatures have progressed significantly in the last five years, largely through the development of new experimental methods based on nuclear demagnetisation refrigeration. By using multiple, macroscopic de-

magnetisation refrigerators to cool the substrate and electrical contacts of a device, and by incorporating microscopic volumes of nuclear refrigerant into a device structure, it is now possible to produce and measure low- and sub-millikelvin electron temperatures on-chip. The continuing development of immersion cells cooled by demagnetisation refrigeration may also provide a solution, particularly for very low impedance devices. Despite these advances, the sensitivity of on-chip electrons to parasitic heating and electrical noise mean that it is still experimentally challenging to get the electrons cold and to perform accurate thermometry. Coulomb blockade thermometers have proven to be an excellent testbed for new cooling techniques, as they provide both reliable thermometry and a degree of built-in protection against electrical noise. It is an open question how these new cooling techniques can be applied effectively to other types of device. Based on the work to-date, it seems unlikely that one single approach to cooling will be effective for every type of micro/nanoelectronic device or sample. It also seems inevitable that careful consideration and design of the on-chip thermal environment will be needed for any experiment where sub-millikelvin electron temperatures are required.

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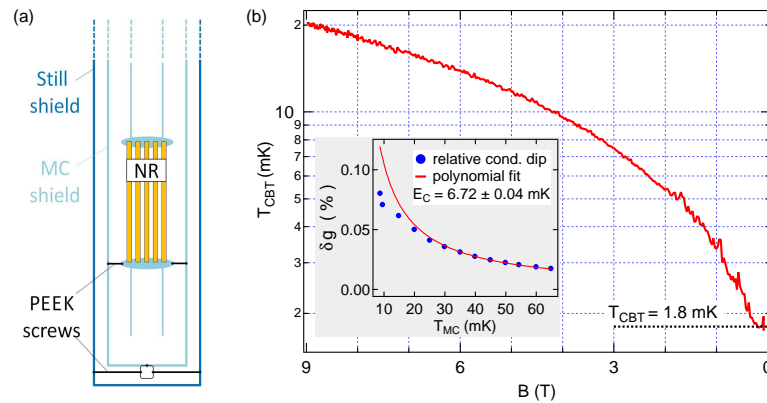


Fig. 13. Nuclear adiabatic demagnetization of a metallic Coulomb blockade thermometer. (a) Schematic showing the demagnetization stage being fixed rigidly with respect to mixing chamber shield. A second set of PEEK screws fixes the mixing chamber shield with respect to the still radiation shield. (b) The main panel shows the extracted CBT temperature as a function of magnetic field during the demagnetization process. Calibration data are shown in the inset, where blue markers correspond to measurements of the relative conductance dip  $\delta g/g_T$  and a fit to the data in the high temperature regime from 30 mK to 65 mK is shown in solid red. The resulting charging energy is  $E_C = 6.72 \pm 0.04$  mK.

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