Plug-in Repetitive Control Strategy for High-Order Wide Output Range Impedance Source Converters

Yachao Wang, *Student Member, IEEE,* Ahmed Darwish, Derrick Holliday and Barry W. Williams

***Abstract*—High-order wide-output (HOWO) impedance source converters (ISCs) have been presented for ac inverter applications that require voltage step-up ability. With intrinsic passive impedance networks as energy sources, these converters are able to achieve voltage boosting with either polarity, leading to improved dc-link voltage utilization compared with the conventional two-level converter. However, HOWO-ISCs suffer from transfer functions giving low bandwidth, a penalty of increased passive devices and right-half-plane zeros, which result in lower order distortion of the ac output power. In this paper, a modified plug-in repetitive control scheme is presented for HOWO-ISCs with accurate reference tracking (hence low distortion), fast dynamic response, and enhanced robustness. By using zero-phase-shift finite impulse response filters in both the internal model of the repetitive controller and its compensation network, the proposed method achieves zero steady-state error and an extended closed-loop bandwidth. For HOWO-ISC cases, this method outperforms conventional proportional-integral (PI) control, which has considerable steady-state error. It also eliminates the need of parallel loops for several frequencies when proportional resonant control or orthogonal transformation based PI schemes are used to remove lower order distortion. The design process and performance analysis of the proposed repetitive control strategy are based on a novel three-phase HOWO-ISC configuration with a reduced number of switches. Simulation and experimental results confirm the feasibility and effectiveness of the proposed control approach.**

***Index Terms*—Impedance source converter; dc-ac conversion; low distortion; power converter modeling; digital repetitive control, zero-phase-shift filter.**

I. INTRODUCTION

With an increasing demand for interconnecting multiple dc distributed energy resources (DERs) such as photovoltaic (PV), fuel cell and battery storage devices with the traditional energy infrastructures, a power inverter stage becomes necessary to convert the dc energy source into an ac waveform [1-3].

Since a single DER unit usually has a low output voltage, matured schemes employ many units to create a high dc-link voltage for transferring the power through a conventional central inverter, which has only voltage step-down characteristics [4, 5]. However, this method does not guarantee an optimal operation point for each DER unit [6].

To enable distributive access to low dc voltage DERs for improved energy utilization, power inverters with output voltage boosting ability are required [7]. With such motivation, a range of impedance source converter (ISC) topologies have been introduced in the recent literature [8-16], among which, the Ćuk, sepic, semi-Z-source (SZS) and semi-quasi-Z-source (SQZS) topologies all consists of two inductors and two capacitors as in their dc-dc switched mode classified by Tymerski [17]. By using an impedance network as virtual energy source, these converters achieve improved dc-link voltage utilization and terminal current profiles. However, the higher number of passive elements increases the order of converter transfer function; thus, complicating the modeling process. Specifically, high-order wide-output (HOWO) ISC topologies have non-minimum phase characteristics with extra phase lagging effect, which imposes limitation on the control design for achieving high loop-gain (low tracking error) and sufficient stability margin. Hence, a reliable control strategy with accurate reference tracking ability is demanded for ISCs, which enables them to precisely execute the system level command for power flow regulation in an interconnected energy network, such as maximum power point tracking.

In an ac system, conventional instantaneous value based proportional-integral (PI) control cannot achieve zero steady-state tracking error. Thus, PI control in the synchronous reference frame (SRF) using frequency decoupling, is employed [11] in the three-phase SQZS converter. However, to cancel the resonant peak in its transfer function, the active bandwidth needs to be reduced to a low level which weakens the dynamic performance. Also, parallel control loops for each frequency are adopted to guarantee output power quality, which leads to undesirable interaction between the different loops due to the frequency decoupled model approximation. Similarly, to save on mathematical transformations, parallel proportional resonant (PR) control loops are applied to the Ćuk type three-phase inverter in [12] to achieve sufficient harmonic rejection. Since each PR control loop targets only a specific frequency component, multiple control loops are needed; where the loops may interact. This complicates the controller and its efficiency. Nonlinear schemes such as sliding-mode control have been employed in differential mode sepic and Ćuk converters [13, 14]. The target variable usually cannot be directly controlled; so a proper sliding surface, combining several state variables, has to be selected. High-

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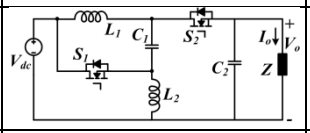
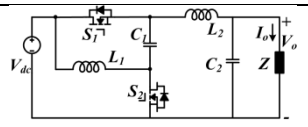
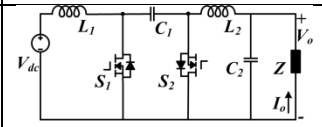
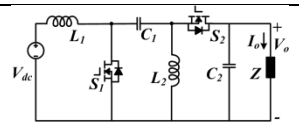
Table 1. Schematics, voltage transfer ratio, and voltage and current stresses of power switches of four ISCs.

	SZS	**SQZS**	**Ćuk**	**sepic**
Topology				
Voltage transfer ratio	$M=-\frac{2\delta-1}{\delta'}$	$M=\frac{2\delta-1}{\delta}$	$M=-\frac{\delta}{\delta'}$	$M=\frac{\delta}{\delta'}$
Voltage stress	V_{dc}/δ'	V_{dc}/δ	V_{dc}/δ'	V_{dc}/δ'
Current stress	I_o/δ'	I_o/δ	I_o/δ'	I_o/δ'
i/p and o/p current	discontinuous/ discontinuous	discontinuous/continuous	continuous/continuous	continuous/discontinuous
High frequency isolated version	No	No	Yes	Yes

pass filters are required to derive the transient signal of the control input in a time-variant ac system. Also, the sliding surface coefficient is influenced by parameter mismatches and load variations, which affects the practical performance.

Repetitive control, based on the internal model principle, is able to attenuate periodic disturbances, and has been adopted in power electronic converter applications [18-23]. In [20], plug-in repetitive control is directly adopted for the SPWM two-level inverter in an uninterruptable power supply (UPS), to ensure a low distortion, robust output voltage. In [21], parallel plug-in repetitive control with reduced data memory is used in a bridgeless rectifier topology. The modular multilevel converter (MMC) circulating current can also be eliminated by repetitive control, as in [22, 23]. However, unlike the mentioned topologies, HOWO-ISC transfer functions usually have right-half-plane (RHP) zeros, time-variant zero-pole locations, and high resonant peaks. These factors impose higher demand on the design of digital filter and compensator parameters over that for a lower order converter model.

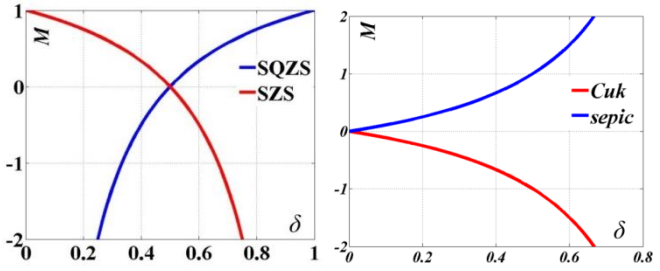
This paper presents a generic design of a digital plug-in repetitive control strategy for a family of HOWO ISCs with emphasis on the analysis of the zero-phase-shift (ZPS) filter and compensation network to achieve an extended closed loop bandwidth (improved dynamic response) and minimized reference tracking error. In the proposed strategy, an inner PI control loop and a zero-phase-shift (ZPS) finite impulse response (FIR) compensator are employed to stabilize the converter model plant with improved error convergence speed. Another ZPS low-pass FIR filter is incorporated in the internal model feedback path of the repetitive controller to attenuate the high frequency gain. In this manner, the robustness of the overall system is guaranteed. The paper is organized as follows: section II gives a brief review of representative HOWO ISC topologies with their potential configurations for multi-phase ac applications. Then the design process of the proposed control strategy is described using a selected case study with a novel three-phase SQZS converter configuration having a reduced number of switches. Simulation and experimental verification form section IV, and finally, outcomes and observations are highlighted in section V.

II. REVIEW OF HOWO-ISC TOPOLOGIES

Four representative HOWO-ISC topologies are reviewed to give an understanding of their technical merits and operational challenges, which are critical for control design. Based on inverter mode operation for a solar energy harvesting system, the characteristics of these topologies in three-phase configurations are analyzed.

A. Operation principles of the HOWO-ISC topologies

Table 1 summarizes the schematics and main operational features of four representative HOWO-ISC bidirectional topologies, including the semi-Z-source (SZS), semi-quasi-Z-source (SQZS), Ćuk and sepic converters, in which each have two inductors and two capacitors [10-14]. In Table 1, where δ is the duty cycle of S_1 (complementally, δ'=1-δ is the duty cycle of S_2) for all candidates, their voltage transfer ratio M can be derived from the inductor steady-state volt-second balance principle. In Fig. 1(a), the SZS and SQZS converters afford bi-polarity voltage output; while, as shown in Fig. 1(b), the Ćuk and sepic converters have unipolar voltage gains. The extended output voltage range of these HOWO-ISCs create increased voltage and current stresses on the power switches, which are a function of the duty cycle as in Table 1 . Also, in [12, 24], the Ćuk and sepic converters can be derived into their high frequency isolated versions by using coupled inductors.



(a) (b)

Fig. 1. Steady-state voltage transfer ratio of: (a) SZS and SQZS and (b) Ćuk and sepic converters.

The ISC topologies have been developed mainly to improve the AC side voltage magnitude (thus, dc-link voltage utilization) in the conventional half-bridge inverter [10-14]. Using the basic converter modules in Table 1, both two-leg (four-switch) and three-leg (six-switch) configurations can be employed for three-phase dc-ac applications, as in Table 2.

As with typical six-switch three-phase (SSTP) inverters, and all the topologies in Table 1, any dc components and zero sequence harmonics cancel in the output line-to-line voltages [11, 12]. The four-switch three-phase (FSTP) inverter with two buck converters and the mid-point of dc-link capacitor feeding the three-phase output [25], reduces the device and passive component count. Similarly, for the ISC topologies, the sepic converter can be configured as a FSTP inverter by using the dc source positive terminal, since it has a positive step up/down gain [13]. This scheme inherits a dc offset common mode voltage between its dc ground and AC neutral point. To suppress such a dc common mode voltage, as shown in Table 2, the SZS and SQZS converters with bipolar voltage gain are developed as FSTP inverters in this paper, among which the SQZS solution is selected as the case study for generic control design interpretation. The Ćuk converter cannot be used as an FSTP inverter due to its negative voltage gain (its output cannot be within the rail bounds).

B. Constraints of HOWO-ISCs

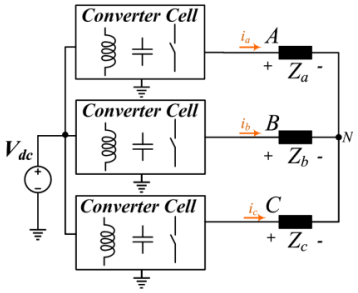
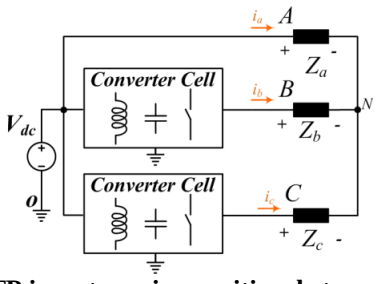
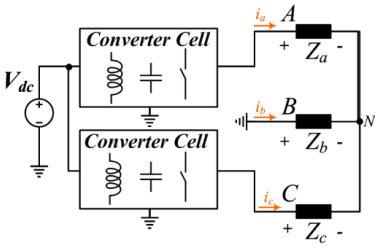
Although improved dc-link utilization can be achieved by ISC schemes, the passive components of their impedance network introduce a high number of poles and zeros (including RHP zeros) into their transfer functions. This leads to a low closed-loop bandwidth, high steady-state error, and considerable lower order harmonic distortion for the HOWO-ISCs when conventional PI control is employed.

As analyzed in [11], the SSTP SQZS converter inherits 2nd order harmonic distortion in its output voltage, which requires two parallel control loops to manage the fundamental and 2nd order harmonic simultaneously. However, in the FSTP or single-phase applications, the lower order distortion is distributed continuously in the baseband including 3rd order harmonic components; hence this parallel loop method becomes complex and inefficient.

To address this limitation, a generic repetitive control strategy applicable for all HOWO-ISC configurations is developed in the next section. Specifically, the islanded mode SQZS FSTP inverter is used as the illustrative case study due

Table 2. Configurations for three-phase inverters using basic units in Table 1.

V_m is the peak value of AC side phase voltage; ω is the fundamental angular frequency.

Three-phase inverter type	Possible topology in Table 1	Modulation Mechanism
 **SSTP inverter**	SZS, SQZS, Ćuk, sepic (with the zero sequence components being cancelled in the output line-to-line voltage) Ćuk and sepic can be high frequency transformer isolated	$V_{AN}(t) = V_m \sin \omega t$ $V_{BN}(t) = V_m \sin(\omega t - \frac{2}{3}\pi)$ $V_{CN}(t) = V_m \sin(\omega t + \frac{2}{3}\pi)$
 **FSTP inverter using positive dc terminal**	sepic (with positive voltage gain)	$V_{BO}(t) = V_{dc} - \sqrt{3}V_m \sin \omega t$ $V_{CO}(t) = V_{dc} + \sqrt{3}V_m \sin(\omega t + \frac{2}{3}\pi)$
 **FSTP inverter using dc side ground terminal**	SZS, SQZS (with bipolar voltage gain)	$V_{AB} = \sqrt{3}V_m \sin \omega t$ $V_{CB} = \sqrt{3}V_m \sin(\omega t + \frac{1}{3}\pi)$

to its control design complexities, with the following factors:

1) The islanded mode SQZS converter has a higher order transfer function than in a grid-connected mode due to the pole caused by the output capacitor and
2) Unlike the SSTP configuration with zero-sequence component cancellation, the FSTP converter requires phase independent control for distortion immunity over the full baseband range, including the zero-sequence harmonics.

III. PLUG-IN REPETITIVE CONTROLLER FOR SQZS FSTP INVERTER

A. FSTP SQZS Inverter

Based on Table 1 and Table 2, the FSTP SQZS inverter can be depicted as in Fig. 2, where two SQZS converter output terminals and the dc negative reference are connected to a three-phase balance load. In this arrangement, the total device and passive component count is reduced. If Vdc is the dc input voltage, Vm is the peak value of the desired output phase voltage, and ω is angular fundamental frequency; in order to achieve the output voltage as in (1), the modulation references for the two SQZS converters are expressed by(2).

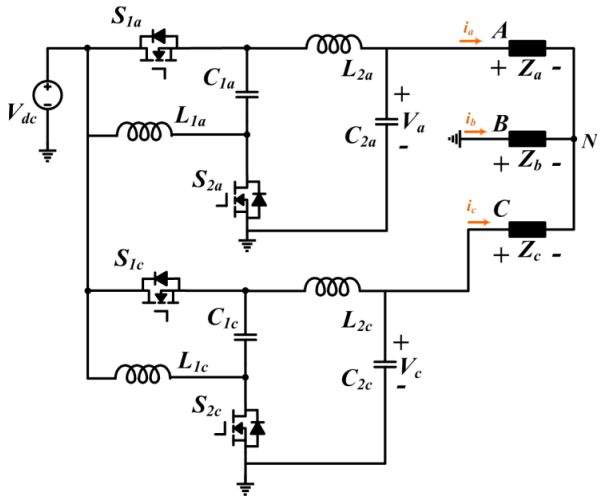


Fig. 2. SQZS-based FSTP Inverter.

From Fig. 2, the two SQZS converter output voltages in the FSTP configuration are equal to the line-to-line voltages V_{AB} and V_{CB}, respectively. With the voltage gain of the SQZS topology in Fig. 1(a), its maximum ac output voltage magnitude is V_{dc}; thus, in an FSTP arrangement, the peak phase voltage V_m is $0.5774V_{dc}$, which is higher than $½V_{dc}$ in the conventional three-phase two-level inverter (using six switches, without triplen injection). Also, compared to the sepic based FSTP inverter [13], this scheme has a pure sinusoidal ac common mode voltage (no dc component) between its ac side neutral point and the dc-link negative terminal. This eases the insulation design for an interfacing transformer in a grounded system.

$$\begin{cases} V_{AN}(t) = V_m \sin \omega t \\ V_{BN}(t) = V_m \sin(\omega t - ⅔\pi) \\ V_{CN}(t) = V_m \sin(\omega t + ⅔\pi) \end{cases} \quad (1)$$

$$\begin{cases} V_a(t) = \sqrt{3}V_m \sin(\omega t + ⅙\pi) \\ V_c(t) = \sqrt{3}V_m \sin(\omega t + ½\pi) \end{cases} \quad (2)$$

In contrast to SSTP inverters, where the zero sequence components cannot propagate onto the line-to-line voltage, their FSTP counterparts require each converter output voltage to be a purely fundamental component. This requires the control strategy of ISC based single-phase or FSTP configurations to have sufficient harmonic rejection over all baseband frequencies.

B. Modeling of the SQZS converter

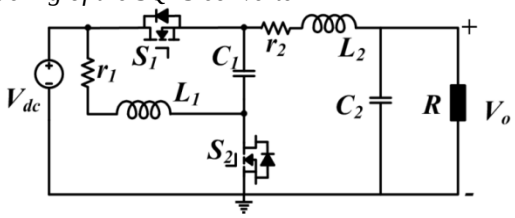


Fig. 3. SQZS converter topology.

The SQZS converter topology is redrawn in Fig. 3, where L1 (with parasitic resistance r1) and C1 form the impedance source network; L2 (with parasitic resistance r2) and C2 form the second order output filtering stage; Vdc is the input voltage and R is the load impedance in islanded mode. The two switches operate in a complementary manner with the duty cycle of S1 as the control input, which can be decoupled into a steady-state value δ plus its small perturbation Δδ in classical small signal dynamic analysis.

Then linearizing, the generic small-signal transfer function G(s) of the SQZS converter is (3), where Δvo represents the small voltage increment caused by the duty cycle perturbation Δδ around the steady-state value.

Similarly, applying this perturbing and linearization method to the steady-state equation of the voltage transfer ratio M and duty cycle δ in (4) (see Table 1), the dynamic relationship between Δm and Δδ is as in (5). Therefore, to view the voltage transfer ratio as the controller output signal, the equivalent plant of the SQZS converter for control design can be rearranged as in (6) and Fig. 4. Then the dc steady-state gain of the plant transfer function Gvm(s) (s=0) becomes independent of duty cycle variation (neglecting inductor parasitic resistance).

$$G(s) = \frac{\Delta v_o(s)}{\Delta\delta(s)} = \frac{V_{dc}}{\delta} \frac{A_0 + A_1 s + A_2 s^2}{B_0 + B_1 s + B_2 s^2 + B_3 s^3 + B_4 s^4}$$

$$A_0 = \delta R - M(\delta - 1) r_1$$

$$A_1 = C_1 R r_1 - M(\delta - 1) L_1$$

$$A_2 = C_1 L_1 R$$

$$B_0 = \delta^2 (R + r_1 + r_2) - (2\delta - 1) r_1 \quad (3)$$

$$B_1 = \delta^2 (C_2 R r_2 + L_2) + (\delta - 1)^2 (C_2 R r_1 + L_1) + C_1 r_1 (R + r_2)$$

$$B_2 = \delta^2 C_2 R (L_1 + L_2) - (2\delta - 1) C_2 L_1 R + C_1 L_1 (R + r_2)$$

$$+ C_1 L_2 r_1 + C_1 C_2 R r_1 r_2$$

$$B_3 = C_1 C_2 R L_1 r_2 + C_1 C_2 R L_2 r_1 + C_1 L_1 L_2 \qquad B_4 = C_1 C_2 L_1 L_2 R$$

$$\delta = \frac{1}{2 - M} \quad (4)$$

$$K(s) = \frac{\Delta\delta(s)}{\Delta m(s)} = \delta^2 \quad (5)$$

$$G_{vm}(s) = \frac{\Delta v_o(s)}{\Delta m(s)} = K(s) \cdot G(s) = \delta^2 G(s) \quad (6)$$

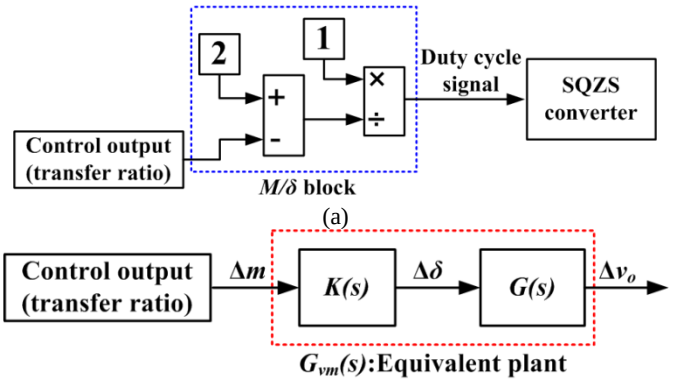


Fig. 4. Relationship between voltage transfer ratio and duty cycle in SQZS converter: (a) the signal transformation and (b) small-signal equivalent plant for controller design.

In quasi-steady-state analysis of the SQZS inverter, the voltage transfer ratio M should be modulated as a pure sinusoidal waveform as in (7), where A_m is the ratio of the converter ac side voltage magnitude (line-to-line voltage for the FSTP inverter) over the dc-link voltage. Then, from (4), the duty cycle can be estimated by (8) when ignoring the internal inertia of the SQZS converter.

$$M(t) = A_m \sin \omega t \tag{7}$$

$$\delta(t) = \frac{1}{2 - M(t)} = \frac{1}{2 - A_m \sin \omega t} \tag{8}$$

The passive element parameters of the SQZS converter are usually determined by the voltage and current peak ripple constraints, as discussed in [10, 12, 13]. With these principles, the FSTP SQZS inverter specification for this study is shown in Table 3.

In Table 3, with the shown dc-link and ac side line-to-line voltages, Am = 0.8; hence, the duty cycle of each SQZS converter module varies approximately between 0.36 and 0.83, based on (8). Then, by substituting the parameters in Table 3 and varying the steady-state duty cycle δ, a family of Bode plots and pole-zero plots for the transfer function Gvm(s) result as in Fig. 5.

From Fig. 5(b), when the duty cycle is less than ½, RHP zeros emerge, leading to non-minimal phase system performance with significant phase delay, as shown by the phase-frequency Bode plots in Fig. 5(a). Thus, a phase-leading compensation network is required to increase the phase margin and improve the dynamic response [26]. Also, in the amplitude-frequency Bode plots of Fig. 5(a), the resonant peak increases with increasing duty cycle.

Table 3. Rated Values for the FSTP SQZS Inverter.

Power rating	P	2	kW
Per phase load	R	2.5	Ω
Input dc voltage	V_{dc}	125	V
AC line-to-line peak voltage	$\sqrt{3}V_m$	100	V
Inductor	L_1 and L_2	0.5	mH
Capacitor	C_1 and C_2	10	μF
Switching frequency (sampling frequency)	f_s	30	kHz
Fundamental frequency	f_o	50	Hz

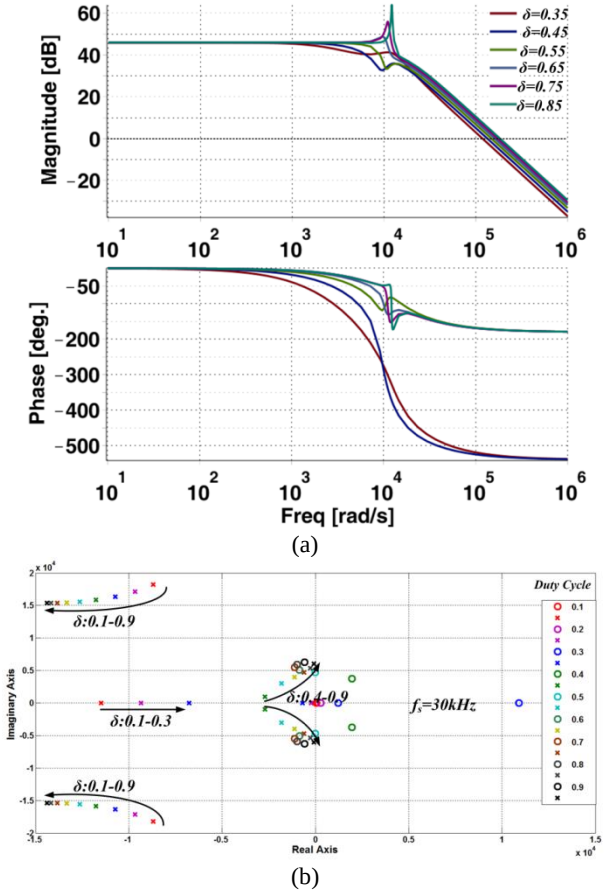


Fig. 5. SQZS inverter characteristics with duty cycle variation: (a) Bode plots of $G_{vm}(s)$ and (b) pole-zero map.

This time-varying performance with duty cycle is in-line with the topologically asymmetrical operation of the SQZS inverter (also other ISCs) for generating bipolar voltage. For example, in the SQZS inverter, the positive voltage level is generated directly by the dc-link; while the negative level is derived from the energy stored in the impedance network.

From (6), by using the transformation block K(s), the dc steady-state gain of $G_{vm}(s)$ is independent of δ variation compared to (3); however, the gain of $G_{vm}(s)$ in the low frequency range ($s \neq 0$) is of concerned for a dc-ac inverter system and changes with duty cycle variation. Consequently, the SQZS converter (and other ISCs) has a time-variant gain effect on the modulating signal along a fundamental period, which means that lower order harmonic distortion will appear if the modulating signal is purely the fundamental component. But the real SQZS duty cycle trajectory should deviate from (8) if a pure fundament output voltage is generated.

Thus the SQZS control strategy (and other HOWO-ICSs) should have sufficient harmonic rejection ability to ensure power quality. In this paper, repetitive control with periodic disturbance attenuation is adopted to address this problem. Compared to its application in the two-level converter (such as in UPS [20]), the challenge of using this method in HOWO-ISC is mainly the design of the digital ZPS filter and compensation network for a time-variant plant, which is able to stabilize the converter and increase the effective closed-loop bandwidth. The detailed analysis and design procedure are based on the FSTP SQZS inverter.

C. Digital plug-in repetitive controller for the FSTP SQZS inverter

1) Overall control strategy for the SQZS inverter

The FSTP inverter requires independent control of its two converter modules to ensure voltage reference tracking as in (2), but only one inverter needs to be considered in the control design process. Fig. 6 illustrates the proposed digital plug-in repetitive control strategy for the SQZS inverter with V_d representing all external disturbances. The proposed control scheme employs a repetitive controller outer layer and a PI controller in the inner layer.

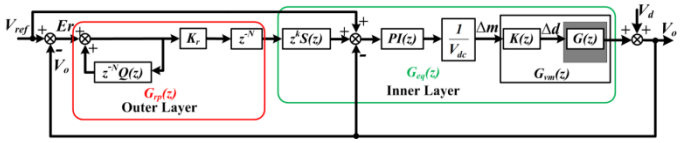


Fig. 6. Proposed Plug-in Repetitive Control Scheme.

Theoretically, an ideal plant for repetitive control should have an amplitude gain close to unity (0dB) in the low frequency range (before the cut-off frequency) and then rapidly fall off, monotonically [23]. Therefore, the inner PI controller in Fig. 6 is adopted to stabilize the converter transfer function $G_{vm}(z)$. However, PI control is not able to achieve zero steady-state error for the ac signal; thus, the fundamental error and lower order harmonic distortion (baseband frequency range) cannot be eliminated. Also, since the converter model in the negative half cycle has RHP zeros as in Fig. 5(b), its dynamic response with only PI control is slow. To provide sufficient closed-loop bandwidth as well as harmonic rejection capability, a FIR ZPS compensator $S(z)$ and an outer layer repetitive controller with a FIR ZPS low-pass filter $Q(z)$, are employed in Fig. 6 to provide fast and accurate voltage reference tracking [20].

2) Compensation network for modifying the converter plant

In Fig. 6, the inner layer compensates the converter plant (close to the ideal case), for the outer layer repetitive controller.

By the forward difference mapping method from the s-domain to the z-domain, the discrete transfer function of the normal PI controller can be transformed into (9), where T_s is the sampling (switching) period. Then, if $G_{vm}(z)$ represents the z-plane transformed version (forward difference mapping) of the transfer function $G_{vm}(s)$ in (6), its closed-loop z-domain transfer function $G_p(z)$ with PI control is expressed by (10). To suppress the resonant peak of $G_{vm}(z)$ in Fig. 5(a) over the full duty cycle range, the PI control parameters should be sufficiently small due to the RHP zeros when the duty cycle falls below ½; hence the dynamic response of the inner closed-loop is slow. For the specification in Table 3, the PI parameters are selected as P=0.4, I=600, which sets the cross-over frequency of the open loop transfer function $G_{vm}(z)PI(z)$ to about 200Hz, ensuring sufficient stability margin to adapt to a wide load range variation and other disturbances. Then, the amplitude Bode plot of the inner closed-loop system $G_p(z)$, with dc-link voltage normalization, drawn in Fig. 7, still has high resonant peaks and is not a qualified plant for repetitive control.

$$PI(z) = P + I \times T_s \frac{1}{z-1} \tag{9}$$

$$G_p(z) = \frac{G_{vm}(z) \cdot PI(z)/V_{dc}}{1 + G_{vm}(z) \cdot PI(z)/V_{dc}} \tag{10}$$

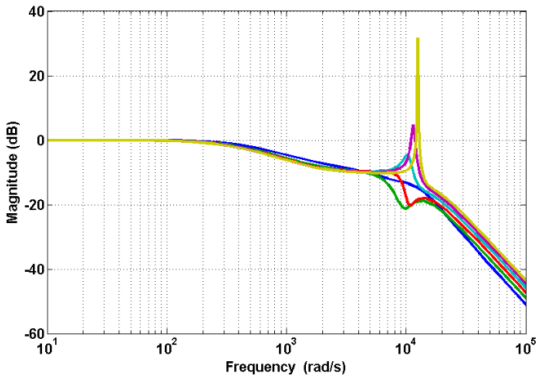


Fig. 7. Magnitude Bode plot of $G_p(z)$ with only PI control.

In order to eliminate the high resonant peaks of $G_p(z)$ for large duty cycles, an additional compensator is required. Considering the low phase margin caused by the RHP zeros and the floating position of the resonance peak due to its time-variant performance, the traditional second-order low-pass filter with additional phase delay and a fixed resonance frequency ZPS notch filter are not applicable to the SQZS inverter [20]. Instead, to mitigate a set of resonant peaks for a wide duty cycle range in the SQZS inverter without deteriorating its phase margin (dynamic performance), a m order FIR ZPS compensator $S(z)$ as in (11) with no phase lag, is employed. For the design case of Table 3, the resonance frequencies vary approximately between 1.5kHz and 2kHz as in Fig. 5(a); thus, a 17 order FIR ZPS filter $S(z)$ with a cut-off frequency of 1.5kHz is designed in MATLAB to suppress the resonance peak to below 0dB. The $S(z)$ parameters for this case are listed in Table 4.

$$S(z) = \sum_{i=0}^{m} a_i (z^i + z^{-i}) \tag{11}$$

Table 4. Coefficients a_i for the FIR ZPS compensator $S(z)$ in (11), m=17.

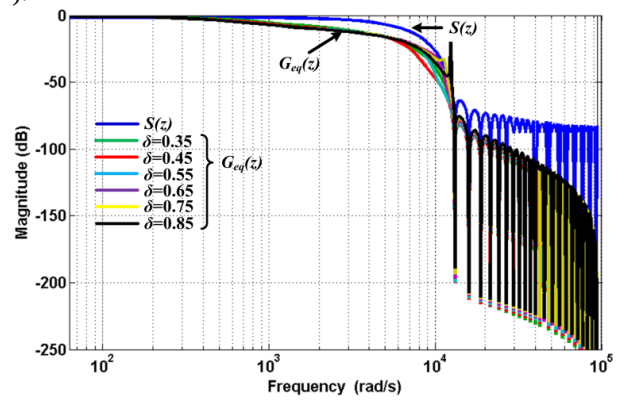
a_0=0.02442;	a_1=0.00104;	a_2=0.00196;	a_3=0.00329;	
a_4=0.00508;	a_5=0.00736;	a_6=0.01015;	a_7=0.01343;	
a_8=0.01714;	a_9=0.02120;	a_{10}=0.02548;	a_{11}=0.02985;	
a_{12}=0.03413;	a_{13}=0.03816;	a_{14}=0.04174;	a_{15}=0.04472;	
a_{16}=0.04697;	a_{17}=0.04836.			

Further, to achieve sufficient phase margin and a fast dynamic response, a k step leading unit z^k is inserted to compensate the phase-lag, particularly for the RHP zeros. Due to the data storage of repetitive control, this leading unit will not result in a non-causal system and allows a faster PI controller to improve the dynamic performance. Then, the SQZS inverter repetitive control plant can be expressed by (12), in which stability is guaranteed and the transient performance is enhanced. Specifically, k is selected to be 9 in this design case.

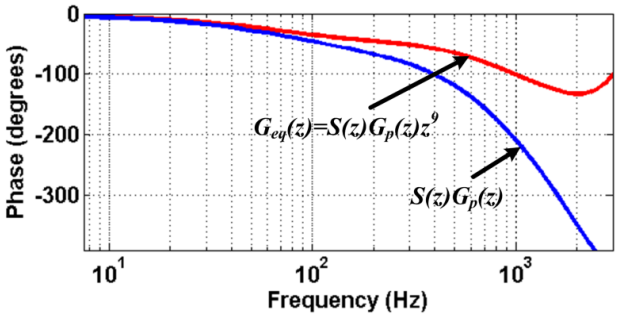
$$G_{eq}(z) = z^k S(z) G_p(z) \tag{12}$$

With all parameters now known in this case study, the amplitude Bode plots of $G_{eq}(z)$ change with duty cycle δ can be displayed in Fig. 8(a), where all the resonant peaks have been suppressed below 0dB. Also, the phase responses of the original plant $G_{vm}(s)$ in Fig. 5(a) reveal that the most severe phase lag occurs at the smallest duty cycle, which is approximately 0.35 in this case. The phase responses of $G_{eq}(z)$

with k=9 and $S(z)G_p(z)$ without phase-leading compensation are both displayed in Fig. 8(b), where the leading unit z^k is able to significantly increase the phase margin to realize an improved closed-loop bandwidth. A compensated equivalent plant suitable for repetitive control can now be achieved, as in (12).



(a)



(b)

Fig. 8. Compensation effects: (a) magnitude response of $G_{eq}(z)$ and $S(z)$ and (b) phase compensation at δ=0.35.

3) Internal model design for plug-in repetitive control

The repetitive controller with a fast feed-forward path is shown in the outer layer of Fig. 6. The discrete implementation of the internal model of repetitive control is expressed by (13), where K_r is the gain coefficient to adjust the tracking error convergence rate and Q(z) is a low-pass filter to guarantee stability at high frequencies [27]. By periodic integration, any repeatable disturbances can be accumulated in the output; thus high gains for these periodic signals can be achieved in (13), where N is number of sampling points within one fundamental period.

$$G_{rp}(z)=\frac{z^{-N}K_r}{1-Q(z)z^{-N}} \tag{13}$$

Based on Fig. 6 and (13), for the modified plant $G_{eq}(z)$, the voltage tracking error Er(z) is expressed in (14). To ensure repetitive controller stability, the condition in (15) should be satisfied according to the small gain theorem [28]. This reveals that the magnitude of $\left|H(e^{j\omega T_s})\right|$ should always be less than unity when ω changes from zero to πf_s (Nyquist frequency).

$$\begin{aligned} Er(z)=&\frac{(1-G_p(z))(z^N-Q(z))}{z^N-\left[Q(z)-K_rG_{eq}(z)\right]}V_{ref}(z)\\ &-\frac{(1-G_p(z))(z^N-Q(z))}{z^N-\left[Q(z)-K_rG_{eq}(z)\right]}V_d(z)\end{aligned} \tag{14}$$

$$\begin{aligned}\left|H(e^{j\omega T_s})\right|&=\left|Q(e^{j\omega T_s})-K_rG_{eq}(e^{j\omega T_s})\right|\\&=\left|Q(e^{j\omega T_s})-e^{j\omega kT_s}K_rS(e^{j\omega T_s})G_p(e^{j\omega T_s})\right|<1\end{aligned} \tag{15}$$

where $\omega\in[0,\frac{\pi}{T_s}],T_s=\frac{1}{f_s}$

In practice, to ensure sufficient stability margin, Q(z) can be selected as a close-to-unity constant (such as 0.95) or a low-pass filter, which is able to ensure sufficiently high magnitude gain in $G_{rp}(z)$ within the baseband. Thus, provided the reference voltage V_{ref} and disturbance V_d are both purely repetitive as in (16), by viewing $Q(z)$ as 1 in the low frequency range and substituting it into (14), the tracking error Er(z) can be expressed by (17). This means that after each fundamental period, the magnitude of error Er(z) can be attenuated to H(z) times its previous value. Therefore, to ensure stability and increase the convergence rate, H(z) must fall within the unity circle and should be as small as possible.

$$\begin{cases}z^{-N}\cdot V_d(z)=V_d(z)\\ z^{-N}\cdot V_{ref}(z)=V_{ref}(z)\end{cases} \tag{16}$$

$$z^N\cdot Er(z)=H(z)\cdot Er(z) \tag{17}$$

In the frequency domain, (14) can be rewritten as (18) with $T(e^{j\omega T_s})$ being expressed by (19). By decreasing the magnitude of the term $T(e^{j\omega T_s})$, the harmonic rejection ability can be enhanced and the steady-state error of the repetitive controller is minimized. Specifically, zero steady-state error can be achieved at frequency ω, where $Q(e^{j\omega T_s})=1$.

$$\begin{aligned}\left|Er(e^{j\omega T_s})\right|=&\left|T(e^{j\omega T_s})\right|.\left|\left(1-G_p(e^{j\omega T_s})\right)V_{ref}(e^{j\omega T_s})\right|\\&-\left|T(e^{j\omega T_s})\right|.\left|\left(1-G_p(e^{j\omega T_s})\right)V_d(e^{j\omega T_s})\right|\end{aligned} \tag{18}$$

$$T(e^{j\omega T_s})=\frac{1-Q(e^{j\omega T_s})}{1-H(e^{j\omega T_s})} \tag{19}$$

For better convergence performance, Q(z) should not introduce any additional phase delay into the control loop. Therefore, for low distortion in the SQZS converter output voltage, a FIR structure ZPS low-pass filter is designed for Q(z) with a 3kHz cut-off frequency, for the case in Table 3. The expression of Q(z) is indicated in (20) with the coefficients calculated in MATLAB, listed in Table 5.

$$Q(z)=\sum_{i=0}^{n}b_i(z^i+z^{-i}) \tag{20}$$

Table 5. Coefficients b_i for the FIR ZPS low-pass filter $Q(z)$ in (20), n=6.

b_0=0.59961; b_1=0.21864; b_2=-0.01795; b_3=0.0063; b_4=-0.00624; b_5=0.0008; b_6=0.00007.

To highlight the effect of Q(z), the stability constraint of (15) is plotted in Fig. 9, where the vector $H(e^{j\omega T_s})$ should not exceed the unity circle. Due to the design demand, in low frequency range, $Q(e^{j\omega T_s})$ should be close to 1 as interpreted by the solid line in Fig. 9. Also, with the compensated converter plant of (12), $K_rG_{eq}(e^{j\omega T_s})$ maintains an approximate unity magnitude gain (when K_r=1) and small phase delay within the baseband frequency range. These imply that $\left|H(e^{j\omega T_s})\right|$ is sufficiently small and the repetitive controller is able to achieve steady-state error mitigation and fast convergence at its effective bandwidth. For the specific

case in Table 3, the designed gain of the FIR ZPS filter $Q(e^{j\omega T_s})$ in (20) and Table 5 can be maintained as 0.98 up to 2 kHz, which is satisfactory to ensure sufficient lower order harmonic rejection. With increasing frequency, the phase delay of $G_{eq}(e^{j\omega T_s})$ increases, while its magnitude decreases. This makes the $K_r G_{eq}(e^{j\omega T_s})$ vector rotate closer to the imaginary axis, as shown by the dashed line in Fig. 9. Due to the high frequency attenuation effect of $Q(z)$, the unity circle around the terminal of vector $Q(z)$ moves left (dashed line) with an increase of frequency, which helps maintain the stability margin by ensuring sufficient distance from $H(e^{j\omega T_s})$ to the new circle (dashed line). For the spectrum range above the cut-off frequency, the magnitude of $G_{eq}(z)$ falls off rapidly, as in Fig. 8.

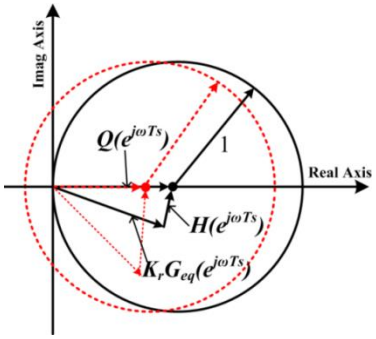


Fig. 9. Operational stability explanation.

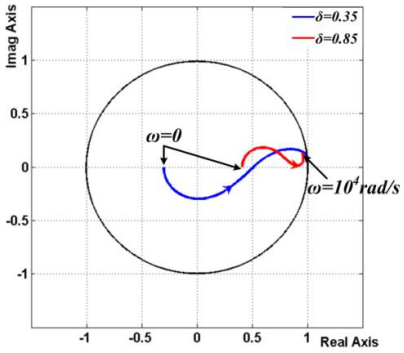


Fig. 10. Vector $H(e^{j\omega T_s})$ locus.

The proportional gain of the repetitive controller K_r is usually a real number smaller than 1. A larger K_r produces faster error convergence but less stability margin, as it will determine the length of $K_r G_{eq}(e^{j\omega T_s})$ (thus, also $H(e^{j\omega T_s})$) in Fig. 9. The trajectory of $H(e^{j\omega T_s})$ in the complex plane is drawn in Fig. 10 for K_r=1 at the operational points of minimum and maximum duty cycle δ. The stability margin is guaranteed with the selected control parameters for the SQZS inverter design case in Table 3.

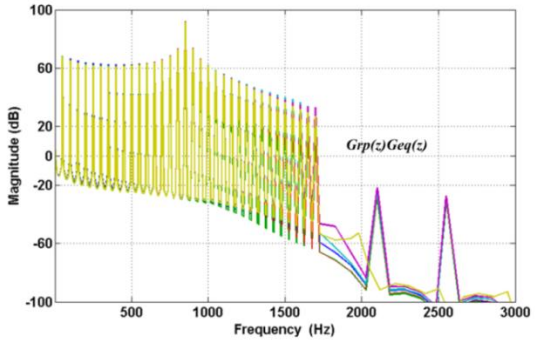


Fig. 11. Open loop gain $G_{rp}(z)G_{eq}(z)$ amplitude response.

With all the design parameters known, the discrete open loop transfer function of the SQZS inverter with the proposed plug-in repetitive control strategy can be expressed as $G_{rp}(e^{j\omega T_s})G_{eq}(e^{j\omega T_s})$, and its amplitude gains under the full duty cycle variation range are shown in Fig. 11 (K_r= 1). The repetitive controller is able to attenuate the lower order distortion in the baseband by increasing its open loop gain at integer times of the fundamental frequency. Due to the use of FIR ZPS compensator $S(z)$ and low-pass filter $Q(z)$, high frequency disturbance can be suppressed significantly. The effective bandwidth is extended compared to conventional methods, as shown in Fig. 11.

IV. SIMULATION AND EXPERIMENT VERIFICATION

To verify the effectiveness of the proposed control scheme, simulation and experimentation on the FSTP SQZS inverter have been performed.

A. Simulation Tests

The simulation model of the topology in Fig. 2 is based on the specification in Table 3; thus, the desired output line-to-line voltage peak value is 100V (57.7V phase voltage) in the FSTP SQZS inverter. Initially, it operates with only the inner PI controller of Fig. 6, with parameters P=0.4 and I=600, which is achieved by considering the relative stability indicators.

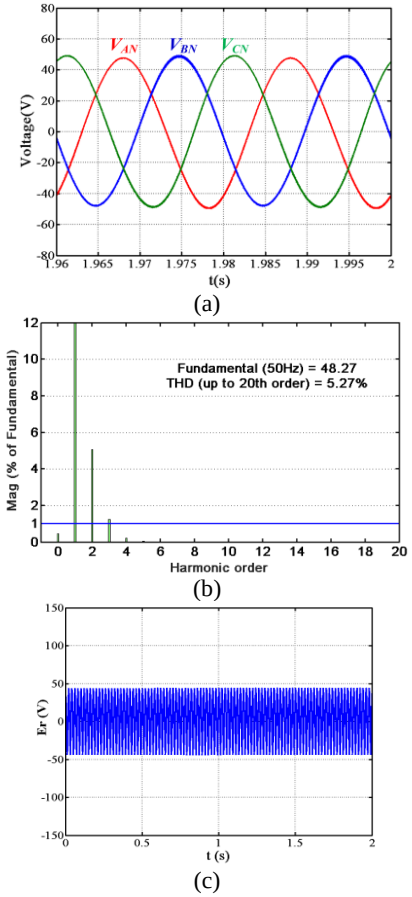


Fig. 12. FSTP-SQZS inverter with PI controller: (a) output phase voltage waveforms, (b) fundamental magnitude and low order harmonic distribution for phase A output voltage; and (c) steady state error caused by PI control.

The results in Fig. 12 show considerable fundamental component tracking error and low order harmonic distortion

(mainly 2nd order); and the calculated baseband (up to 20th order) total harmonic distortion (THD) is 5.3%. This is consistent with the theoretical analysis of the PI controlled SQZS converter with low bandwidth and non-uniform gains at different operating points.

To eliminate the low order harmonic distortion and improve the reference tracking accuracy, repetitive control is employed, initially without compensator $S(z)$ but the PI parameters remain the same. The repetitive controller has a magnifying effect on the magnitude gain, including the resonant peaks. Due to the absence of $S(z)$, the proportional gain of the internal model K_r has to be decreased to guarantee stability. In this case, K_r is chosen to be 0.01. From Fig. 13(b), increased fundamental voltage magnitude and reduced 2nd order harmonic distortion can be achieved. However, in Fig. 13(c), the error convergence rate is slow due to small K_r.

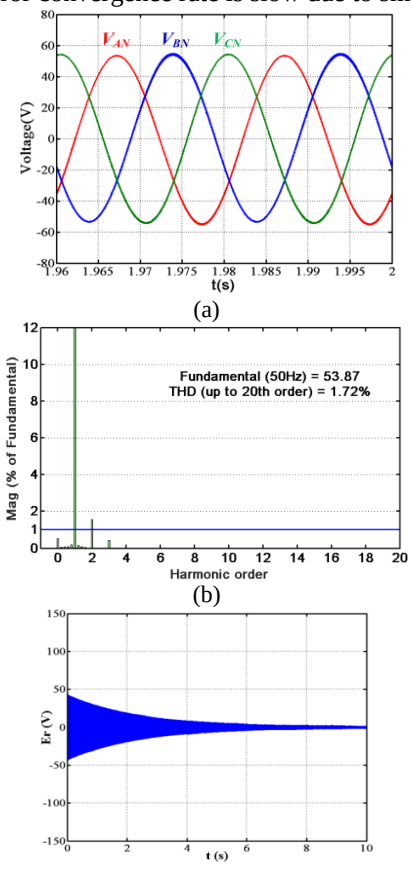


Fig. 13. FSTP-SQZS inverter using repetitive control without compensator $S(z)$ and K_r=0.01: (a) output phase voltage waveforms, (b) fundamental magnitude and low order harmonic distribution for phase A output voltage; and (c) error convergence process.

By incorporating compensator $S(z)$ into the control loop, the proportional gain K_r of the repetitive controller can be increased. With $S(z)$ based on Table 4 and K_r=0.8, Fig. 14(b) shows that the fundamental voltage is able to precisely track the reference and low order harmonic components can be eliminated; hence, almost zero steady-state-error is obtained; and the error convergence rate significantly improves with a settling time of less than 0.2s, as illustrated in Fig. 14(c).

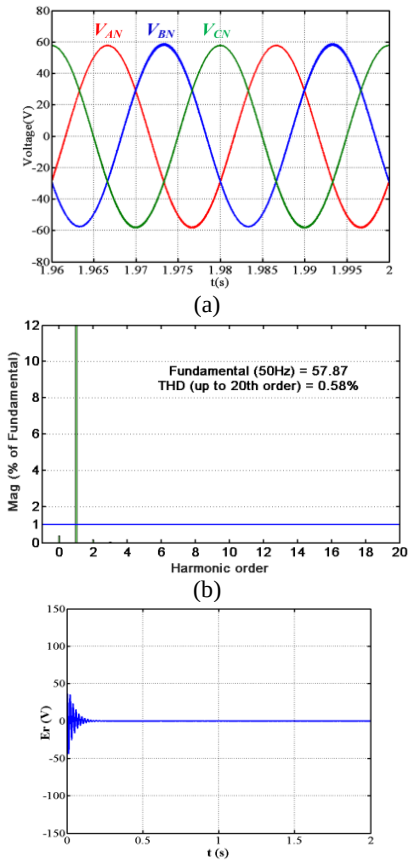


Fig. 14. FSTP-SQZS inverter using the proposed repetitive control scheme including $S(z)$ and K_r=0.8: (a) output phase voltage waveforms; (b) fundamental magnitude and low order harmonic distribution for phase A output voltage; and (c) error convergence process.

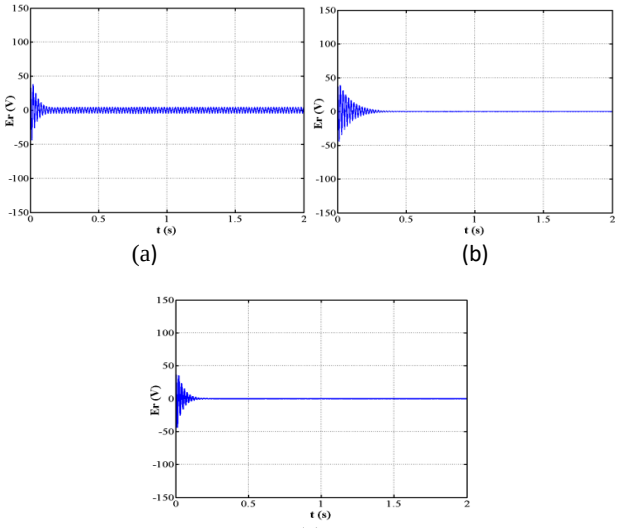


Fig. 15. Error convergence comparison for the plug-in repetitive controller with different parameters: (a) $Q(z)$=0.95, K_r=0.8, (b) Q(z) is low-pass filter, K_r=0.4, and (c) $Q(z)$ is low-pass filter, K_r=0.8.

The impact of K_r and $Q(z)$ is analysed with the error convergence process in Fig. 15, where it is deduced that a higher K_r shortens the settling time, but its maximum value is restricted by the stability constraint shown in Fig. 9. When $Q(z)$ is 0.95, zero steady state error cannot be achieved due to its attenuation effects on the low frequency loop gains, which

finally degrades the ability for lower order harmonic rejection. Comparison between Fig. 15(a) and (c) reveals that $Q(z)$ significantly influences the steady-state error.

B. Experimental Results

A MOSFET based SQZS FSTP inverter is used for practical operational validation purposes. Due to the high voltage stress on the power switches in the SQZS converter (and other ISCs), the dc-link voltage and ac line-to-line peak voltage are scaled down to 40V and 32V (power rating is 200W) respectively, while the other parameters are maintained as in Table 3. With this arrangement, the original pole-zero positions of the SQZS converter design case are unchanged. Since the control design diagram in Fig. 6 has an $1/V_{dc}$ stage to normalize the converter model to unity (with 0dB open-loop gain in baseband), the previously selected parameters for the PI controller, $S(z)$, phase-leading compensator, and the internal model ($Q(z)$ and K_r), remain valid (provided the $1/V_{dc}$ stage is included).

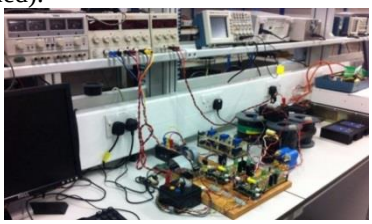


Fig. 16. Photograph of the experimental rig.

The control strategy of the FSTP SQZS inverter is realized on a Texas Instrument TMS320F280335 DSP platform with a sampling frequency equal to switching frequency (30 kHz). The power switches are RFP4668PBF MOSFETs and the overall experiment setup is shown in Fig. 16.

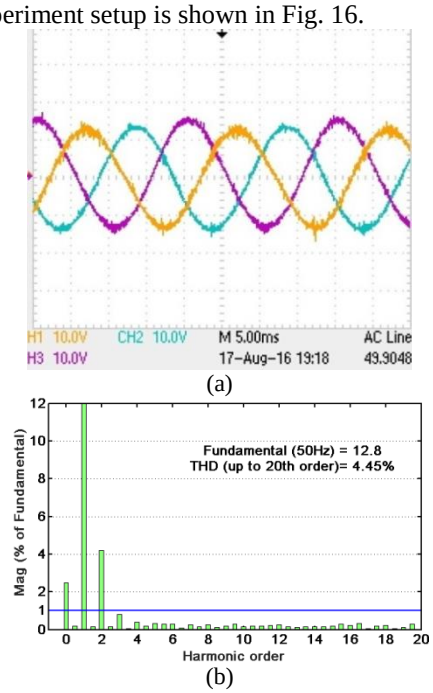


Fig. 17. Experimental results with conventional PI control: (a) three-phase output voltage and (b) fundamental magnitude and low order harmonic distribution for phase A output voltage.

Initially, conventional PI control for the FSTP SQZS inverter is tested with the results in Fig. 17, where the achieved fundamental magnitude is much lower than the desired reference. Also, due to the inadequate bandwidth, the voltage waveform deviates from the pure sinusoid by considerable 2nd order harmonics.

Next, the three-phase output voltage and FFT analysis with the proposed repetitive control and 2.5Ω resistive load are given in Fig. 18, where all low harmonic components are less than 1% of the fundamental except a residual dc component due to the transducer zero-point 1% calibration error.

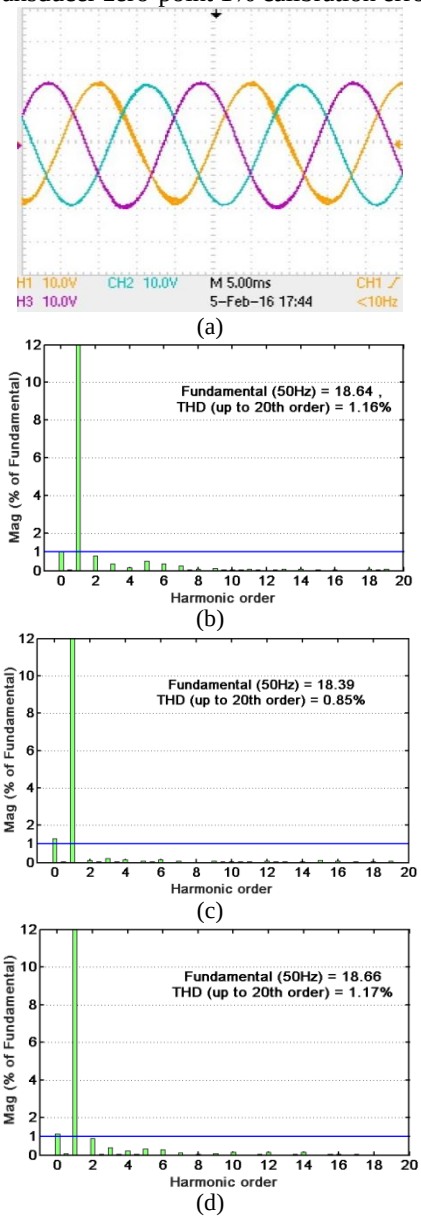


Fig. 18. Experiment results using proposed repetitive control strategy for FSTP-SQZS inverter: (a) three-phase output voltages; and fundamental magnitude and low order harmonic distribution for the output voltages of (b) phase A; (c) phase B; and (d) phase C.

Furthermore, Fig. 19 shows the output voltage and current waveforms under different load conditions. In Fig. 19 (a), the single-phase output voltage with 2.5Ω resistive load is displayed; and Fig. 19 (b) shows the line-to-line voltage and line current with a 5Ω plus 10mH inductive series load. For an unbalanced load, the three-phase line-to-line voltage in Fig. 19 (c) is able to maintain balanced; while the load current becomes unbalanced as in Fig. 19 (d). To examine the dynamic performance of using the proposed repetitive controller, Fig. 19 (e) demonstrates the transient performance

of the SQZS inverter output voltage when the load is step changed from 6Ω to 3Ω. The converter output voltage quickly tracks the reference.

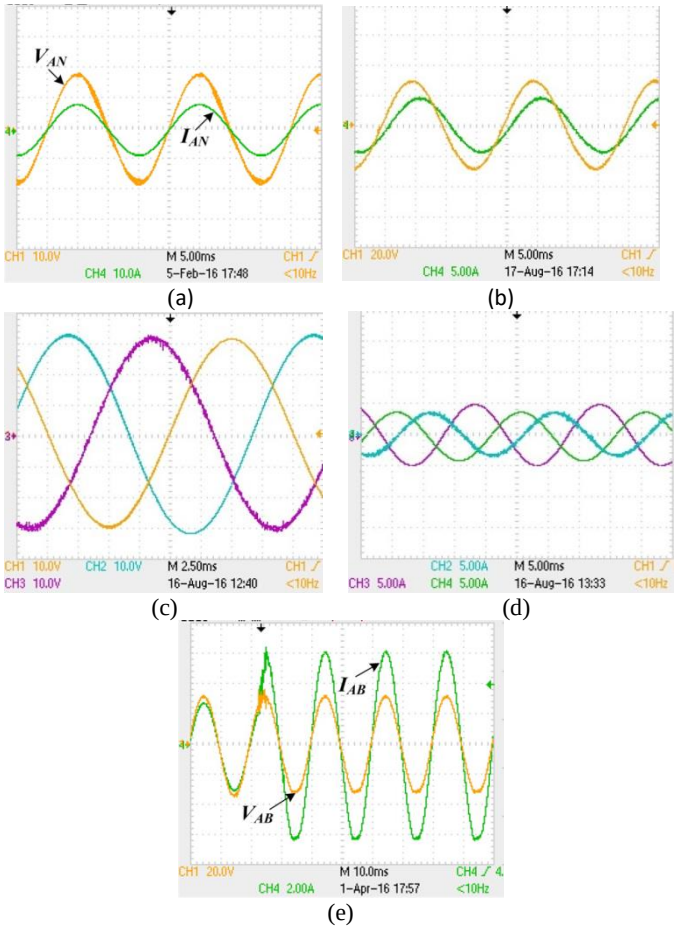


Fig. 19. FSTP-SQZS inverter with different load conditions: (a) phase voltage and current with 2.5Ω load; (b) line-to-line voltage and converter output current with 5Ω+10mH load; (c) balanced three-phase line-to-line voltage with unbalanced load (5.6Ω for phase A and C, 3Ω for phase B); (d) three-phase unbalanced current; and (e) voltage transient performance during load step change (6Ω to 3Ω).

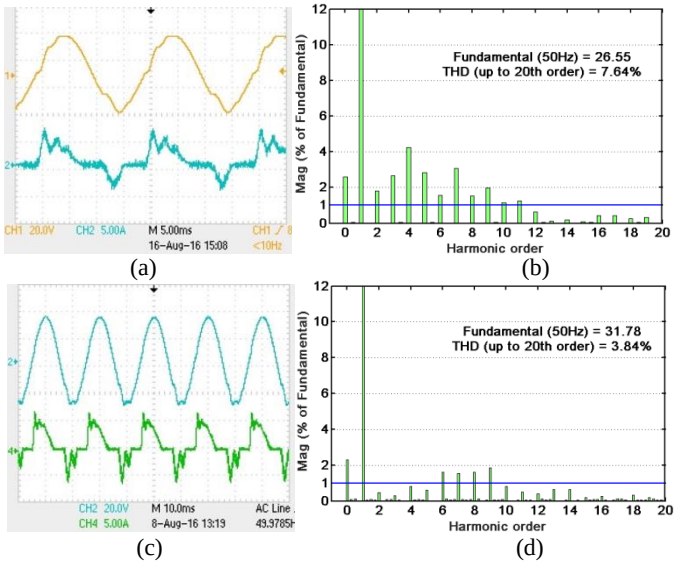


Fig. 20. Experiment results with a nonlinear load (diode rectifier with 300μF capacitor and 10Ω resistor): for PI control (a) voltage and current waveforms; and (b) fundamental magnitude and low order harmonic distribution; and with repetitive control (c) voltage and current waveforms; and (d) fundamental magnitude and low order harmonic distribution.

These experimental results imply that both the steady-state and dynamic performance of the SQZS inverter can be improved by using the proposed plug-in repetitive control scheme with a ZPS compensation network.

Fig. 20(a) and (b) give the output voltage and current waveform of the SQZS inverter using PI control under a typical rectifier nonlinear load. Due to limited bandwidth and poor harmonic rejection ability, the output voltage deviates from its reference with inadequate fundamental component magnitude and significant low order harmonics. But the results in Fig. 20(c) and (d) with the proposed repetitive control strategy, maintain the desired fundamental magnitude and suppress the dominant low order harmonics.

V. Conclusions

A generic digital plug-in repetitive control strategy has been proposed for a series of high-order wide-output range impedance source converters (HOWO-ISCs). Specifically, a four-switch three-phase (FSTP) semi-quasi-Z-source (SQZS) islanded mode inverter was adopted as a representative case study. The time-variant characteristics for HOWO-ISCs with non-uniform gains in their transfer function over a fundamental period were analyzed, which leads to inherent lower order harmonic distortion in the output voltage during open-loop operation.

The proposed repetitive control strategy eliminates the reference tracking error for the HOWO-ISCs using a single loop, which outperforms conventional proportional-integral (PI) and proportional-resonant (PR) methods with multiple parallel loops for suppressing all low order harmonics. In the proposed scheme, with the designed finite impulse response (FIR) zero-phase-shift (ZPS) compensator and phase-leading unit, an extended bandwidth is obtained by overcoming the initial phase-lag caused by right-half-plane (RHP) zeros; furthermore, the internal model of the repetitive control unit offers increased loop gain with a wide frequency range. Therefore, accurate reference tracking, fast convergence rate, and robust stability can be achieved. A design procedure of the proposed controller has been presented for a FSTP-SQZS islanded inverter, which has been validated by simulation and experimental results.

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