
# Thematic Group 2

## *Nanoelectronics and Nanotechnologies*

Report for Public Consultation

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# TG2 Nanoelectronics and Nanotechnologies

## 1. Introduction and motivation

Information and communication technologies have benefited from the downsizing of components since the sixties. This trend is often represented by the well-known Moore's law, which describes the exponential downscaling of transistors with a doubling of the number of transistors per unit area every 18 months. The present semiconductor technology entered recently the nano-scale world, since the microelectronics industry is already producing transistors with critical dimensions below 100 nm. Nanoelectronics and nanotechnologies are expected to have a strong impact on future economic growth. Areas benefiting from these developments will include materials, medicine, and information technology.

It is expected, however, that the ever-increasing computing performance and storage capacities achievable with existing technologies will eventually reach a plateau in 10-15 years time with storage capacities of Terabytes and peak performance of TeraFLOPS for a standard chip. On the other hand the power consumption of high-performance chips is estimated to rise to intolerably-high values. These predictions have highlighted the need to explore technological alternatives to extend IT capabilities beyond the limitations of current CMOS technology and underpin the current trend towards diversification and increased complexity of technologies hybridized onto CMOS platforms.

## 2. Vision and Grand Challenges

To differentiate future research directions, it is useful to draw a distinction between the *More of Moore, More than Moore* and *Beyond Moore* technology drivers. The *More of Moore* approach is focused on delivering the ITRS roadmap for late CMOS and post-CMOS systems and in particular, how to continue Moore's law beyond the predicted 22 nm node in 2011. The *More than Moore* approach is focused on delivering greater functionality through heterogeneous integration of nanosystems with electronic, optical, magnetic, chemical, biological, mechanical and other functions. Research themes, which extend *Beyond Moore* in terms of their potential to deliver disruptive technologies, include new paradigms such as intra-molecular computing and engineered coherent solid-state quantum systems.

Future disruptive technologies and breakthroughs may come from progress in a range of rapidly-developing areas, including

- Information carriers: electrons, spins, photons, phonons, atoms, molecules, mechanical state, material phase and quantum phase;
- Materials: SoI, Ssi, SiGe, SiC, C, InSb, InAs, strained Si/Ge, InGaAs, Cu, high-k dielectrics, polymer, DNA, RNA and bio-cells;
- Structures: 2D and 3D structures, vertical structures, heterogeneous structures, nanotubes, nanowires, nanoparticles, quantum dots, single molecules, atoms and spintronic devices;
- Fabrication methods: bottom up, top down, templated, printing, self-assembled, bio-generated and other disruptive approaches to lithography;

- Functions: logic, memory, sensors, actuators, wet interfaces, biomimetics, cryptography;
- Architectures: highly scalable, reconfigurable, programmable, fault tolerant, self-testing, self-repairing, manufacturable, low power, asynchronous, spatial and temporal redundancy, biologically-inspired, ballistic and coherent.

The medium-term impact of many of these technologies may initially occur in niche *Moore than Moore* areas, which would provide economic benefits and stimuli before impacting on the *More of Moore* challenge. The recommendations presented below are aimed at positioning the EU at the forefront of these developments, thereby maximising the economic and societal gains from these future and emerging technologies.

# 3. Recommendations

## 3a Summary of recommendations

**Recommendation 1: Cooperative research on "*System-ability*" of emerging ICT technologies and devices.**

**Challenge:** Develop radically new design methods and tools for systems with over 100 billion nano-devices, exhibiting new characteristics and variability, while reaching the objectives of low power consumption, reliability, evolvability and affordable design effort.

**Recommendation 2: Exploring the interfacing of cell-level biology with nano-electronics.**

**Challenge:** Experiment with and develop new ways to implement bidirectional interfaces between man-made electronic systems with living entities, at the cellular scale and below. Develop new information processing or communication elements based on biological structures, which would open the way to replicate biological properties, such as growing, shrinking and reconfiguring electronics

**Recommendation 3. Future interconnects for heterogenous system integration**
**Challenge:** Research the basis for future on-chip interconnects, exhibiting lower delays and power consumption, while providing required signal integrity and while also considering ease of design and manufacturing.

**Recommendation 4: Post CMOS devices and storage**

**Challenge:** To research new paradigms or to invent new realisations of emerging paradigms for switches, memories, interconnects or other functions that would overcome some of the expected limitations in the further scaling of current industrial technologies such as CMOS devices.

**Recommendation 5 Nanoelectromechnical systems (NEMS)**

**Challenge:** Develop new technologies and applications of NEMS, in particular, pushing the downscaling limits and exploring the application potential of massively parallel arrays of NEMS.

**Recommendation 6: Nanotechnologies for quantum-coherent systems**

**Challenge:** Explore quantum properties in nanoscale devices reaching the quantum limit, for the development of information processing, communication and sensing.

## 3b Detailed recommendations

**Recommendation 1: Cooperative research on "*System-ability*" of emerging ICT technologies and devices.**

**Challenge:** Develop radically new design methods and tools for systems with over 100 billion nano-devices, exhibiting new characteristics and variability, while reaching the objectives of low power consumption, reliability, evolvability and affordable design effort.

### 1a Rationale

In evolving to sub 10nm scaling, we will pass through many new device architectures exploiting new materials and new manufacturing technologies, including non-classical CMOS devices such as multiple-gate FETS and later to beyond-CMOS devices, possibly involving carbon nanotubes or single molecules. New information carriers such as spin, photons, orbitrons and phase may give rise to new devices and interconnects. These devices may exhibit properties that are quite different from those of CMOS gates.

However, device-oriented researchers currently pay little attention to the ability for meaningful application of these emerging devices to future systems and few system architects are investigating what new system-design issues will arise when integrated systems with 100 billion devices become possible. Currently-available deterministic design tools are increasingly inadequate for CMOS and the tools needed for future nanoscale-system design do not currently exist. At present, it is not clear if it will be possible to abstract the unusual behaviour of nanoscale devices, possibly exploiting quantum effects, so that systems can be developed from simple components, as is currently the case for CMOS gates, or if radically new tools and design flows and architectures will be needed to exploit the nanoscale.

### 1b Expected benefits

New tools would allow the investigation of the interaction between computation, storage and communication (interconnects) and the design of programmable and/or reconfigurable systems, which minimise and better amortise the non-recurring engineering cost of >100 billion device architectures. New tools should lead to an understanding of power and/or energy consumption of all system functionalities and their interaction, and ultimately to better systems than equivalent scaled silicon solutions. They would enable the development of analog or mixed signal systems from these devices, evaluation of their added value with respect to the best silicon solutions achievable at the end of scaling and investigation of their potential for other functionality besides computing, such as sensing and actuating.

### 1c Objectives

The objective is to research new paradigms for systems design, leading to the design of cost-effective and reliable systems, formed from uncertain components. They

should cover system-level requirements, and match to new device and interconnect technologies and new computational paradigms.  that work with

- multilevel, multiscale architectures
- the statistical nature of nanoscale devices,
- post fabrication correction and configuration,
- fault detection and correction,
- both static and soft errors
- power and thermal management,
- evolvability of systems.

At the device level, new atomistic simulation tools should be used to generate libraries of models and abstractions to represent the nano building blocks (including their device variability), which feed into higher-level tools.

**1d Research Focus**

Efforts should also be made to develop reliable, predictive and quantitative nanoscale-device simulation methods and to interface these into higher-level design tools comprehending extreme heterogeneity, thereby underpinning cooperative long-term research on fault- and variability-tolerant systems of over 100 billion nano-devices. Research should focus the tools needed to understand new materials, such as SoI, Ssi, SiGe, SiC, C, InSb, InAs, strained Si/Ge, InGaAs, Cu, high-k dielectrics, polymer, DNA, RNA and new structures, such as 2D and 3D structures, vertical structures, heterogeneous structures, nanotubes, nanowires, nanoparticles, quantum dots, single molecules, spintronic devices. Research should take place within multi-disciplinary teams of nano-technology researchers and system architects, that would also be able to drive device research into realistic avenues that can lead to economically-justifiable nano-electronic systems for the future.

**1e Why now?**

European system providers critically need access to efficient design methods and tools and the expertise to deploy and tune such tools, in order to capitalise on superior abilities to design and develop application-oriented embedded systems. This activity is emerging rapidly in the US and in Japan.  Without such efforts, device work funded under earlier national and EC programmes may not result in added value for society and “beyond CMOS” systems will be dominated by US and Asian companies.

**Recommendation 2: Exploring the interfacing of cell-level biology with nano-electronics.**

**Challenge:** Experiment with and develop new ways to implement bidirectional interfaces between man-made electronic systems with living entities, at the cellular scale and below. Develop new information processing or communication elements based on biological structures, which would open the way to replicate biological properties, such as growing, shrinking and reconfiguring electronics

**2a Rationale**

CMOS scaling of computing systems will allow intelligence to be embedded in nearly all material objects, and increasingly in systems tightly coupled with living beings. Therefore there is a need to develop the theoretical and experimental bases for new technologies for the integration of biological and non-biological components. Advances in our understanding and harnessing of biological processes also open up new avenues for man-made systems that exploit biological materials and information processing schemes, and their growth, healing and evolutionary properties. The resulting hybrid bio-electronic systems require the establishment of a whole new set of protocols and techniques to work at the interface between well-established micro and nanoelectronics technologies and the biochemical processing structures prevalent in living beings.

**2b Expected benefits**

This research will create new interfaces between nano-scaled electronics and living tissues, which will broaden the scope of systems on chip and systems in package that can be delivered. Microelectronics and nanoelectronics may benefit from new fabrication techniques based on biochemical processing that take advantage of evolutionary processes common in the bioworld. Other benefits will include laboratories-on-a-chip and laboratories-in-a-pill, involving electronic sensors with nanowires, nanotubes, magnetoresistive sensors, optical waveguides, photonic crystals, magnetic beads for manipulation of biomolecules and biochip arrays with wide-ranging applications to e-health.
At an application level, the technologies could lead to new sensors for quick biomedical diagnostics and analysis, requiring a minimum amount of sample (especially blood), specific, easy to handle, pollution-free, nontoxic and cheap. The research highlighted here will also provide the material basis of future health products that will help counter the rising cost of healthcare and wellness, the aging of society and accelerate the development of advanced methods for drug development, DNA sequencing and drug delivery, by embedding signal processing, computing and communication in living beings for monitoring, prevention and curing.

**2c Objectives**

By its very nature, this is an area where top-down lithographic and bottom-up self-organizing principles come together. In particular research is needed in the following areas:

Bio-nano transduction, including:

- Bidirectional interfaces between the biochemical world of living tissues and nano-electronics –sensing, actuation, control and communication.
- “Intelligent" processing of complex biomedical information close to the actual bio-electronic junction.

Growable electronics, including:

- Circuits and connections which grow, shrink or reconfigure according to demands on functionality
- Evolvable hardware as a new concept straddling nano- and bio-technology and emergent design
- Molecular templating with synthetic or engineered natural biomolecules

**2d Research Focus**

One research focus is the creation of biomimetic interfaces that allow living cells to behave as if they were residing in a natural environment, and that guides neuronal growth, with exact control over the spot where a functional synapse or electrical junction has to be formed. The interface must also provide the transduction between ionic activity in the cells and electronic responses in the nano-scale electronic sensors. This should be complemented by research on the direct coupling of sensors with the intelligent processing components. This will require breakthroughs in biosensors, which will need the above chemical interfacing, ultra-low power algorithms and nano-scaled electronic system architectures, as well as process and design technologies supporting them. The outcome will also be useful in other application domains like ambient intelligence and autonomous environmental sensor networks.

New paradigms are expected to emerge for computing and ICT based on natural models , including architectures mimicking the brain (neuronal networks), systems capable of self assembly (using vesicles for instance), direct utilisation of actual neural networks (see below) and the use of cells, which could be genetically modified to create computing capability. Routes to growable electronics include self-assembly by modifying genetic code in an evolutionary way and self-assembly through programming oligo-nucleotides

**2e Why now?**

Clearly such research can only be based on joint efforts of multidisciplinary teams of researchers from the fields of biology, chemistry, micro- and nano-systems and information technology. Europe has some leading groups, but will begin to lag behind competitors in the US, unless multidisciplinary research teams are created, which combine existing European expertise and knowledge in the relevant fields needed to compete in the area of nanobiotechnology transfer and nano-bio-cognition transfer.

**Recommendation 3. Future interconnects for heterogenous system integration**

**Challenge:** Research the basis for future on-chip interconnects, exhibiting lower delays and power consumption, while providing required signal integrity and while also considering ease of design and manufacturing.

**3a Rationale**

Despite an early start on nanoelectronic devices since the mid-1990s, very few advanced research projects on interconnects resulted from the calls in the IST/FET programme. Present challenges for interconnects include delay, power consumption, signal integrity (cross talk, noise).
Current nanoscale research efforts on interconnects provide a number of promising ideas, which require further development and especially integration into system-wide interconnect concepts. Molecular interconnects using nucleic acid (RNA, DNA)-assembled wires, molecular templating and molecular recognition could be a route to automate on-chip wiring. Diverse templating has been achieved for 15nm Au particles assembled between Au contacts, but so far only activated, non-ohmic conduction has been demonstrated. Chemical or biochemical (DNA) templates for assembling functional carbon nanotubes devices are also being developed, including a recently-demonstrated "lithography free" nanotube FET assembled onto DNA strands. The challenges here are to prepare individual devices, assemble a large number of them in a dynamic and (re)configurable way and ensure good electrical properties of the interconnects based, for example, on metallised nucleic acids. Other routes to self-assembly involves the growth of nanowires or nanotubes at pre-defined locations.

**3b Expected benefits**

Whereas critical dimensions of transistors are now below 100nm, the widths of interconnects are still on a micron scale, because, for example Cu resistance becomes worse at low dimensions due to boundary scattering and defects and as a consequence, approximately 75% of power is dissipated in interconnects rather than active devices. This in turn leads to short battery life in laptops and handheld devices. The proposed research will overcome these limitations. Self-assembly, and bio inspired fabrication in particular may lead to a revolution in the fabrication processes especially by lowering the costs of fabrication.

**3c Objectives**

Research objectives should cover:

New carriers, materials, structures, for the implementation of interconnections, including

- Nanowires and nanotubes, leading to new interconnects in 2D and 3D ICs,
- Disruptive, on-chip opto-electronics
- 3d architectures for self-assembling neural-network systems.

Interconnect-lean architectures and other architectures aiming at improving interconnection performance

Viability of self-assembly, usability of a canonical set of functions and regular layouts for general regular, modular, scaleable and reusable interconnect schemes, and whether or not the brain (high connectivity etc) is a good model for future IT systems.

**3d Research Focus**

Research should focus on future interconnect technologies and feed into the activities under recommendation 1, which would enable rapid integration of new knowledge about interconnects and devices into system-level design.

Promising avenues include the use of nanotubes, recently-synthesised molecules non-linear wave propagation and 3d architectures (which allow higher integration density, less I/Os, shorter wires, less power and higher speed). Nerve bundles are an example of unidirectional, self-restored signal propagation, chemically assisted guided growth and life-long repair capability. To avoid problems associated with high-density interconnects, non-local processing in non-charge-based devices and interconnect-lean architectures such as cellular automata could be explored. Semi-conductor nanowire-based electronics is currently showing particular promise. The growth of nanowires is a bottom up, self-assembly process, which produces wires with diameters as small as 5 nm.

A different approach to system-level interconnects to overcome constraints of a single clock, there is a move to asynchronous, on-chip internet-like networks. Challenges here occur, because key parameters such as latency, energy consumption, abundancy of wires and pins and deterministic wiring are different from the standard internet.

**3e Why now**

Strong generalist centres exist, but there is little top-down driven research and no EU equivalent of eg the US-funded Marco Interconnect Centre.. Action is needed now to correct this European imbalance and ensure that the EU does not lag behind in this important technology.

**Recommendation 4: Post CMOS devices and storage**

**Challenge:** To research new paradigms or to invent new realisations of emerging paradigms for switches, memories, interconnects or other functions that would overcome some of the expected limitations in the further scaling of current industrial technologies such as CMOS devices.

**4a Rationale**

Research is needed to identify and demonstrate new nanodevices and circuits that have a clear potential to outperform scaled CMOS for some characteristics. These could be disruptive or based on evolution from existing technologies such as CMOS or photonics.

One direction is to develop devices that integrate gracefully with CMOS and to identify architectures that exploit the advantages of both CMOS "hosts" and nanotech blocks. New materials are likely to be compatible with Si circuit fabrication and Si circuits must be more tolerant of other materials. Directed growth/assembly on Si should include materials for which growth/assembly can occur under conditions which do not degrade the Si circuit and an increase in the temperature stability of Si circuits should be sought through the use of alternative materials.

Devices based on photonics principles would be highly desirable for their integration with interconnects and parallel processing. Emerging concepts and applications in nano-photonics include arrays of micro-gratings recorded at different wavelengths for multiplexed and multilayer storage, mechanically-flexible supports for storage of personal data, holographic and near-field, multi-level storage with pico- and femto-second access times and the delivery of long-term removable storage with lifetimes in excess of 100 years.

**4b Expected benefits**

The electronics industry and increasingly, all industries embedding electronics in their products, are relying on a continuous increase of performance and decrease of cost of electronic systems. Pursuing this trend beyond the expected slow-down of shrinking according to Moore's law is a key challenge for future industrial development. The switch to a different technology will only be economic if a radical improvement is foreseen in terms of performance, cost, size or power consumption. On the scale of the next decade, magnetic memory and logic could progress to 10 times faster programming speed, lower power consumption, lower operation voltage, but possibly still low integration density, because large switching currents require wide word lines. FPGAs could develop with steadily increasing signal amplitudes (now at ~300% MR change) and low signal-to-noise ratios. Alternative spin solutions, perhaps using self-assembled nanoparticles, could mimic brain-like learning, including self-programming logic and feedback. If the above progress is delivered, MTJs could provide a unified chip solution, with logic and memory CPU, ROM, DRAM and HDD as a single system on chip. Purely electronic switching, via spin transfer will remove the need for word lines, which is a major disadvantage in current devices. Recent strong progress in semiconductor nanowire and nanotube research suggests

that this may provide a generic and disruptive technology leading to new FETs, RTDs, SETs, memory applications, on-chip opto-electronics, thermoelectrics and solar cells, spintronics, nanomechanics and biosensor applications.

**4c Objectives**

Research objectives include:

- Identification and proof-of-concept of nanodevices that realise appropriate logic, memory, sensing or other functions.
- Identification and research into nanodevices and that integrate gracefully with CMOS and architectures that exploit the advantages of both CMOS "hosts" and nanotech blocks.
- Directed growth/assembly on Si of narrow-gap semiconductors, nanostructured dielectrics, photonic crystals and cavities, organic molecules and carbon nanotubes, spintronics.
- (Nano-) photonic integration for interconnects and parallel processing.
- Nano to micro interfacing, including energy efficiency, signal integrity and system-ability
- Routes to post CMOS storage

**4d Research focus**

Emphasis should be placed on technologies that have clear potential for performance improvement, or that would open the way to bottom-up manufacturing, and/or that have the potential to integrate with silicon, or offer clear advantages in the post-CMOS era. The issue of interfacing with contacts and communication among concatenated devices is absolutely crucial and may have to be solved *before* these devices can be incorporated into higher-level architectures. The future could be to fabricate small circuits-level systems based on a limited number of nanodevices interconnected at the nano-level with inputs and outputs to the macro world, study in particular their collective behaviour and develop efficient connections to the macro-world. Reliable ab initio simulation tools will be needed to take into account the quantum nature of the physical phenomena at the basis of the device operation and the collective association of the devices in systems.

Critical issues for nanotube and molecular electronics include the currently-unknown, ultimate precision and reliability of bottom-up techniques and the question of how to achieve precise positioning, growth and handling of a huge number of nano-objects (CNTs, nanowires and nanoparticles) to Å or even sub- Å accuracy. For these reasons, the issues of precision, error correction, yield, 3D, or environment for example have to be considered. Hybridisation to silicon technologies is likely to be necessary, but brings in a number of materials issues and may require a mix of bottom-up and top-down technologies. Routes for future fabrication could involve block copolymer lithography, guided self-assembly (possibly photon assisted) and biological toolkits for fabrication, including proteins, nucleic acids and viruses. Nano to micro interfacing will be necessary, interfacing to the environment should be mastered, complexity and faults must be handled and quantitative multi-scale modelling will be needed.

**4e Why now?**

The current shrinking of CMOS devices is likely to slow down and reach some limitations in a 10-year time frame. Other solutions must be researched now to enable industrial research and take-up in 2015-2020.Framework 6 has witnessed significant progress in several of the novel materials mentioned above, and this continues to progress worldwide. The EU must continue competing in this area if it is to remain a significant future player in nanoelectronics.

**Recommendation 5 Nanoelectromechnical systems (NEMS)**

**Challenge:** Develop new technologies and applications of NEMS, in particular, pushing the downscaling limits and exploring the application potential of massively parallel arrays of NEMS.

**5a Rationale**

Nanoelectromechanical systems (NEMS) have potential applications to microwave signal processing, mechanically detecting magnetic resonance imaging, BioNEMS (sensors and actuators), micro-nanofluidics (single molecule sensing-analysing), data storage (memories, probe detection for magnetic storage) and operation at the quantum limit. A rapidly-developing technology, which promises a broad range of contributions to future *More than Moore* developments, involves the use of scanning probe arrays, with integrated write/read/erase functionality. This progress has led to proposals and research activities for a range of other probe array storage techniques, such as thermomechanical recording on polymer films, charge based on ferroelectric media, phase change recording using an array of e-beam emitters, phase change recording using conduction probes, probe based magnetic recording, and array-based, near-field optical recording. Extremely parallel arrays of NEMS may lead to new storage and system architectures as well as currently-unknown applications in science and technology and could represent a unique opportunity for Europe now to establish probe array technology leadership position.

**5b Expected benefits**

Developments in nanoscale mechanics could revolutionize IST by bringing back mechanics as an efficient high-speed low-power technology to store and process information.
Other promising NEMS developments relate to sensors, actuators and other non-logical functions. These include biologically-inspired artificial cilia or nanopores, made possible by new technologies and sciences. Applications include sensors for acoustics, ultrasound, chemistry and flow at the single molecule level. Other examples include artificial noses and carbon-nanotube and molecular-scale motors. Nanotube and single-molecule NEMS also have potential applications to microwave signal processing, mechanically detecting magnetic resonance imaging, bio-sensors and bio-actuators, micro-nanofluidics, single molecule sensing and analysing, and operation at the quantum limit.

Expected benefits to life sciences are: detection of molecular interactions using probe and cantilever arrays, parallel topography measurements of biological samples in their natural environment, including nanoscale analysis of living cells; parallel force spectroscopy, including single molecule and single atom pulling; protein folding; binding force measurements and probe functionalization for specific tip-sample interactions, for example via heated or conductive tips.

Expected benefits to materials science include: millipede maskless lithography, nanoscale dispensing and nanoscale deposition of electronic materials. The latter should overcome a critical challenge of dip-pen lithography, which is to modulate deposition from tip, avoiding contamination when registering to previously-fabricated

structures. New tools are also envisaged, such as the development of scanning force endoscopes.

**5c Objectives**

Objectives for NEMS research include the development of:

- Nano-object-based NEMS, with potential applications to microwave signal processing, mechanically detecting magnetic resonance imaging, bio-sensors and bio-actuators, micro-nanofluidics, single-molecule sensing-analysing, data storage and operation at the quantum limit.

- VLSI like arrays of sensors, or probes with integrated sensing and actuation, eventually equipped with local data-processing and heterogeneous integration on CMOS. – for large area imaging or inspection tools.

- VLSI like arrays of probes or sources for manipulating and modifying on the nanometer scale – for maskless lithography, maskless material deposition or arranging and sorting nanoscale objects.

**5d Research focus**

This research is focused on developing nanoelectromechanical systems which are operable at the molecular or atomic level and deploying these in a wide variety of applications. CNT-NEMS engineering challenges include controlled positioning of carbon nanotubes, primarily through self-assembly in solution or localised and oriented growth, the development of nanoscale CNT and molecular motors, the pursuit of ultrahigh Q and frequencies, development of efficient detection and actuation schemes, reproducible nanofabrication and RF operation. Other nanotubes of potential interest are carbon-boron-nitride and cyclacene-based nanotubes and microtubulin. Rotational carbon nanotube motors are a recent development with a range of potential applications. A key question is the extent to which parallel arrays of NEMS can be developed into usable systems and what new tools are needed to realise the immense potential of NEMS. The integration of many equal or differently-tasked NEMS elements via probe array technology would create further functionality and added value.

**5e Why now?**

Scanning Probe Technology (SPT) is an important enabler for nanoscience and technology. Since the STM was invented in 1981, various probe approaches have been developed, including STM, AFM, MFM, SNOM. Europe led the initial SPT inventions and developments and is still among the leaders in many science fields. Europe however missed the business opportunities, with USA and Japan clearly leading the $150M-$200M instrumentation market. A different course to be exploited now is to incorporate NEMS technology in systems and products, to produce new functionalities. NEMS-array technology is another direction in this evolution and the EU must invest in this area now if the opportunities on offer are not to be lost. Probe Arrays for “every” application could use common platform with customized probe arrays. Nano-object based NEMS can rely on pioneering teams in the EU. Given the

broadening of the scope and the accelerating pace of that research worldwide, the EU needs a strong and coordinated action to maintain a competitive position at this early stage of technological developments.

**Recommendation 6: Nanotechnologies for quantum-coherent systems**

**Challenge:** Explore quantum properties in nanoscale devices reaching the quantum limit, for the development of information processing, communication, and sensing.

**6a Rationale**

Nanoscale quantum-coherent systems have the potential to revolutionize many areas of science and technology. Quantum Information Processing and Communication (QIPC), for example, exploits fundamentally new modes of computation and communication, using a mechanism that is completely different from binary logic. A second example involves the possibility of performing computations within single molecules, quantum wires and quantum-dot hetrostructures, and linking these through incoherent interconnects. A third involves the development of nanomechanical resonators and the possibility of building quantum-coherent mechanical devices. The quantum limit of classical transistors, such as resonant tunneling transistors (RTT), which imposes a physical restriction to the continued downscaling of conventional devices, could also be exploited in a constructive way, for instance to develop new multi-terminal switches implemented in non-classical architectures.

**6b Expected benefits**

The development of emerging quantum-coherent systems will provide new technologies for nanoelectronics, nanophotonics and nanoelectromechanics, microwave technology, sensors and measurements with ultimate sensitivity and ensure a robust, future industrial base in Europe for IST hardware.

**6c Objectives**

Objectives include:

- Developing reliable technologies for reproducibly engineering quantum systems involving molecules, quantum wires, quantum dots, combined with nanomechanics and nanophotonics.
- Exploring phenomena at the quantum limit or exploiting quantum effects and developing nanodevices based on these.
- Developing interfaces and quantum-limited measurements, eg for intra-molecular and one-dimensional solid-state coherent electronics to fulfill its potential to provide useful components and networks.
- Investigating new types of solid-state qubits and scalable coherent systems that could form the basis for building large-scale coherent systems and practical quantum computers.

**6d Research focus**

The aim is to engineer and harness quantum-coherent systems, exploiting solid-state micro- and nanotechnology, materials science, and novel or complex nano-based input-output devices connecting the outside world with individual nanoscale, atomic or hybrid quantum processors. In addition, various inhomogeneities may lead to fluctuations of voltages, currents and magnetic fluxes, as well as difficulties in reproducibly fabricating devices with small variations of essential parameters. Many

of these problems are also barriers to be overcome in the development of intra-molecular computing.

**6e Why now?**

The further progress of electronic and mechanical molecular, semiconductor and superconductor quantum-coherent systems during the time of FP7 requires massive efforts in nanoelectronics, nanomechanics, nanophotonics and materials engineering, both to engineer specific structures which are fundamental to on-chip integration and scaling of quantum systems, and to study decoherence encountered in scaling down components and scaling up systems.

The future of solid-state quantum-coherent systems will hinge on our ability to create perfect materials, free of static and dynamic defects and to engineer both extremely-low noise levels and extremely-long coherence times. The semiconductor industry has been developing silicon and III-V technology during 50 years, and developed tools and processes for fabricating materials and devices with small numbers of defects and excellent reproducibility. The technology for solid-state quantum information processing (SSQIP) is rudimentary by comparison. Quantum technology for superconducting quantum interference devices (SQUIDs) has been developed during the past 25 years, and for single-electron transistors (SETs) during the past 15 years. However, the field of SSQIP for coherent such devices is only about 5 years old, and the barriers to progress are only just beginning to be discovered.