Closed-Form Equations for Through-Silicon Via (TSV) Parasitics in 3-D Integrated Circuits

(Extended Abstract)

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3-D integration using TSVs to interconnect multiple silicon dies in a single chip can offer significant improvements over 2-D Integrated Circuits (ICs) in performance, heterogeneous integration, footprint and integration density [1]. Accurate electrical models of TSV structures are essential in estimating delay, signal integrity (SI) and power integrity (PI) of circuits and interconnects in the design and verification of 3-D ICs. To the authors' best knowledge, no cohesive DC parasitic parameter models for TSVs in a bundle have been reported in the literature [2], [3], [4]. This paper proposes a set of self-consistent equations for resistance (R), capacitance (C) and inductance (L) of TSVs in a bundle, and presents a reduced-order equivalent circuit including capacitive and inductive coupling. The analytic forms for R, C and L eliminate the need for a computationally expensive field solver and enable efficient delay, SI and PI related analyses early in the design flow.

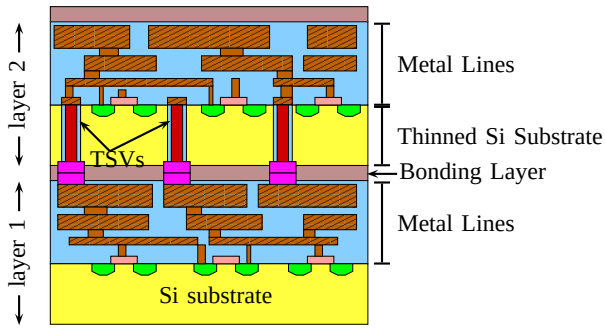

Fig. 1: A General Bulk CMOS 3-D Stack Arrangement

A 3D-IC is shown in Fig. 1 in which two bulk silicon dies are bonded on top of each other and electrically interconnected using TSVs. These TSVs are assumed to have a uniform circular cross-section. The material commonly used for TSVs is Cu, with an annular dielectric barrier (SiO_2 or Si_3N_4) surrounding the Cu cylinder. The insulating dielectric acts as a barrier to the Cu TSV, preventing the migration of Cu ions into the Si substrate which can degrade device performance by inducing leakage currents. It also electrically isolates the Cu cylinder from the substrate, providing improved isolation to power and ground planes. Further, a thin annular TiN layer is usually deposited between the Cu and SiO_2 layers, which acts as an adhesion layer and also concentrates the current in the Cu bar due to its high resistivity [5]. This TiN barrier layer has been neglected for the sake of simplicity and to reduce computational time in the field solver, since its inclusion has an apparently negligible effect on the parasitic parameters.

The general methodology adopted in the modelling is to fit equations to empirical data obtained from a field solver for a range of physical dimensions using analytical forms suggested by physical laws. In a 3-D chip stack, the likely configuration for TSVs is in a regular matrix, for which a representative unit is a 3×3 bundle (see Fig. 2). Such a structure has been simulated in a 3-D/2-D quasi-static electromagnetic-field solver specifically used for parasitic extraction of electronic components [6]. It is assumed that the TSV structure and silicon substrate is floating as layout level information describing adjacent ground layers as defined by nearby metal lines distributing power and ground is not present early in the design flow. Also, it is assumed that the substrate is highly resistive [3] as is typical for low noise applications. Further,

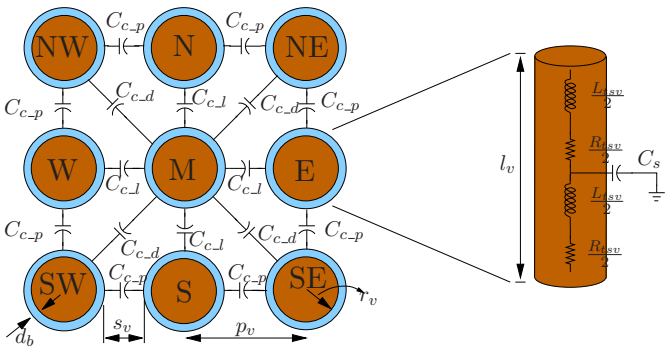

Fig. 2: Representative unit for a TSV bundle assuming a uniform circular cross-section of Cu, with an annular dielectric barrier of SiO_2 [5].

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the thickness of the SiO_2 barrier d_b is set to be constant equal to $0.2\mu m$ as it is fixed for a given technology. The simulated ranges for length (l_v), radius (r_v), and inter-via spacing (s_v) (see Fig. 2) are $20\mu m \leq l_v \leq 140\mu m$, $10\mu m \leq r_v \leq 45\mu m$ and $40\mu m \leq s_v \leq 140\mu m$ respectively, in corresponding steps of $40\mu m$, $5\mu m$ and $20\mu m$. These values are representative of most TSV technologies commonly reported.

Resistance of a TSV can be described using the traditional function of conductivity (σ) and cross-sectional area:

$$R_{via} = \frac{l_v}{\sigma \pi r_v^2}. \tag{1}$$

The model of (1) is accurate to within 98% of the simulated values.

In a TSV bundle that comprises an $m \times m$ matrix, all self and coupling terms are given by:

$$C_{bundle} = \begin{bmatrix} C_{1,1} & -C_{1,2} & \cdots & -C_{1,n} \\ -C_{2,1} & C_{2,2} & \cdots & -C_{2,n} \\ \vdots & \vdots & \ddots & \vdots \\ -C_{n,1} & -C_{n,2} & \cdots & C_{n,n} \end{bmatrix}, \tag{2}$$

where $n = m^2$. In (2), the diagonal element $C_{i,i}$ represents the sum of the self ($C_{i,0}$) and inter-via coupling capacitances ($C_{i,j}$) as given in (3):

$$C_{i,i} = C_{i,0} + \sum_{j=1}^{n} C_{i,j}. \tag{3}$$

The capacitance matrix is sparse; the main diagonal and adjacent diagonals representing coupling terms to nearest neighbours are populated while the other entries are vanishingly small in comparison (Refer Fig. 3). With reference to the naming convention given in Fig. 2 the distances from M TSV to N, E, S and W TSVs are the same, while the distances to NE, NW, SE and SW TSVs are also equal. Therefore, the capacitance formulae for the total capacitance of M, N, and NE TSVs ($C_{i,i}$), and the coupling terms to their nearest neighbours ($C_{i,j}$) as defined in Fig. 2 are a representative unit for a TSV bundle of any size.

With reference to Fig. 2, the self capacitance $C_s = C_{i,0}$ of a TSV is of the form:

$$C_s = C_{tsv} - k_1 C_{tsv} e^{\left(k_2 \frac{p_v}{r_v} + k_3 \frac{p_v}{l_v}\right)} \left[k_4 \left(\frac{l_v}{r_v}\right)^{k_5} + k_6 \left(\frac{p_v}{r_v}\right)^{k_7} + k_8 \right], \tag{4}$$

where C_{tsv} is the capacitance of an isolated TSV given by:

$$C_{tsv} = \frac{63.34 \epsilon_0 l_v}{ln\left(1 + 5.26 \frac{l_v}{r_v}\right)} \tag{5}$$

and the constants in (4) are defined in the first three rows of Table I. In (4) the constants k_2 and k_3 are negative, and therefore as p_v approaches infinity, C_s approaches C_{tsv}, the capacitance of an isolated TSV given in (5), with a maximum error contained to 6% for the simulated range.

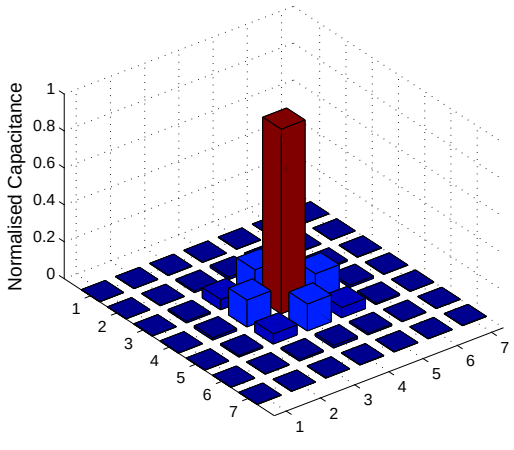

Fig. 3: Capacitive coupling between the centre TSV of a 7 × 7 bundle with its surrounding TSVs. Values are normalized to the total capacitance of the center TSV.

The formula for the coupling capacitance ($C_c = C_{i,j}$) terms of (2) for $i \neq j$ (defined in Fig 2) is of the form:

$$C_c = \frac{k_1 \epsilon_0 l_v}{ln\left(k_2 \frac{p_v}{r_v}\right)} \left[1 + k_3 \left(\frac{p_v}{r_v}\right)^{k_4} + k_5 \left(\frac{l_v}{r_v}\right)^{k_6} + k_7 \left(\frac{p_v}{l_v}\right)^{k_8} \right], \tag{6}$$

with the constants $k_1, \cdots, k_8$ corresponding to C_{c_l}, C_{c_p} and C_{c_d} defined in the last three rows of Table I respectively.

As can be seen in Table I, all models have a *minimum* accuracy over the full simulated range of approximately 90%. It should be noted that the C_{s_M} value is valid only when $\frac{C_{s\_M}}{C_{t\_M}} \geq 0.09$, where C_{t_M} ($C_{i,i}$) is the total capacitance of the M TSV. Below this range C_{s_M} values are so small that they are negligible for any meaningful delay, SI or PI analysis. For those geometries the self capacitance values are in fact indistinguishable from numerical noise in the field solver, as the ground component is very small. Comparisons between the calculated and extracted C_t values for M, N, and NE TSVs for the whole range have maximum absolute errors of 2.3%, 3.6% and 2.9% respectively.

The self (L_s) and mutual (L_m) inductance terms for a TSV bundle are defined by:

$$L_{bundle} = \begin{bmatrix} L_{1,1} & L_{1,2} & \cdots & L_{1,n} \\ L_{2,1} & L_{2,2} & \cdots & L_{2,n} \\ \vdots & \vdots & \ddots & \vdots \\ L_{n,1} & L_{n,2} & \cdots & L_{n,n} \end{bmatrix}, \tag{7}$$

where diagonal elements represent the self inductance terms, and off diagonal elements the mutual inductance terms. Inductive coupling is long range and therefore the inductance matrix is well populated, with all elements being non-negligible (See Fig. 4). The self inductance (L_s) can be estimated from:

		k_1	k_2	k_3	k_4	k_5	k_6	k_7	k_8	Max. % Error	Average % Error
(a)	C_{s_M}	0.1505	-0.0071	-0.0291	0.1849	-1.9371	6.9577	-0.0131	-0.0354	13.0	6.3
(b)	C_{s_N}	0.6876	-0.0390	-0.0583	1.8076	-0.2229	11.3537	0.0402	-13.1813	10.2	1.9
(c)	C_{s_NE}	0.3406	-0.0345	-0.0686	5.0708	-0.1530	-5.6346	-0.3859	-0.7643	13.3	2.0
(d)	C_{c_l}	10.191	0.5490	-0.014	0.796	0.054	-1.157	-0.018	-0.600	8.7	1.9
(e)	C_{c_p}	3.180	0.5440	-0.199	0.586	0.122	0.540	2.176	0.110	10.9	1.8
(f)	C_{c_d}	18.117	28.457	-1.734	-2.178	0.600	-0.518	-0.470	0.188	8.0	1.4

TABLE I: Constants for self and coupling capacitance terms of 3×3 TSV bundle (see Fig. 2 for capacitance definitions).

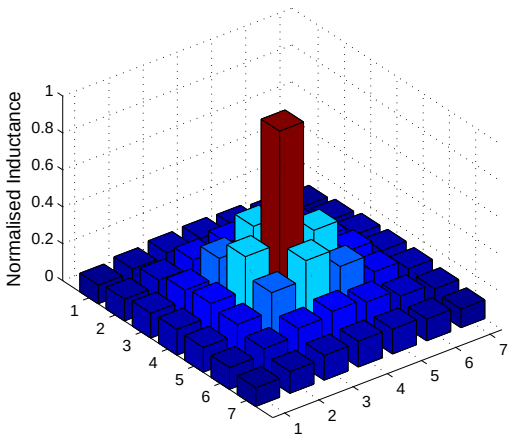

Fig. 4: Mutual inductance between the centre TSV of a 7×7 bundle normalized to self inductance of the centre TSV

$$L_s = \frac{\mu l_v}{2\pi} ln\left(1 + \frac{2.84}{\pi}\frac{l_v}{r_v}\right). \tag{8}$$

This empirical model predicts the self-inductance with 97% accuracy.

In contrast to capacitive coupling, the inductive coupling is long range and the mutual inductance between non-adjacent lines are significant. The mutual inductance (L_m) between any two TSVs in a bundle is defined by:

$$L_m = 0.199\mu l_v ln\left(1 + 0.438\frac{l_v}{d_v}\right), \tag{9}$$

where d_v is the center-to-center distance between the lines. The maximum error in this model is contained to within 8% for the simulated range of physical dimensions.

As the intended use of the compact models is to calculate circuit related metrics, it is important that any deviations in these from the values when using the nominal parasitic values returned by the field solver, is contained. In order to check the sensitivity of the circuit metrics to errors in the parasitic values, simulations were carried out to estimate the 50% delay and coupled noise amplitude with a worst-case switching pattern in a 3×3 bundle. The absolute errors in delay and noise resulting from the recorded *maximum* errors in each parasitic component when the others are held at their nominal values is reported in Table II. Inductance is not considered as its effect is negligible, as shown in the next section. It can be seen that in all cases the error is *less* than the error in the parasitic values predicted by the compact models. Given in the last column are the errors in delay and noise resulting from a worst-case combination of errors in the parasitic values, which is contained to 10% in the case of delay, and 14% in the case of noise. These errors represent the absolute upper bound, and will occur only in the singular case when R_{tsv}, C_s, C_l and C_d are all individually in error by their maximum values simultaneously, and in a manner that maximises the error in the calculated metric.

Parameter	Max. % error in model	% Error in metric	
		Delay	Noise
R_{tsv}	2%	0%	0%
C_s	13%	3%	6%
C_l	8.7%	6%	7%
C_d	8%	1%	1%
R_{tsv}, C_s, C_d, C_l	Worst-case combination	10%	14%

TABLE II: Variation of delay and coupled noise for the center TSV in a 3x3 bundle with worst-case switching

Compact closed-form equations for calculating resistive, inductive and capacitive parasitic parameters of TSV bundles in 3-D ICs were proposed in this paper. These parasitic models were shown to exhibit fidelity; when the model extracted parasitics were used in circuit simulations, the final error in the metrics of delay and noise amplitude when compared to the same simulation using field solver extracted parasitics was less than the error in the parasitics themselves, showing the usefulness of the proposed models.

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