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Class AB regulated cascode current memory cell

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The presented sampled-current memory cell demonstrates class AB operation where the bipolar input current magnitude may exceed twice the quiescent bias current even though full cascode regulation is maintained. Calculation of the necessary safety margin to accommodate process tolerances is shown to be simplified compared with the standard regulated cascode cell.

Introduction: Switched current (SI) signal processing has recently come of age and several interesting designs have emerged for both the basic building blocks [1] and more complex designs [2]. The growth of SI techniques looks set to increase still further because the technological requirements are modest [3], requiring only a single polysilicon layer, and are thus ideally suited to producing analogue circuits on the periphery of digital core chips.

Fundamental to almost any SI design is the memory cell, a number of which are shown in Fig. 1. The simple cell shown in Fig. 1*a* suffers badly from channel length modulation [4] which gives a poor output impedance of approximately $1/g_{ds}$ (typically 500kΩ for a drain current of 100μA).

The cascoded cell of Fig. 1*b* improves the output resistance by approximately a factor of 100 but the penalty paid is that the minimum voltage at the I/O node is at least two threshold voltages plus the body effect of transistor M2, approximately 2.2V in total for *n*FET threshold voltages of 0.9V.

The final circuit of Fig. 1 shows an opamp regulated memory cell. This circuit looks superficially attractive but contains a number of problems which make its implementation unattractive. Assuring stability of the opamp leads to a bandwidth for the whole circuit very much less than that for either of the two previous circuits. The additional complexity is also problematic for circuits with a large number of memory cells.

The regulated cascode cell [5] shown in Fig. 2 has been used as a memory cell and offers a large output resistance of approximately

$$\frac{g_{m_2}g_{m_3}}{g_{ds_1}g_{ds_2}g_{ds_3}} \quad (1)$$

which is typically 10GΩ if all the transistors operate in saturation mode.

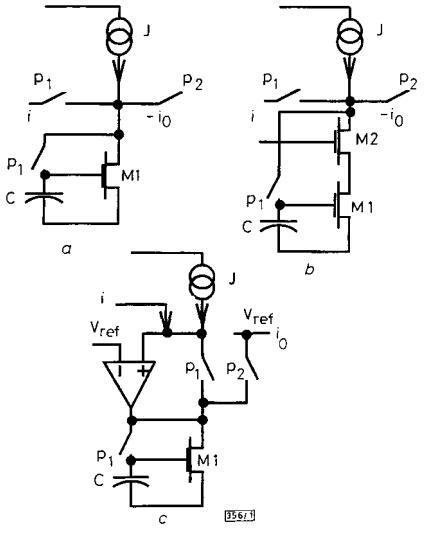

Fig. 1 *Early current memory cells*

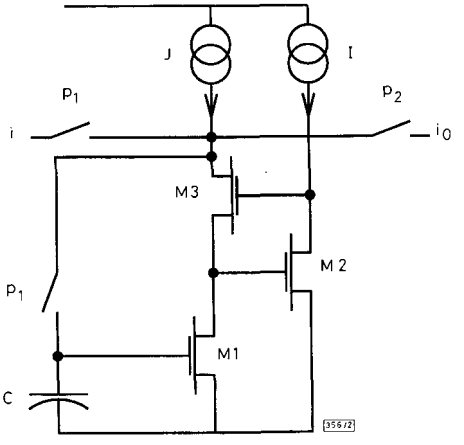

Fig. 2 *Regulated cascode current memory cell*

To obtain a sufficient voltage range at the i/o node it is necessary to run M3 in the linear region of operation so that its drain-source voltage may be reduced to around 0.5 V. Under all input conditions and full process tolerance, the range of allowable aspect ratios for M1 is given by the following two equations:

$$A_{MIN} > \frac{I_{MAX}}{K_{SLOW}((V_{GS_{MAX}}-V_{T_{SLOW}})-V_{DS}/2)V_{DS_{M1}}} \quad (2)$$

and

$$A_{MAX} < \frac{I_{MIN}}{K_{FAST}((V_{GS_{MIN}}-V_{T_{FAST}})-V_{DS}/2)V_{DS_{M1}}} \quad (3)$$

where the symbols have their usual meanings, $I_{MIN/MAX}$ is the input current plus the bias current, A is the aspect ratio (W/L) of M1 and $V_{DS_{M1}}$ is assumed to be constant. These bounding functions are clearly a function of both fast and slow process parameters which tends to lead to extreme values of A_{MIN} and A_{MAX} especially

on a digital process not optimised for high precision analogue work.

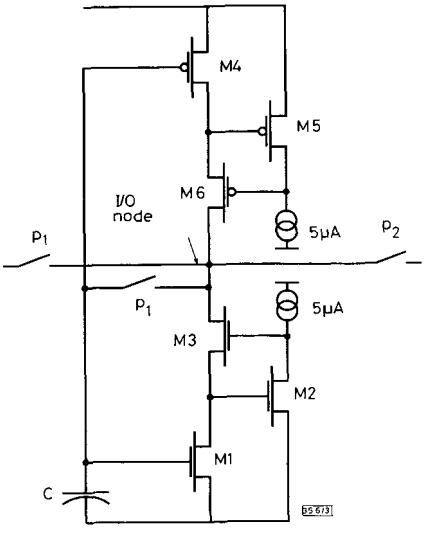

Fig. 3 *Class AB current memory cell*

Class AB current-memory cell: The push-pull regulated cascode cell shown in Fig. 3 allows alteration of the bias current produced by the upper regulated cascode. It has the very desirable feature that as the current through M1 increases, the bias current supplied by M4 decreases. The input current range is therefore increased to the extent that class AB operation is easily possible.

The current provided by the upper and lower regulated cells is given approximately by

$$I_P = |I_{M4}| = K_P A_P((V_{GSP} - V_{TP}) - V_{DSP}/2)V_{DSP} \quad (4)$$

$$I_N = I_{M1} = K_N A_N((V_{GSN} - V_{TN}) - V_{DSN}/2)V_{DSN} \quad (5)$$

and their difference is the input or output current. Assuming that $K_P A_P \simeq K_N A_N$, $|V_{TP}| \simeq V_{TN}$, $V_{DSP} \simeq V_{DSN}$ the difference between the currents may be written as

$$\Delta I = I_P - I_N \simeq KA(V_{GSP} - V_{GSN})V_{DS} \quad (6)$$

The quiescent bias current, I_0, is the current through M_1 (or M_4) with zero input/output current to the cell as a whole and may be written as

$$I_0 = I_N = KA((V_{GSN0} - V_T) - V_{DS_{M1}}/2)V_{DS_{M1}} \quad (7)$$

where V_{GSN0} is the quiescent gate-source voltage of M1. Thus the total input current range is written as

$$\frac{2\Delta I}{I_0} = \frac{2(V_{GSP} - V_{GSN})|_{MAX}}{((V_{GSN0} - V_T) - V_{DS}/2)} \quad (8)$$

Table 1: Principal process parameters

FET	Process	K	V_T
		μA/V²	V
*n*MOS	Slow	24	1.0
	Typical	35	0.8
	Fast	48	0.6
*p*MOS	Slow	9	1.0
	Typical	12	0.8
	Fast	18	0.6

Inserting the values $(V_{GSP} - V_{GSN})|_{MAX} = 2$, $V_{DS} = 1$V and slow parameters (worst case input current range) from Table 1 gives

$$\frac{2\Delta I}{I_0} \simeq 4 \quad (9)$$

This represents a lower limit to the achievable input current range. With typical or fast process parameters the input current range is greater although I_0 is also greater. One great advantage of this circuit is that input current range is defined almost solely by the slow parameter set. The aspect ratios of transistors M1 and M2 may be more accurately defined as a result, and the spread of aspect ratios necessary to accommodate process variations is reduced.

Table 2: Input current range simulation results

Parameter	I_{BIAS}	I_{MAX}	I_{MIN}
	μA	μA	μA
Slow	94.5	201.1	−205.2
Typical	135.2	238.7	−224.7
Fast	171.6	276.4	−235.6

Performance: Table 2 shows the input current limits of the class AB regulated cascode cell in the limit that the IO node voltage is constrained to $1.5 < V_{IO} < 3.5$.

Table 3: Sample and output simulation results

Parameter	I_{IN}	I_{OUT}	I_{ERROR}
	μA	μA	bit
Slow	100.0002	99.9987	16.0
Typical	100.0013	99.9985	15.1
Fast	100.0027	99.9941	13.5

Performing sample and output simulations of the class AB memory cell across slow, typical and fast process parameter sets with a 100μA input current gives the results shown in Table 3. Clearly the current copying accuracy is better than 13bit across the full process range, although it must be stated that charge injection effects due to mismatch of the switch transistors will almost certainly degrade these accuracies.

Conclusion: A novel class AB memory cell suitable for a current mode ADC or DAC has been described and simulated. The design significantly reduces the static bias current and offers the advantage of reduced power consumption while increasing the maximum allowable signal amplitude. By careful consideration of the necessary bias voltages and the use of a novel class AB architecture, the input current range is greatly extended beyond that available with previous current memory cells. Current copying accuracy of 13bit or better has been simulated.

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