Class AB regulated cascode current memory cell

A.H. Bratt, T. Olbrich and A.P. Dorey

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The presented sampled-current memory cell demonstrates class AB operation where the bipolar input current magnitude may exceed twice the quiescent bias current even though full cascode regulation is maintained. Calculation of the necessary safety margin to accommodate process tolerances is shown to be simplified compared with the standard regulated cascode cell.

Introduction: Switched current (SI) signal processing has recently come of age and several interesting designs have emerged for both the basic building blocks [1] and more complex designs [2]. The growth of SI techniques looks set to increase still further because the technological requirements are modest [3], requiring only a single polysilicon layer, and are thus ideally suited to producing analogue circuits on the periphery of digital core chips.

Fundamental to almost any SI design is the memory cell, a number of which are shown in Fig. 1. The simple cell shown in Fig. 1a suffers badly from channel length modulation [4] which gives a poor output impedance of approximately $1/g_{ds}$ (typically 500kΩ for a drain current of 100μA).

The cascoded cell of Fig. 1b improves the output resistance by approximately a factor of 100 but the penalty paid is that the minimum voltage at the i/o node is at least two threshold voltages plus the body effect of transistor M2, approximately 2.2V in total for nFET threshold values of 0.9V.

The final circuit of Fig. 1 shows an opamp regulated memory cell [5] which is typically 100kΩ if all the transistors operate in saturation mode.

The regulated cascode cell [5] shown in Fig. 2 has been used as a memory cell and offers a large output resistance of approximately

$$g_{ms}g_{ds}$$

$$9d_{ds}$$

which is typically 100kΩ if all the transistors operate in saturation mode.

![Fig. 1 Early current memory cells](image1)

![Fig. 2 Regulated cascode current memory cell](image2)
on a digital process not optimised for high precision analogue work.

Class AB current-memory cell: The push-pull regulated cascode cell shown in Fig. 3 allows alteration of the bias current produced by the upper regulated cascode. It has the very desirable feature that as the current through M1 increases, the bias current supplied by M4 decreases. The input current range is therefore increased to the extent that class AB operation is easily possible.

The current provided by the upper and lower regulated cells is given approximately by

\[ I_P = I_{MAX} = K_T A_P (V_{GSUP} - V_{TP}) - 2V_{DSUP} \]  
\[ I_N = I_{MIN} = K_N A_N (V_{GSN} - V_{TN}) - 2V_{DNS} \]

and their difference is the input or output current. Assuming that \( K_T A_P = K_N A_N \), \( |I_P| = |I_N| \), \( V_{DSUP} = V_{DNS} \) the difference between the currents may be written as

\[ \Delta I = I_P - I_N \approx K_A (V_{GSUP} - V_{GSN}) \]

The quiescent bias current, \( I_0 \), is the current through \( M_1 \) (or \( M_2 \)) with zero input/output current to the cell as a whole and may be written as

\[ I_0 = I_N = K_A (V_{GSUP} - V_T) - 2V_{DNS} \]

where \( V_{GSN} \) is the quiescent gate-source voltage of \( M_1 \). Thus the total input current range is written as

\[ \Delta I = \frac{2(V_{GSUP} - V_{GSN})}{I_0} \]

Table 1: Principal process parameters

<table>
<thead>
<tr>
<th>FET</th>
<th>Process</th>
<th>( K )</th>
<th>( V_T )</th>
</tr>
</thead>
<tbody>
<tr>
<td>nMOS</td>
<td>Slow</td>
<td>24</td>
<td>1.0</td>
</tr>
<tr>
<td></td>
<td>Typical</td>
<td>35</td>
<td>0.8</td>
</tr>
<tr>
<td></td>
<td>Fast</td>
<td>48</td>
<td>0.6</td>
</tr>
<tr>
<td>pMOS</td>
<td>Slow</td>
<td>9</td>
<td>1.0</td>
</tr>
<tr>
<td></td>
<td>Typical</td>
<td>12</td>
<td>0.8</td>
</tr>
<tr>
<td></td>
<td>Fast</td>
<td>18</td>
<td>0.6</td>
</tr>
</tbody>
</table>

Inserting the values \( V_{GSUP} - V_{GSN} = 2 \), \( V_T = 1 \) and slow parameters (worst case input current range) from Table 1 gives

\[ \Delta I \approx 4 \]

This represents a lower limit to the achievable input current range. With typical or fast process parameters the input current range is greater although \( I_0 \) is also greater. One great advantage of this circuit is that input current range is defined almost solely by the slow parameter set. The aspect ratios of transistors \( M_1 \) and \( M_2 \) may be more accurately defined as a result, and the spread of aspect ratios necessary to accommodate process variations is reduced.

Table 2: Input current range simulation results

<table>
<thead>
<tr>
<th>Parameter</th>
<th>( I_{MAX} )</th>
<th>( I_{MIN} )</th>
<th>( I_{BMIN} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slow</td>
<td>94.5 ( \mu A )</td>
<td>201.1 ( \mu A )</td>
<td>-205.2 ( \mu A )</td>
</tr>
<tr>
<td>Typical</td>
<td>135.2 ( \mu A )</td>
<td>238.7 ( \mu A )</td>
<td>-224.7 ( \mu A )</td>
</tr>
<tr>
<td>Fast</td>
<td>171.6 ( \mu A )</td>
<td>276.4 ( \mu A )</td>
<td>-235.6 ( \mu A )</td>
</tr>
</tbody>
</table>

Performance: Table 2 shows the input current limits of the class AB regulated cascode cell in the limit that the I0 node voltage is constrained to \( 1.5 < V_{IO} < 3.5 \).

Table 3: Sample and output simulation results

<table>
<thead>
<tr>
<th>Parameter</th>
<th>( I_{IN} )</th>
<th>( I_{OUT} )</th>
<th>( I_{DRY} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slow</td>
<td>100.0002 ( \mu A )</td>
<td>99.9987 ( \mu A )</td>
<td>16.0 ( \mu A )</td>
</tr>
<tr>
<td>Typical</td>
<td>100.0013 ( \mu A )</td>
<td>99.9985 ( \mu A )</td>
<td>15.1 ( \mu A )</td>
</tr>
<tr>
<td>Fast</td>
<td>101.0027 ( \mu A )</td>
<td>99.9941 ( \mu A )</td>
<td>13.5 ( \mu A )</td>
</tr>
</tbody>
</table>

Performing sample and output simulations of the class AB memory cell across slow, typical and fast process parameter sets with a 100\( \mu A \) input current gives the results shown in Table 3. Clearly the current copying accuracy is better than 13bit across the full process range, although it must be stated that charge injection effects due to mismatch of the switch transistors will almost certainly degrade these accuracies.

Conclusion: A novel class AB memory cell suitable for a current mode ADC or DAC has been described and simulated. The design significantly reduces the static bias current and offers the advantage of reduced power consumption while increasing the maximum allowable signal amplitude. By careful consideration of the necessary bias voltages and the use of a novel class AB architecture, the input current range is greatly extended beyond that available with previous current memory cells. Current copying accuracy of 13bit or better has been simulated.

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References