A Design for Testability Study on a High Performance Automatic Gain Control Circuit

A. Lechner[1], A. Richardson[1], B. Hermes[2] & M. Ohletz[3]
[1] Lancaster University, Engineering Department, Lancaster, LA1 4YR, UK.
[2] Philips Semiconductors, Millbrook Industrial Estate, Southampton, SO15 ODJ, UK.
[3] Universität Hannover, Institut für Theoretische Elektrotechink, 30167 Hannover, Germany.

Abstract

A comprehensive testability study on a commercial automatic gain control circuit is presented which aims to identify design for testability (DfT) modifications to both reduce production test cost and improve test quality. A fault simulation strategy based on layout extracted faults has been used to support the study.

The paper proposes a number of DfT modifications at the layout, schematic and system levels together with testability guidelines that may well have generic applicability. Proposals for using the modifications to achieve partial self test are made and estimates of achieved fault coverage and quality levels presented.

Keywords: Design-for-testability, mixed signal, test, integrated circuit, I_{DDQ}

1 Introduction

The escalating cost of testing analogue functionality in mixed signal VLSI has become a problem requiring an urgent solution. In this paper, the testability of a commonly used mixed signal macro, an automatic gain control circuit (AGC) has been investigated & improved. This has been achieved through the application of a structured, hierarchical design for testability (DfT) methodology validated by a robust fault simulation strategy. The objective of the work is to both reduce test cost and test escapes and hence improve test quality to a level now achieved for digital IC's through scan and I_{DDQ} test strategies. The circuit is particularly problematic as its configuration can be changed, the gain varied and its feedback path tends to reduce the impact of faults on primary measurands. A defect oriented test approach has been applied involving detailed fault simulation to determine the fault coverage and clearly define the testing problem. In order to optimise the testability, difficult to detect faults have been examined in detail, leading to DfT improvements involving layout modifications, additional circuitry to support current testing and the integration of test modes capable of reconfiguring parts of the circuit to support partial built-in self test (BIST). Generic DfT guidelines at the schematic and layout level, which can be applied in the early design stages to prevent time consuming redesign, have been generated.

1.1 State-of-the-Art in Analogue and Mixed Signal Testing

In the digital domain, design for testability (DfT) is well established[1], with full or partial scan[2] being implemented successfully in the majority of complex products. In addition, the IEEE standard 1149.1 test access port and boundary scan architecture[3] has been well accepted by digital designers. Due to the dramatic increase in complexity of digital circuits, built-in self-test (BIST) has been realised mainly in highly structured commercial designs to implement some of the test functions on-chip.

Currently, functional testing is performed on analogue circuits after wafer processing, where every IC is checked against critical specifications[4,5]. The optimisation of such circuit specific test programs is difficult to handle and expensive due to the required engineering resources. Additionally, neither the test quality nor the yield can be estimated, as the product is not directly tested for defects. Generic DfT guidelines which can be applied in the early design stages and practical mixed signal BIST could pave the way to satisfying industrial demands for the use of digital only testers[6,7]. Increasing test cost, aggressive time to market (TTM) and the need to improve product quality is currently driving this change in test philosophy. Finally, it should be noted that for many highly safety critical applications, DfT is already essential, as in many cases the circuit has to be highly testable and capable of on-line verification.

An overview of defect oriented testing and DfT optimisation of mixed signal ICs is presented in[5,8]. Several DfT studies have been published, including work on a current mode DAC where test vectors are optimised and

redundancies removed[9], on analogue filters where the controllability and observability is improved to test a number of stages separately[10,11,12,13] and on flash ADC[14,15]. Motivated by the success of the 1149.1 scan bus, the IEEE Mixed-Signal Testability Bus Standard P1149.4 has been developed[16, 17] which despite little interest to date, is likely to radically improve test access at the chip level. The Analogue Circuit Observer Block[18] reduces the need for precision by encoding the data during circuit test. A DfT system level architecture, using the sw-opamp concept[19], improves the controllability and observability in a multi stage circuit and includes off- and on-line tests with BIST capabilities[13]. A similar demonstrator has been chosen for AUBIST[20,21] which compares the output response of cascaded biquads. The multifunctional ABILBO structure includes a test stimulus generator (TSG), output response analyser (ORA) and an analogue scan path. Further proposals have been made to realise a pure analogue BIST. The TBIST[22] translates parameters at certain circuit nodes into a proportional DC voltage to verify whether a parameter (gain or phase) is inside specification. The ABIST[23,24] allows parallel loading of test data (voltages or currents) into a buffer and serial transfer to the output. The structure has been extended for mixed signal circuits in order to implement one structure that enables digital and analogue BIST[25]. The HBIST concept[26] includes an on-chip TSG that converts digital test patterns to a test stimulus, and is realised by the reconfiguration of cells already present to perform the digital BIST. Other concepts suitable for mixed signal circuits where the digital kernel is surrounded with analogue sub-circuits on the input and output, are the MADBIST concept for ΣΔ converters [27,28,29] and the BIST for the converters on a single-chip CODEC[30]. The OBIST technique[31], suitable for both functional and defect oriented testing, is based on the oscillation test methodology. Finally, a promising approach to calculate analogue parameters for DAC's and ADC's has been presented by Sunter and Nagi[32].

In the majority of cases, the effort and initial financial investments required to integrate DfT are usually justified, as either test cost or test quality is improved. Additional benefits are gained where the design becomes part of a cell library or is intended for re-use. Most DfT methodology should also be re-usable to be industrially practical.

In this paper, some easy to apply DfT guidelines and structures are presented which are transferable to other mixed signal designs. The improvement in test quality and the reduced demands on external automatic test equipment (ATE) are presented and justified in the following sections. In section 2, the AGC structure is summarised together with the functional tests currently applied. The fault simulation approach, including the fault list generation and fault simulation models used are presented in section 3. Section 4 describes the DfT study including several DfT optimisations at the layout, schematic and system level. Finally the paper concludes with a discussion and future issues.

2 The Automatic Gain Control Circuit (AGC)

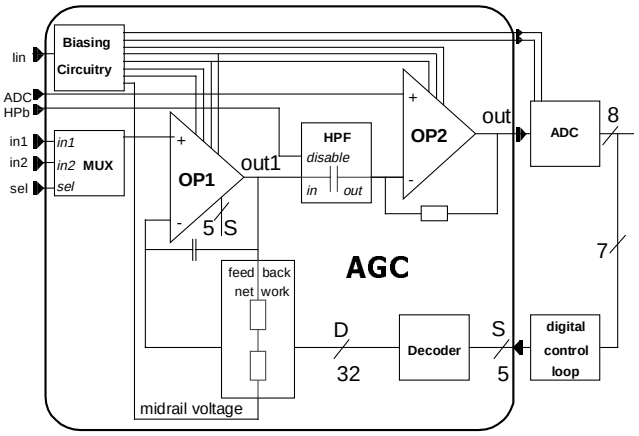

Figure 1 : Simplified AGC structure

The demonstrator is an AGC macro used to digitise sound signals. As depicted in figure 1, the input stimulus is fed to an adjustable high bandwidth OTA (*OP1*) in a non-inverting configuration whose gain is controlled digitally. The gain can be varied in 32 steps by a decode on the 5-bit gain set *S* provided by the digital control loop. The high pass filter (*HPF*) with a 3 dB corner frequency of 3.5 MHz is controlled by the top level signal *HPb* and can be by-passed. The second stage of the AGC is an inverting folded cascade OTA (*OP2*) providing a level shift, as the output (*out*) is referenced to the 24.57 MHz flash-ADC mid-ladder potential.

The AGC, containing 544 CMOS transistors, 394 in the digital converter, has been designed in a 1.0µm single poly double metal CMOS process and occupies 0.4 mm^2 of silicon. A typical test plan for the AGC circuit is listed in table 1.

1	AC performance in all gain sets (gain peaking, group delay)
2	DC offsets in 3 gain sets using Monte-Carlo analysis
3	Transient response to switched capacitor load.
4	Transient response to input sinusoid at two frequencies

Table 1: Functional test program

The main test problem for this circuit is the variable gain. Furthermore, two inputs and the configuration with en-/disabled *HPF* need to be tested. A massive reduction in test time could be achieved by reducing the number of gain

sets that the circuit needs to be switched into during test. Reductions in test cost can also be realised by on-chip test response evaluation or pre-processing. The surrounding digital and mixed signal cells should be taken into account in order to reduce the demands on external ATE.

The goal of this paper is to investigate these possibilities through extensive fault simulation. A defect oriented approach has been adopted based on the success of the technique on related projects.

3 Analogue Fault Simulation

Defect oriented testing has the potential to decrease test time and cost whilst improving test quality. The costs for collecting process and defect statistics and creating simulation models can be significantly reduced if hierarchical defect oriented fault simulation is embedded within the design cycle, using appropriate CAD tools. The trend towards cell based system design creates a demand for analogue libraries containing testability optimised cells, including macro fault models and test strategies. Once this is achieved, the DfT and fault simulation problem can be transferred to a higher design level.

The quality of any fault simulation strategy strongly depends on the simulation models used and the applied fault set. Fault simulation models have to be developed to transfer an electrical interpretation of several physical defect mechanisms to the schematic level. For a set of faults, the corresponding fault simulation models are inserted at the schematic level and simulated. The fault coverage (FC) can be determined through a comparison of the faulty and the fault free test response by taking realistic fault detection criteria into account.

In section 3.1 the fault list generation is described, followed by a presentation of the fault simulation models used, (3.2) the fault simulation methodology and the estimation of fault detection criteria (3.3).

3.1 Fault List Generation

Currently, a number of different techniques are used to generate fault lists for analogue circuits[33,34,35]. In this study, the fault list has been extracted from the layout using the Inductive Fault Analysis (IFA)[36] tool VLASIC[37]. The resulting layout extracted fault list contains several kinds of shorts (inter-node, inter-resistor or shorts affecting multiple nets) and opens. The main advantage of this fault list is that a weighted fault coverage (WFC), taking the fault probability into account, can be computed and difficult to detect faults can be related to certain layout structures[38, 39]. To enable fault simulation prior to layout, the re-use of DfT optimised cells and their corresponding layout extracted fault list is a promising compromise. Other techniques link typical schematic level structures, like current mirrors, differential stages, etc., to a list of likely and realistic faults without layout information[40, 41].

3.2 Fault Simulation Models

Fault simulation results have to be linked to the fault list considered and the fault detection thresholds used. Due to the lack of commonly used fault models, those injected into the netlist in this work will be presented briefly in this section. Detailed information about failure mechanisms and defects can be found in[42,43,44].

Short: For any kind of short the built-in resistor model is inserted at the schematic level. If a (polysilicon or diffusion) resistor is connected by a defect to another net, the affected resistor is split in two, each having half the value. For shorts between more than two nets and/or resistors (fig. 2.a) the short-resistor will be split in the same way. The value of the built-in resistor model depends on the spot defect size and exact location[45]. During the fault simulation, a minimum value of 0.2 to 20Ω, depending on the kind of defect, and a maximum value of 1kΩ is used. A short will be classified as detected if both of the resistor values, the upper and the lower, result in a detectable deviation during the applied test program.

Opens at device terminals, inside a resistor and at split nodes (fig. 2.b) will be modelled by a 10MΩ resistor.

Floating Gate Transistor (FGT): The modelling of the floating gate transistor is not easy to handle[46]. For the simulation model used, the following assumptions have been made:

- large opens, means no tunnelling.[47]
- crack close to the gate area.
- coupling from drain (and channel) greater than any other capacitive coupling.[48]

The gate to source voltage that defines the behaviour of the FGT can be given as:

$$V_{gs} = \beta \cdot V_{ds} + \gamma;\ \begin{array}{l} NMOS: \beta = 0.2; \gamma = 0.5V; V_{gs} > 0V; V_{ds} > 0V \\ PMOS: \beta = 0.2; \gamma = 0.2V; V_{gs} < 0V; V_{ds} < 0V \end{array}$$

The term $\beta \bullet V_{ds}$ characterises the coupling and γ represents the initial positive charge on the floating gate caused by the plasmas used for etching in IC fabrication[48]. The replacement model is shown in figure 2.d.

Source Drain Path (SDP): A polysilicon crack in the active gate area results in a smaller width and a diffusion path between source and drain[49]. The corresponding simulation model is shown in figure 2.c. The width of the transistor is assumed to be 50% less in this case with the diffusion path modelled by a resistor. Concerning the fault simulation of the AGC, some devices have a folded poly gate structure, thus the width of the transistor will not be

reduced by a SDP. The value of the resistor R_{crack} has been calculated at 100Ω for a squared defect (1µm•1µm) of missing polysilicon. As a crack will have a much smaller size, the simulation model for the SDP includes a 1 kΩ resistor between drain and source.

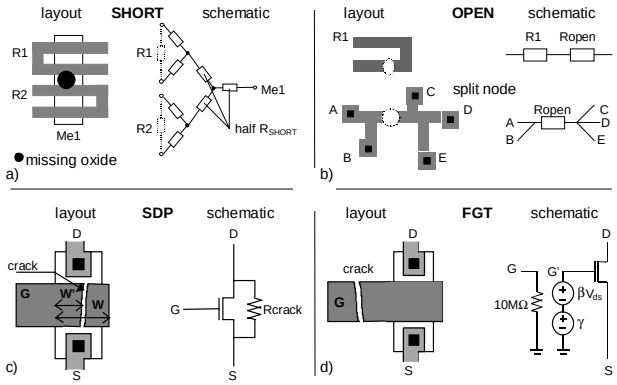

Figure 2: Fault simulation models

3.3 Fault Simulation and Fault Detection

The analogue fault simulation tool AnaFAULT[50] has been used to run the fault simulation. In addition, the ATE resolution, process variations and specification tolerances are simulated using Monte Carlo analysis to estimate realistic fault detection thresholds.

For future research, the computer aided test (CAT) tool, CADEFSIM, that has been embedded into the design environment and successfully demonstrated by Lancaster University[38] will be used. This software enables the generation of a layout extracted fault list by a critical area extractor and allows both schematic based fault simulation and the graphical output of computed FCs without leaving the design environment.

4 Design for Testability Optimisation at the Layout, Schematic and System Level

The generation of an optimum test program for the AGC presented in this section is based on fault simulation against layout extracted faults, as described in section 3. Using this approach, test quality can be calculated in three different ways, referred to as fault coverage (FC), weighted fault coverage (WFC) and quality estimation in parts per million (ppm) defect levels as given in equation 1[38]. WFC and quality prediction can be achieved because the layout extraction process is statistical involving defect extraction on a batch of devices that is a variable number in the defect extraction tool.

Note that the equation for WFC simply takes into account that some faults will be highly probable and statistically occur on a greater number of devices in a batch than other faults. It hence makes sense that the fault detectability of a certain test should be "weighted" by this "probability" figure.

$$FC = \frac{\sum_{n=1}^{N} Dn}{N} \cdot 100\% \qquad WFC = \frac{\sum_{n=1}^{N} Dn * Wn}{\sum_{n=1}^{N} Wn} \cdot 100\%$$

$$FDL = \frac{\sum_{n=1}^{N} W_n - \sum_{n=1}^{N} D_n \cdot W_n}{B - \sum_{n=1}^{N} D_n \cdot W_n} \cdot 1e^6 \text{ppm} \quad (1)$$

FC:	Fault Coverage	N:	no. faults simulated
WFC:	Weighted Fault Coverage	B:	no. devices in batch
FDL:	Faulty Device Level (ppm)	Dn:	binary function,
Wn:	total number of circuits in the batch affected by fault *n*		detected=1, undetected=0

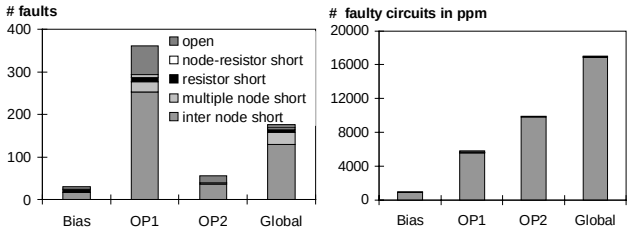

Figure 3: Location of faults and affected circuits in ppm

In the layout extracted fault list, 511 faults affected the digital converter, a FC of more than 99% has been proven for the digital test. Analogue faults are related to the cells affected in figure 3, where inter-cell shorts are grouped in *global*. It can be deduced that most faults (361) affect *OP1* (fig. 3.a), while the most likely faults are located in *OP2* and the global circuitry (fig. 3.b). These are the shorts in *OP2* and the *HPF* capacitors. It can also be seen that shorts between two nodes are more likely to occur than shorts affecting resistors or any kind of open. However, for each test, 624 different faults need to be considered resulting in 1150 simulations, as shorts have to be simulated with the upper and lower value for the resistor simulation model (sec 3.2).

4.1 Ramp Stimulus Test

Several AC, DC and transient simulations have shown that the AGC circuit should be switched in at least two gain sets to achieve an acceptable fault coverage. Due to the implementation of *OP1*, the gain sets S_1 = 01010 and S_2 = 10101 have been chosen. Furthermore *HPF* has to

be disabled. A ramp stimulus has been applied to the first input (*in1*) of the analogue multiplexer and characterised in such a way that the analogue test response will cover the whole input range of the ADC connected to the analogue AGC output (see fig. 1). During test mode, digital cells need to be reconfigured in order to count rising or falling

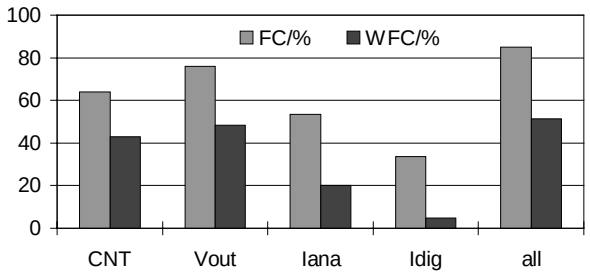

Figure 4: Fault coverage - ramp stimulus

edges of the ADC's least significant bit (LSB). For the fault simulation, a very simple behavioural model of an 8-bit ADC has been used, and the counter has been written as a special fault detection software routine. In future projects the ADC, the 8-bit up/down counter and layout extracted faults for both cells will also be considered.

During the transient fault simulation, the rising and falling edges of the LSB are counted (CNT), the analogue (Iana) and digital (Idig) current consumption monitored and the analogue output voltage (Vout) measured. The calculated fault coverage figures are depicted in figure 4. The difference in the fault coverage between the LSB counting method and the output voltage measurement (Vout) results from a wider tolerance assumed for the ADC output. Once the converter's characterisation is taken into account, the achieved FC should be the same as for the analogue output voltage. It can be seen from the simulation results above that the overall fault coverage for both tests is 85.1% (51.28% WFC).

4.2 Additional DC Test

The test program has to be expanded by the inclusion of a simple DC measurement that includes the *HPF* being enabled and the use of the second analogue input (*in2*, fig.1). This DC test has been designed so that the fault free output voltage is at 2.0V, which is half way between the ADC mid-rail voltage (1.5V) and the maximum of the input range (0.5V - 2.5V). Fault coverage may be assessed by monitoring either the analogue output voltage or the output pattern of the ADC. As shown in figure 5, the FC is improved by 1.8% (WFC by 40%) approximately. The major increase in WFC originates from the detection of the capacitor short in the *HPF* that has a relatively high

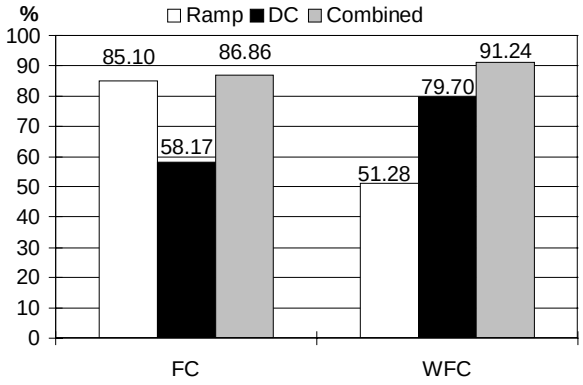

Figure 5: Fault coverage for DC and ramp test

occurrence due to its large area. However, 82 faults reported, affecting 2951 ppm, remain undetected. In the following section, previously undetected faults will be classified and analysed, DfT optimisations are presented for each class of difficult to detect faults.

4.3 Test Program Optimisation

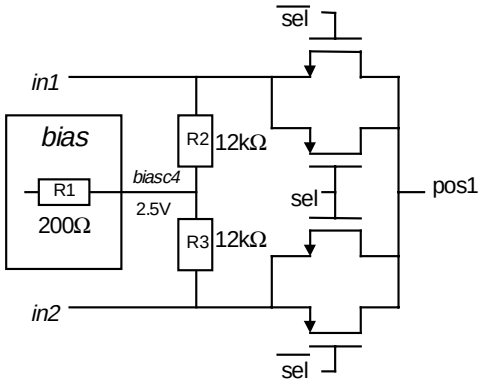

Figure 6: Input Multiplexer *MUX*

Some faults cannot be detected by the tests presented above:

- Two faults (12 ppm) are not detected, as they affect nets which are used by cells not included in the AGC circuitry. In the context of fault coverage they will be considered as detected externally.
- Five faults (9 ppm) affect the digital part of *OP1*. As an exhaustive test will be run on the digital decoder, these shorts will be detected during the digital test.
- Two opens (18 ppm) at the resistors connecting the analogue inputs to the mid-rail voltage (R2 and R3 in figure 6) have not been detected. These faults can be detected by measuring the voltage at the floating input *in2* (*in1*) during the ramp (dc) test.

4.4 DfT Layout Optimisation

The AGC design contains two resistor ladders, one in the *biasing* cell and a second in the *feedback network*. The layout structure is shown in figure 7a. Defect 1 causes a short between resistors R2 and R3 but the fault is likely to be undetectable. In the fault simulation, even defects such as defect number 2 will not be detected in all cases, while defects 3 and 4 result in a parametric fault affecting R1,

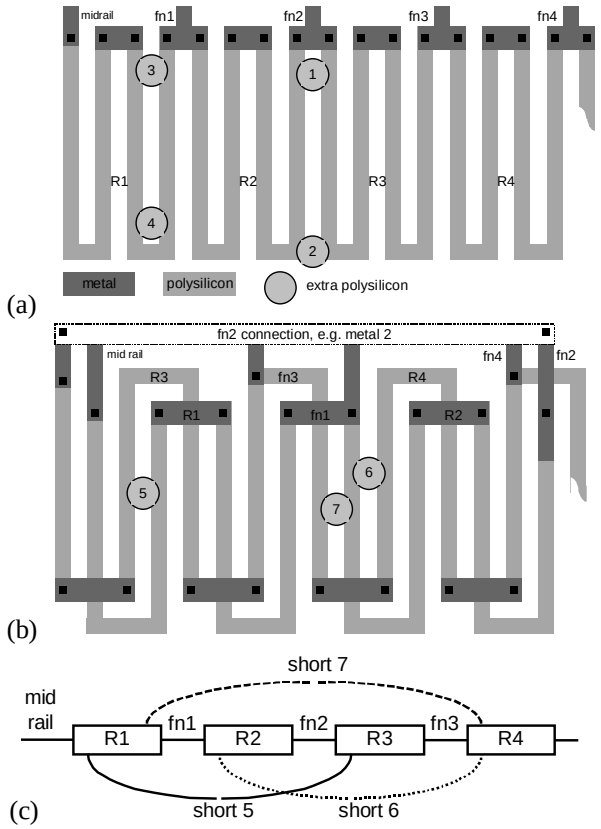

Figure 7: Present and improved layout of resistor ladders

which has not been reported by VLASIC. It should be noted that the VLASIC output will only list faults which result in a changed netlist, thus parametric faults are excluded. If the layout is improved, as proposed in figure 7.b, spot defects can neither cause a short between resistors connected to each other nor parametric faults that affect only one resistor. For example defect 5 shorts R1 and R3 (see figures 7.b and 7.c) which result in equal voltages at the nodes *fn1* and *fn2*. Defect 6 will cause the same voltages at *fn2* and *fn3*. If the resistor layout is changed in this manner, all resistor shorts in the *biasing* cell will be detected. Concerning the resistor ladder in the *feedback network*, the AGC would have to be tested in all 32 gain sets. A DfT optimisation at the system level is proposed in section 4.7, assuming that the improved layout has been implemented. An initial DfT guideline can be developed:

Concerning resistor layouts, adjacent polysilicon (diffusion) tracks should not belong to the same resistor to prevent parametric faults caused by extra resistive material. Additionally, adjacent tracks should not belong to resistors connected to each other, as shorts affecting these tracks are difficult to detect.

4.5 DfT at Schematic Level to Detect Faults Affecting Cascode Transistors

The AGC design does not provide a stand-by mode to reduce the power consumption, this is however not the case in the next generation designs. In figure 8, a section of the *OP1* schematic is shown, including the most likely undetected faults (*F1* to *F7*). One way to reduce the current consumption from more than 1mA to less than 10μA is, to switch V(*biasc2*) to *VSS*. If a faulty circuit contains the short *F7*, the fault will be detected by a current measurement on the AGC. Alternatively V(*biasp*) can be switched to *VDD* and four faults can be detected in the same way (*F1* to *F4*). Switching V(*biasn*) to *VSS* would result in a current consumption of less than 0.4mA. *F5* and *F6* could then be detected. It has to be mentioned that the AGC performance will not be affected, only 12 additional transistors of minimum size have to be implemented to switch three biasing voltages. The WFC increases approximately 3%, corresponding to 1036 ppm. Furthermore, similar faults will be detected in *OP2*, 568 faulty circuits out of one million can be classified as faulty, resulting in an increase of about 1.7% in the WFC. A DfT guideline can be formulated:

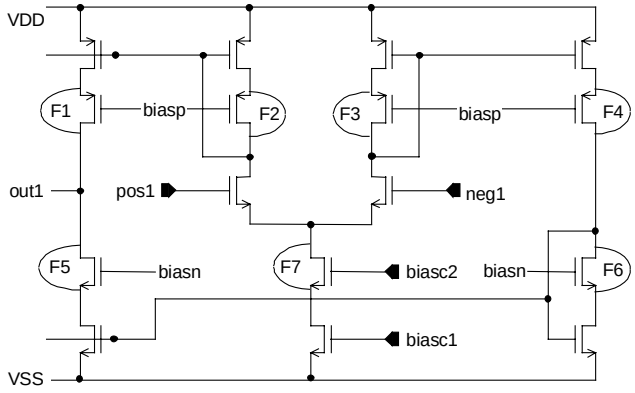

Figure 8: Section of *OP1* schematic

The current consumption and / or the output voltage has to be made more sensitive in stand-by mode in order to detect drain to source shorts at cascode transistors.

4.6 DfT Optimisation at the Schematic Level to Detect Faults by Local Current Comparison

Some shorts within the *biasing* cell (fig. 9) have not been detected. In the fault free case, the current in branch 6 (I_6) is 17.84 µA while the input current *inbias* is equal to 17.55 µA. Most faults result in a significant change in I_6. However, by measuring the current consumption of the cell, no faults will be detected due to the wide tolerances that have to be assumed for analogue current measurements.[51] A solution here is to compare *inbias* and I_6 on chip. Four faults (878 ppm) can be detected using this technique as in the fault free case, I_6 is significantly larger than *inbias*. A similar design for current testability approach is presented in[52] where an on-chip current generation avoids global process variations and only relative ones must be accounted for. Future research will either utilise existing on-chip techniques[53] or develop alternative solutions for the implementation of built-in (programmable) local current comparators to provide a pass-fail output or diagnostic output.

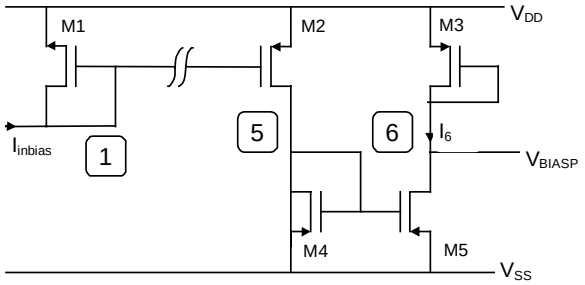

Figure 9: Section of *biasing* cell schematic

4.7 DfT Optimisation at the System Level

As mentioned above, the primary test problem for the AGC is the need to test in all gain steps. An alternative test program can be generated which checks the *feedback network* implemented as discussed in section 4.4. If this part of the circuit can be proven fault free, the AGC needs only to be tested in three gain sets (see sections 4.1 and 4.2). Figure 10 shows the *feedback network* including the additional devices in the shaded area. Additionally the digital decoder has to be reconfigured in test mode in such a manner, that the original 32-bit code *D (see figure 1)* is changed to a new 32-bit code:

$$e_i = d_i + \left(d_{i+1} \cdot test\right) \text{ for } i = 1,\ldots,32 \qquad (2)$$

In operational mode (test=0), *E* is equal to *D*. In test mode (test=1), *E* is a 32 bit code containing a walking pair of bits (as illustrated in table 2). By initiating this sequence in the digital control loop that feeds the decoder, the comparator (*COMP* in fig.10) will check if the voltages *v(fn1)* up to *v(fn32)* are in a decreasing (or increasing) order. This test can be run in parallel with the stand-by mode test for faults in *OP1*, as its output can be driven to *VDD* or *VSS*. Future work will examine the use of the sw-opamp design[13,19] as the structure of *OP1* and *OP2* is compatible with this approach.

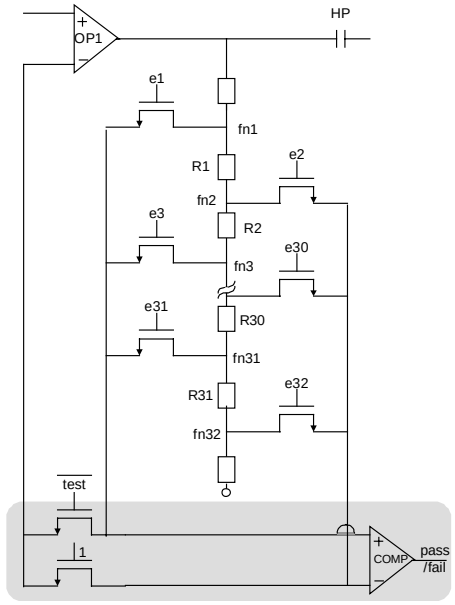

Figure 10: Testing of the *feedback network*

S	d_{32}	d_{31}		d_4	d_3	d_2	d_1	e_{32}	e_{31}	e_{30}		e_4	e_3	e_2	e_1	COMP
00000	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	
00001	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1	v(R1)
00010	0	0	0	0	1	0	0	0	0	0	0	0	1	1	0	v(R2)
00011	0	0	0	1	0	0	0	0	0	0	0	1	1	0	0	v(R3)
11110	0	1	0	0	0	0	0	0	1	1	0	0	0	0	0	v(R30)
11111	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	v(R31)

Table 2: Reconfiguration of digital converter

4.8 Resulting Fault Coverage

Several testability optimisations have been proposed in the previous sections. In addition to two shorts (46ppm) in the *biasing* cell, the following faults remain undetected:

- One open (1 ppm) in *OP1* and two shorts (147 ppm) inside current mirrors of *OP2* are not detected.
- One fault (10 ppm) shorts the ESD protection resistor (R1 in figure 6) at the output of the *biasing* cell. As its value is much smaller than R2 and R3, the short cannot be detected by testing the analogue part of the AGC.

The maximum FC and WFC achievable by the DfT optimisation is **99.04%** and **99.39%** respectively. In figure 11 the fault coverage for the complete test program of the DfT optimised AGC circuit is shown. This includes the

ramp test, DC test, the stand-by mode of both opamps, current comparison for the *biasing* cell, *feedback network* test, digital test, gain measurement, and the measurement of the floating analogue inputs.

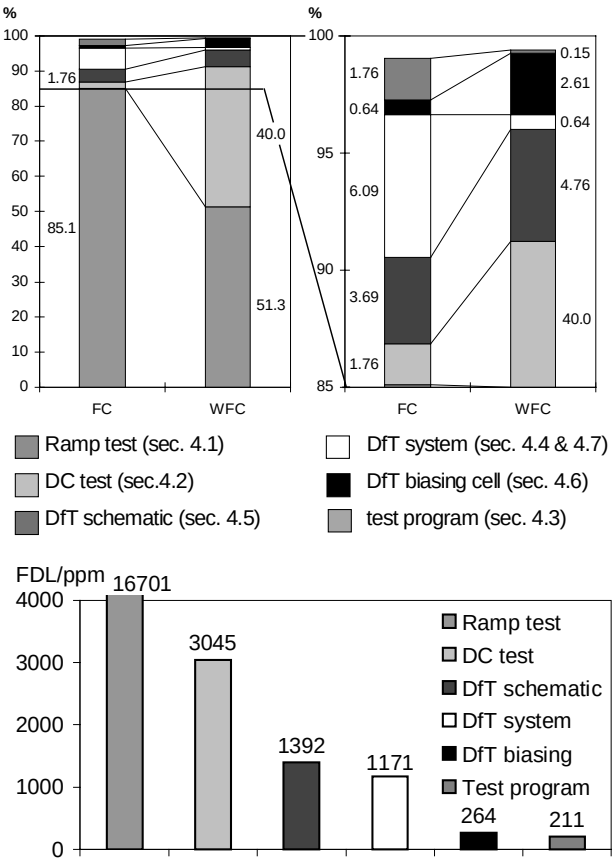

Figure 11: Fault coverage increase due to DfT optimisations

5 Conclusions

In this paper a comprehensive DfT study on a commercial AGC design has been presented. The testability analysis process has been based on fault simulation against layout extracted faults and has lead to a number of DfT modification proposals at the layout, schematic and system level. Generic guidelines drawn in this paper are applicable to the majority of other analogue and mixed signal design and can be taken into account before layout generation. Thus difficult to detect faults can be prevented or the faulty behaviour of the circuit will be easier to detect.

To improve testability, a number of new test strategies have been proposed including a ramp stimulus test, as I_{DDQ} test and a DC measurement. DfT modifications to support the ramp test include additional digital circuitry to reconfigure present digital cells to count rising or falling edges. Additional structures need to be implemented to modify the 32-bit converter output pattern in test mode and to support current testing.

In addition, an important layout modification has been proposed to reduce the probability of difficult to detect parametric faults. These modification allow test time to be reduced by minimising the number of gain sets the circuit must be tested in and boosts fault coverage to over 99%.

Future work on the AGC will target parametric faults and faults affecting the surrounding circuitry. In addition, test time and test cost need to be estimated. The implementation of an on-chip test stimulus generator and on-chip programmable local current comparator will address the realisation of BIST for a large number of typical mixed signal systems. For this purpose, further DfT guidelines will be generated from additional studies on a sub-set of typical analogue macros. The time to invest in these new DfT studies can be reduced significantly taking the experience and results of this work into account.

1	*Prevent difficult to detect shorts between resistors connected to each other. Adjacent resistive tracks should not belong to resistors connected to each other (sec. 4.4)*
2	*Realise stand-by mode by switching gate potentials of cascode transistors to the power supply in order to detect faults affecting cascode transistors (sec. 4.5)*
3	*Reduce demands on ATE (on-chip test support), pre-process test response on-chip through re- use of existing mixed signal and digital structures (sec. 4.1)*
4	*Run simple separate test in reconfigurable structures, such as the AGC feedback network (sec. 4.7)*
5	*Reduce redundancies*

Table 2: Summary of DfT issues identified

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