A Failure Mode Analysis of a 6-bit Folding ADCs

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Abstract

For next generation mixed signal ICs, the integration of Design-for-Testability and Built-In Self-Test structures is expected to be of crucial importance for satisfying quality and economic demands. The judgment and evaluation of such testability optimisations, however, requires a better understanding of circuit specific failure modes in deep sub-micron technologies. This paper presents fault simulation results for a 6-bit folding ADC carried out to identify key failure modes and extract its test requirements.

1. Introduction

Functional testing is the dominant test methodology applied to ADC macros in industry today, to verify that the circuit under test (CUT) meet its specifications under test conditions. This approach can result in excessive or insufficient testing, is in most cases too expensive to implement and doesn't provide a link to a test coverage metric. An attractive alternative to functional testing is the use of defect-oriented techniques. Here the CUT is verified against a set of faults, through both specification and parametric measurements. As the objective of these techniques is to detect faults caused by physical defects, a quantitative test coverage can be predicted through fault simulation, enabling testability improvements, and the identification of difficult to test faults and structures.

For most test methodologies, it is essential to understand the faulty behaviour of the target CUT. The motivation for applying effort here is not just to optimise today's testing but to address urgent future issues. For example, the SIA roadmap [1], predicts decreasing yield figures (50% by 2014) and test costs exceeding manufacturing costs if no advances are made. The development of Built-In Self-Test (BIST) structures and Design-for-Testability (DfT) optimisations for mixed signal IC components is therefore essential and must be supported by new fault models, failure analysis data, and computer-aided test tools to realise a more structural test methodology. The work presented in this paper also supports the motivation for an integration of DfT, design-for-manufacturability, defect-oriented test approaches and

BIST for analogue and mixed signal ICs, which is discussed in [2]. An example for BIST and DfT optimisation of an automatic gain control circuit based on a better understanding of its failure modes can be found in [3].

This paper discusses typical failure modes in a new ADC design, caused by processing defects. A detailed investigation into ADC failures is expected to lead towards more accurate test quality prediction and a better understanding of ADC failure modes and test requirements. The design studied is described in section 3. The fault simulation technique is summarised in section 4, followed by an illustration of ADC failure modes (section 5). Resulting test requirements are discussed in sections 6. Finally the paper concludes with a discussion and future issues.

2. BIST for ADCs

BIST for analogue macros has been identified as one of the major advances required for the use of cheaper digital-only and mixed signal testers, system-on-chip test, and the growth of mixed signal reusable macros. For ADC's, a number of BIST techniques have been published recently.

Sunter and Nagi presented the polynomial fitting algorithm at the ITC'97, which is a method to extract DC offset, gain and harmonic distortion to 2nd and 3rd order harmonics from the coefficients of a third order polynomial [4]. These coefficients are extracted from four integrals computed when a ramp stimulus is applied to the converter.

Oscillation-based testing has been proposed for a number of analogue macros. The CUT is reconfigured where necessary and placed into oscillation. The technique is in the majority of cases a more defect-oriented approach and not directly linked to specifications, as the oscillation frequency is observed for fault detection.

ADCs are historically tested by applying a known input stimulus and evaluating the statistical distribution of the converter's output codes, through mapping to a histogram. When the number of occurrences of each output code is correlated against the input stimuli,

specifications, such as DNL, INL, gain and offset error can be determined. Frisch and Almy presented a histogram-based BIST for ADCs, called HABIST [5]. A technique to minimise this area overhead by the use of time decomposition has been published [6].

BIST for ADCs seems the most promising and realistic on-chip test support solution for analogue macros. However, test quality figures for the techniques proposed are unknown. There is currently little data that summarises the probable spectrum of fault behaviour associated with converters implemented in deep sub-micron technology. Realistic quality improvements through design or DfT need this information. In the long term, fault simulation requirements may even be reduced by the definition of fault simulation models representing groups of faults resulting in similar failure modes. This would enable a faster and more accurate evaluation of existing and future BIST and DfT techniques in terms of test coverage capability.

3. 6-bit folding ADC design

The converter under investigation, a 6-bit 330MS/s differential folding ADC. It is implemented in a 0.3?m standard CMOS process. The layout occupies $0.1mm^2$ of silicon, contains 1050 transistors. 75% of the silicon area is dedicated to analogue circuitry.

The analogue section of the converter comprises a resistor ladder to generate the differential reference voltages, two amplifier arrays, a track and hold array, and a comparator array, as illustrated in Figure 1. Two groups of signal paths can be identified. The first group of signals contributes to the calculation of the four lower bits, d_0 to d_3, while the second group determines the two higher bits d_4 and d_5. For each group the subcircuits contained in the five arrays (Figure 1) are identical, allowing a reduction in the number of faults to simulate, as explained in section 4. To further reduce fault simulation times, the digital encoding block and the clock generator have been replaced by simple behavioural models.
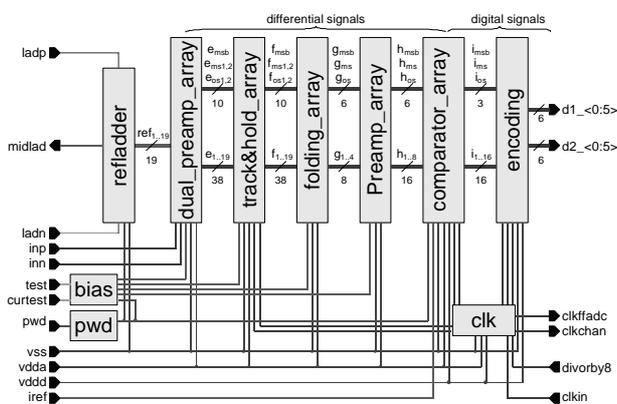

Figure 1: ADC block diagram

4. Fault Simulation of ADC

Fault simulations usually facilitate test quality computation, DfT optimisation, and the identification of difficult to test and difficult to detect faults [7]. Within this work, the approach has been adopted to extract information on failure modes for ADCs.

A fault list has been extracted from the layout based on a detailed investigation into DSM failure mechanisms.

Fault simulation models used (gate-oxide shorts, floating gate transistors, narrow MOS transistors and others) will be listed briefly in the final paper to provide essential background information.

The ADC's fault list obtained contains 4469 faults and includes probability data. As mentioned above, the converter contains a large number of identical sub-circuits composing two types of signal paths. Hence only faults affecting one lower bit signal path and one upper bit signal path are simulated. The reduced fault list contains 629 candidates (Figure 2). Taking fault probability data into account, the group of short (open) faults affects 94% (6%) of faulty devices due to defect statistics applied.
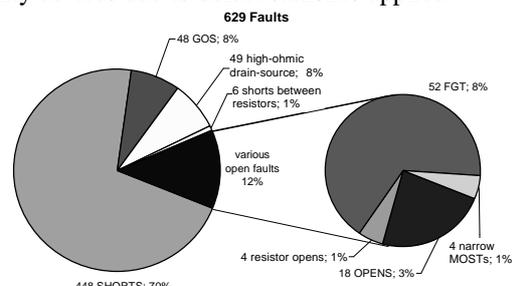

Figure 2: ADC fault set

4.1 Fault Simulation Analyses

A transient simulation for a ramp input stimulus has been chosen in order to evaluate the ADC's failure modes. The stimulus has been defined to cover the full ADC input range (tolerating offset and gain effects) and to allow sampling of the digital output at speed with 5 to 6 samples per code. Apart from computing the first and last transition edge to obtain offset and gain values, the number of code occurrences, minimum and maximum code width (CW), and the running sum of CWs up to a certain code, estimating integral non-linearity (INL), have been measured. Additionally, maximum output code increase and decrease, and the average current consumption at various voltage sources have been monitored. The converter has also been simulated in power down mode where the current consumption is computed. The digital circuitry has been replaced by a behavioural model to reduce simulation times. Simulating 622 faults for the ramp stimulus requires an approximate simulation time of 375 hours on a Sun Ultrasparc II. For our purpose this has

been acceptable, the use of behavioural models for non-fault-affected analogue circuitry, however, is expected to reduce the simulation time dramatically.

Ongoing simulations are performed to evaluate dynamic failure modes, where the converter is fault simulated against a typical functional test.

5. Failure Modes

Data analysis has been based on the use of fault coverage (FC) and weighted fault coverage (WFC), taking the fault probability into account [8], defined as:

$$FC = \frac{\sum_{n=1}^{N} Dn}{N} \cdot 100\% \qquad WFC = \frac{\sum_{n=1}^{N} Dn*Wn}{\sum_{n=1}^{N} Wn} \cdot 100\%$$

Dn: binary detection function
with *0* undetected; *1* detected fault *n* out of *N* faults
Wn: number of circuits containing fault *n*

Figure 3 summaries some of the data obtained. The fault coverage is illustrated for comparing *offset*, *gain* and *CW* against thresholds determined by the use of Monte Carlo process variation simulations. Estimating *INL* as mentioned above is common practise in some BIST techniques for ADCs. Furthermore, coverages for average current measurements during ramp simulation (*Meas*) and monotonicity (*mono*), and the accumulated FC (*Accu*) test are given.

The illustration below also presents data on the hardness of the failure mode exhibited. A significant proportion of short faults are only causing test failures when modelled by a low-ohmic resistor (1Ω to 20Ω), but remain within the tolerance window for higher ohmic shorts ($1k\Omega$). Applying a realistic test threshold (computed by Monte-Carlo simulations taking measurement resolution and other contributing factors into account), leads to an accumulated fault coverage of more than 82%. Widening the test thresholds by 200% will still lead to a FC of more than 75%. The measurement most sensitive to the threshold applied is the CW computation.

Further explanations and coverage figures (FC and WFC) for power-down tests and others will be included in the final paper.
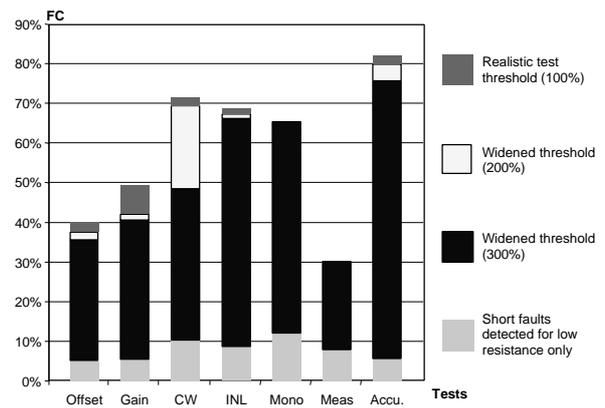
Figure 3: ADC failures

Figures 4 to 8 illustrate some of the failure modes observed for the ramp input stimulus.

The final paper will contain detailed descriptions on faults causing single test failures, for example CW only, and fault diagnosis capabilities. As depicted in Figure 7 and Figure 8, evaluating the number of local CW maxima allows some level of fault location. Also parametric faults will be addressed, leading towards a discussion on Design-for-Robustness for analogue circuitry.
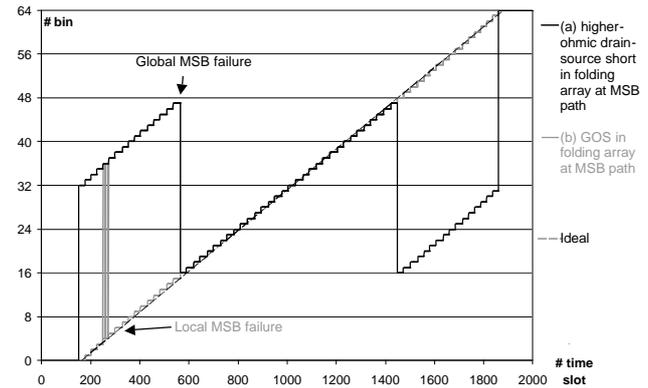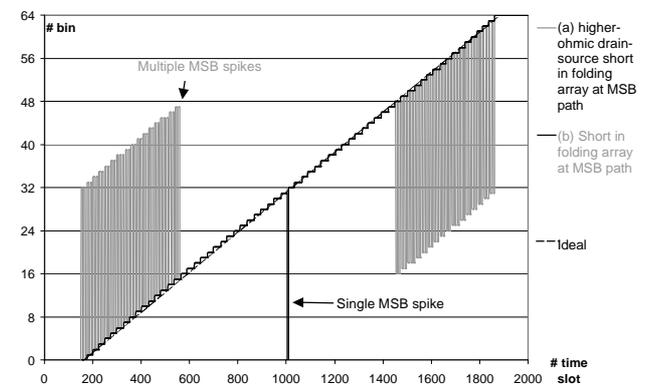
Figure 4: Non-monotonic behaviour I

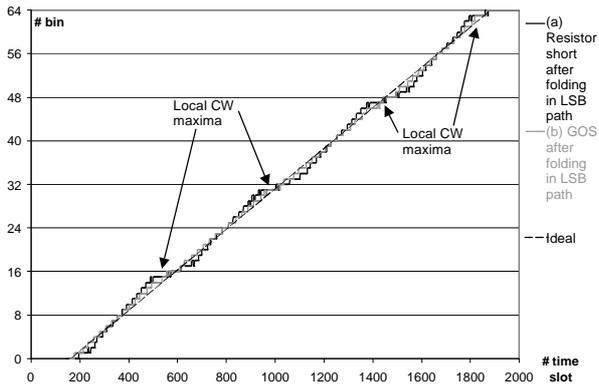**Figure 5: Non monotonic behaviour II**
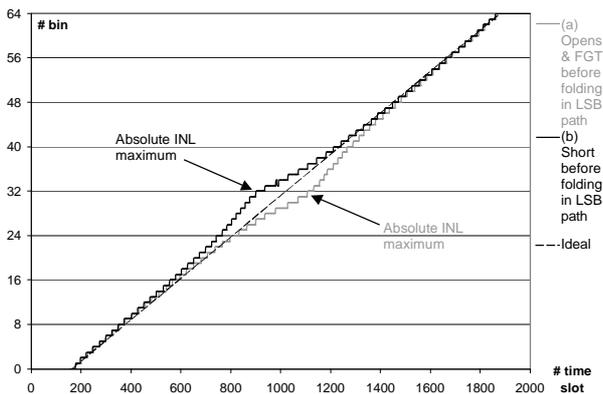
Figure 6: CW only failures
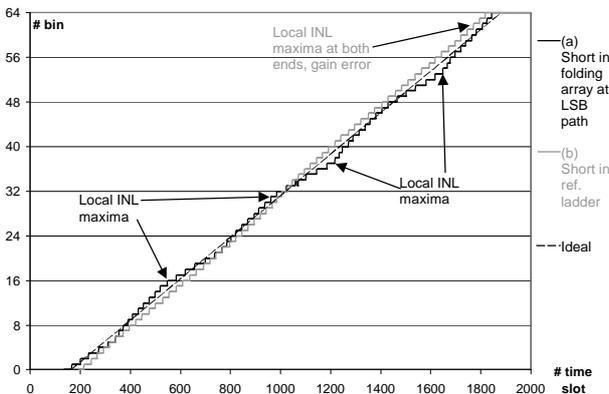

Figure 7: INL only failures I

Figure 8: INL only failures II

6. ADC test requirements

To summarise preliminary results it can be stated that 85 to 90% of faults exhibit failure modes detectable by DC specification measurements. While the majority of faults caused by process induced spot defects exhibit hard functional failure (missing codes, excessive DNL, non-monotonic behaviour), a large portion of the fault set, about 30 to 40%, will result in parametric functional failure only. Examples have been shown, indicating that process induced faults, such as shorts, opens, FGT, GOS etc can in fact cause performance to marginally fail specification, such as DNL or INL.

7. Conclusions & future work

The paper has identified failure modes of the target ADC. It has been shown, that a large proportion of traditionally considered shorts and opens and some other device oriented faults, such as GOS, FGT or SDP, contribute to failure modes missing performance specifications only marginally. Expected test coverage figures against the layout extracted fault set have been presented, that provide key data required for test program optimisation. BIST techniques published recently are expected to achieve fault coverages of about 80 to 90%.

More detailed analysis is required to pinpoint the prime test objective and potential quality problems. Detailed and time-consuming structural DfT studies utilising fault simulation environments seem to remain the only approach leading to a better understanding of analogue circuit specific failure modes. Computer-aided test tools currently under development will reduce required man-time, and new test coverage figures may eventually pave the way for test quality computation. Automating the test program generation and DfT optimisation itself, however, remains a challenge.

Ongoing and future work is addressing dynamic tests to further improve the understanding of failure modes. This may result in the use of defect-oriented, faster and cheaper tests which may also be supported by on-chip test support structures. Also work is required on the definition of appropriate coverage metrics.

Acknowledgements

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